

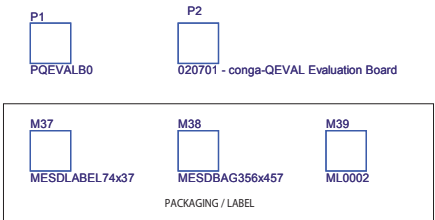
Qeval

Qseven Evaluation Carrier Board

Rev. B.0

Content

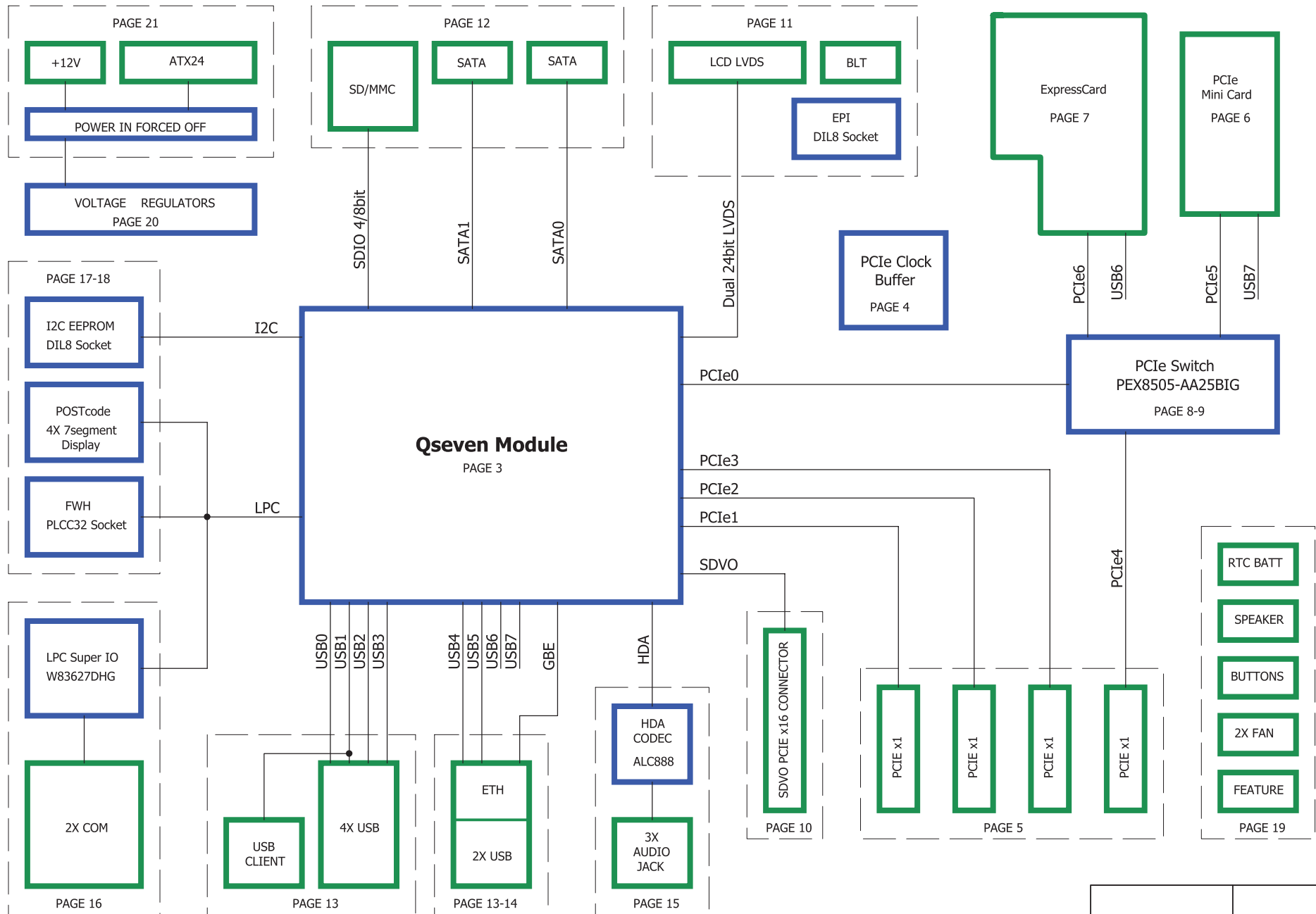
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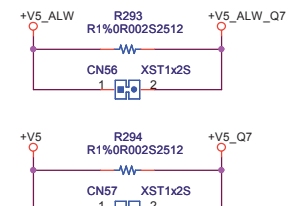
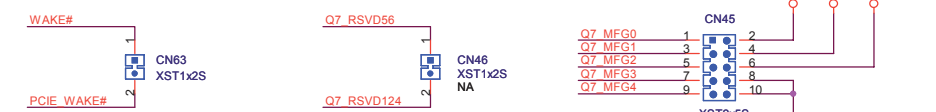
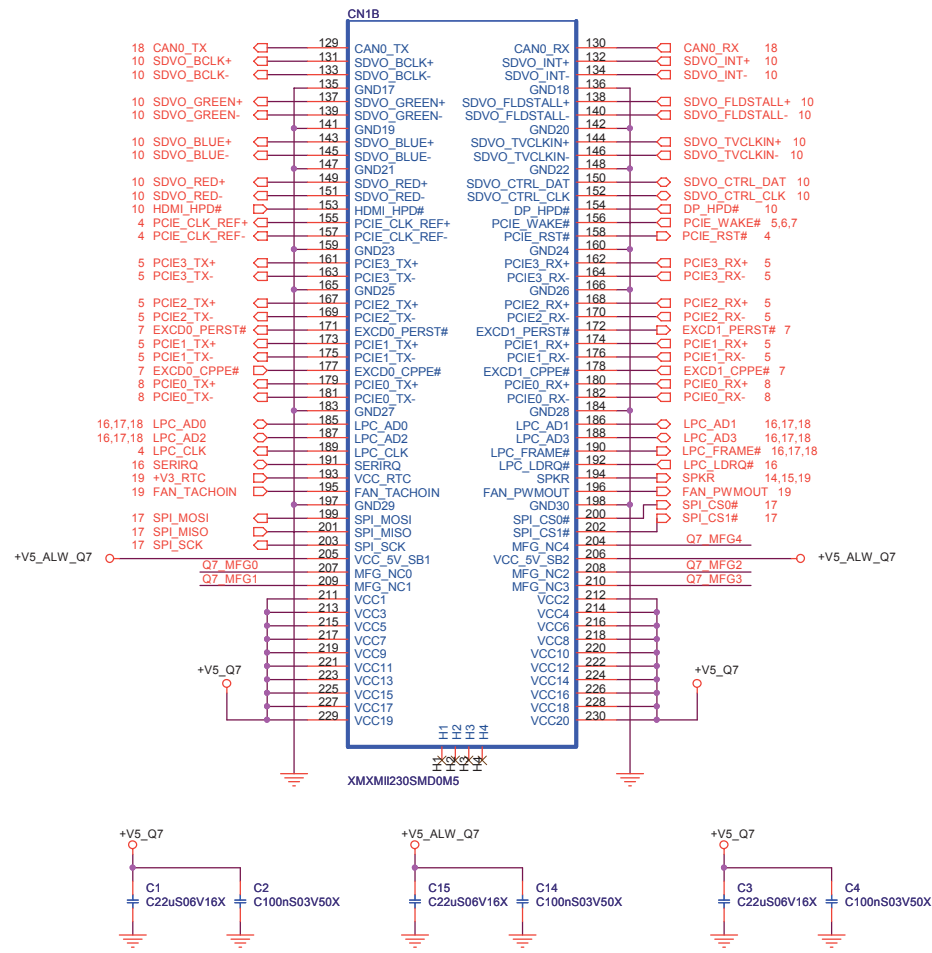
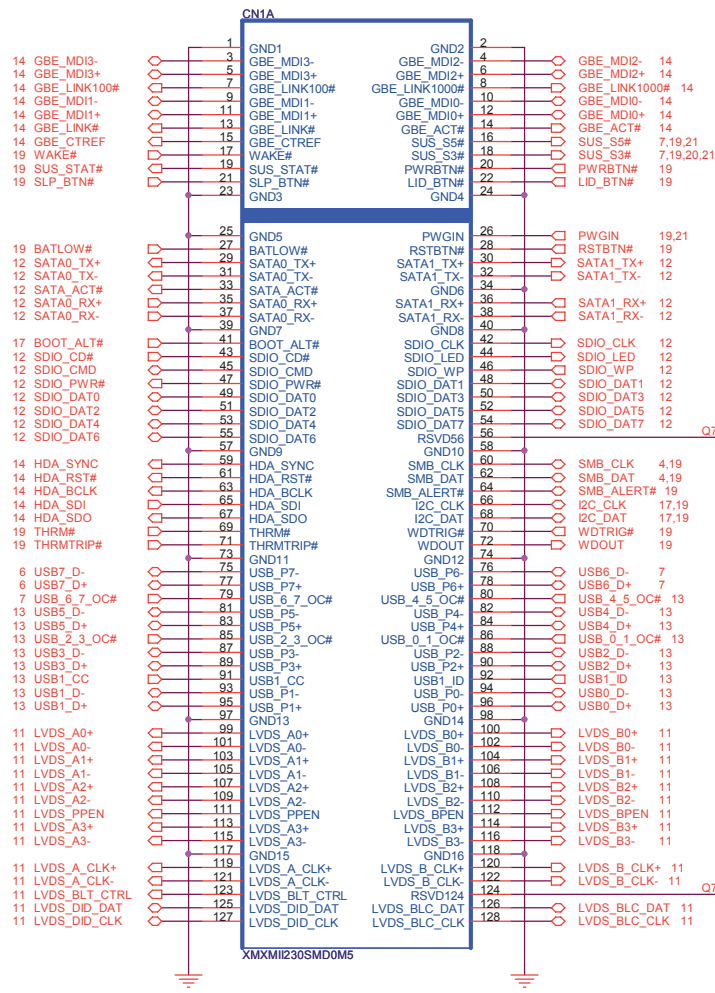
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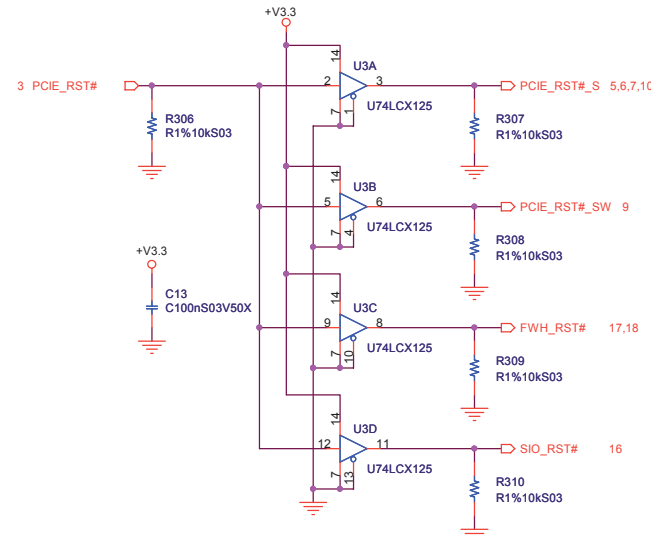
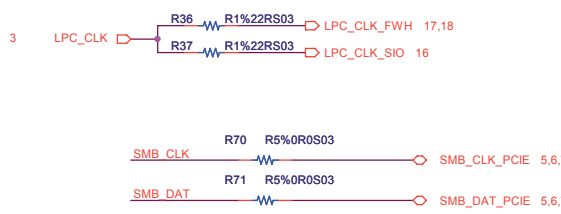
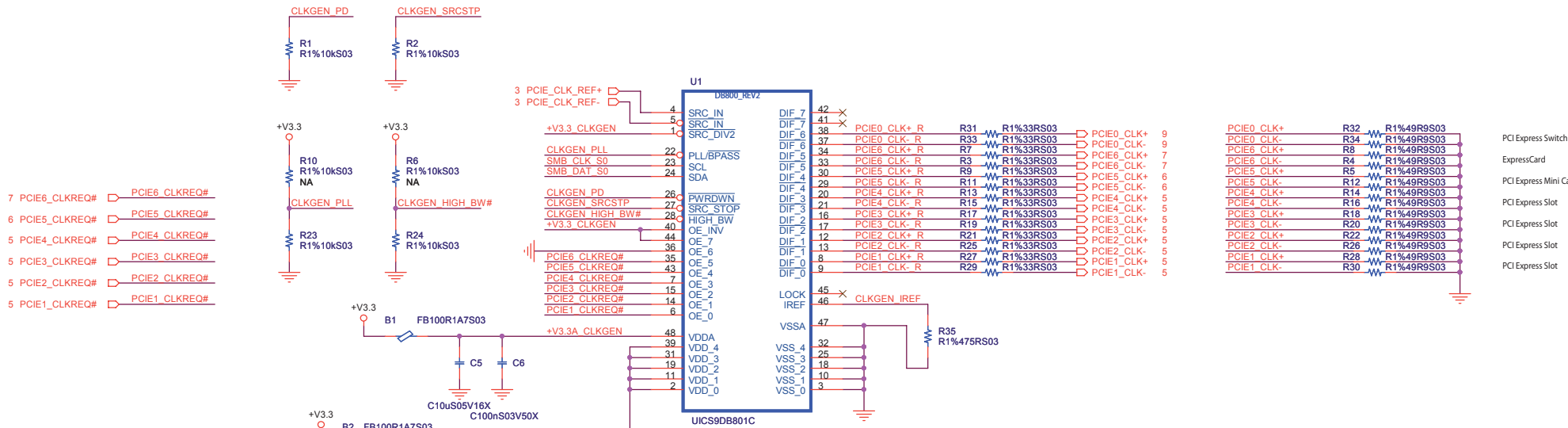
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Title QEVA - Qseven Evaluation Backplane			
Size A3	Document Number QEVASB0	Created	Rev B.0
Date: Monday, February 21, 2011	Sheet 1	of 22	



Title				
Block Diagram				
Size	Document Number	Created	Rev	
A3	QEVASB0		B.0	
Date:	Friday, February 18, 2011	Sheet	2	of 22



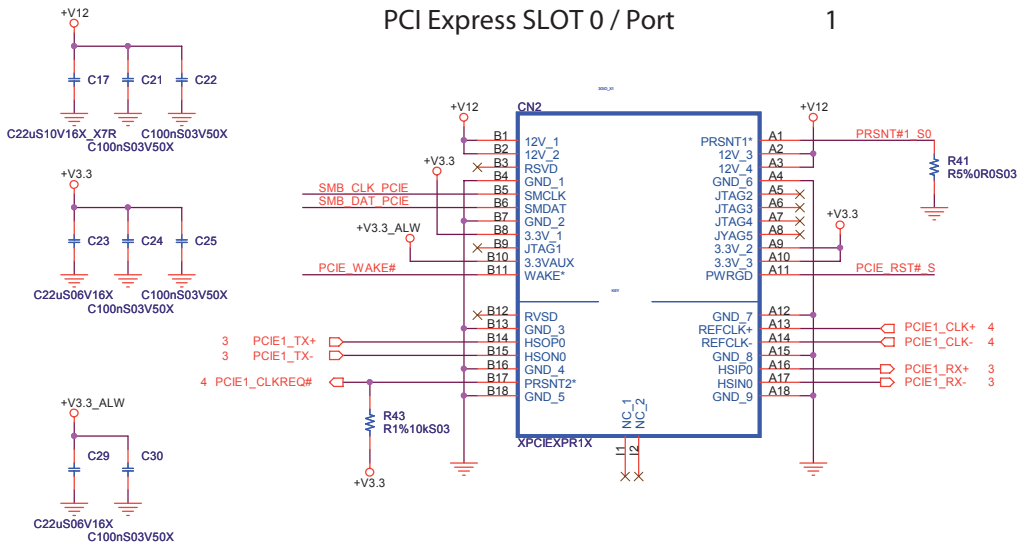
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Qseven connector			
Size	Document Number	Created	Rev
A3	QEVASB0		B.0
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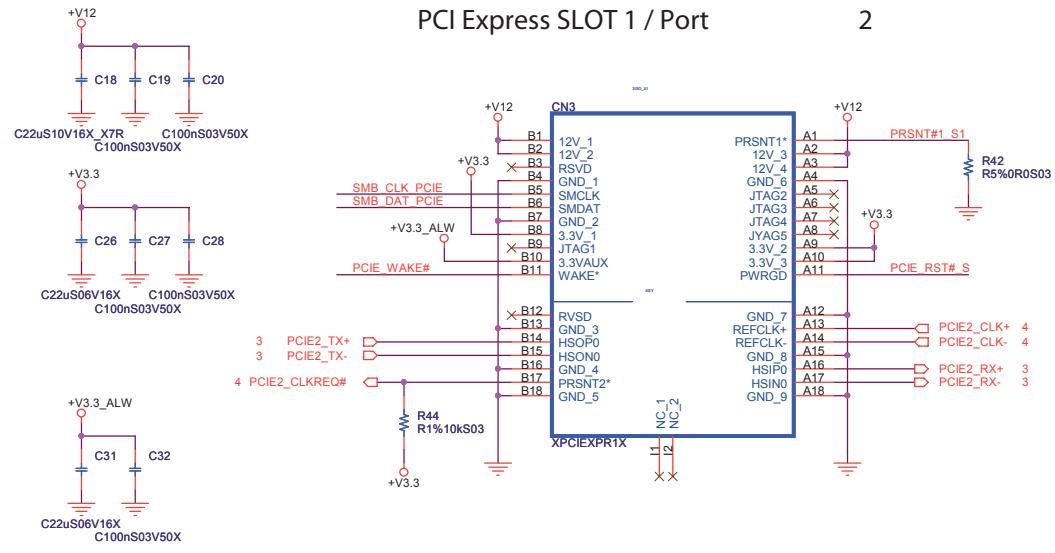
Title			
PCle Clock / Misc.			
Size	Document Number	Created	Rev
A3	QEVASB0		B.0
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4,6,7 SMB_CLK_PCIE ○ SMB_CLK_PCIE
 4,6,7 SMB_DAT_PCIE ○ SMB_DAT_PCIE
 3,6,7 PCIE_WAKE# □ PCIE_WAKE#
 4,6,7,10 PCIE_RST#_S □ PCIE_RST#_S

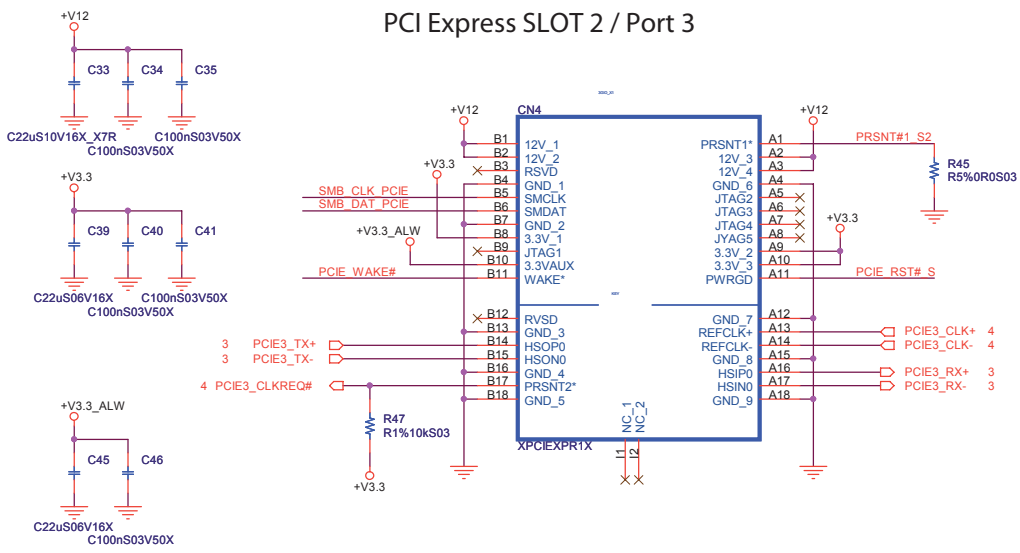
PCI Express SLOT 0 / Port 1



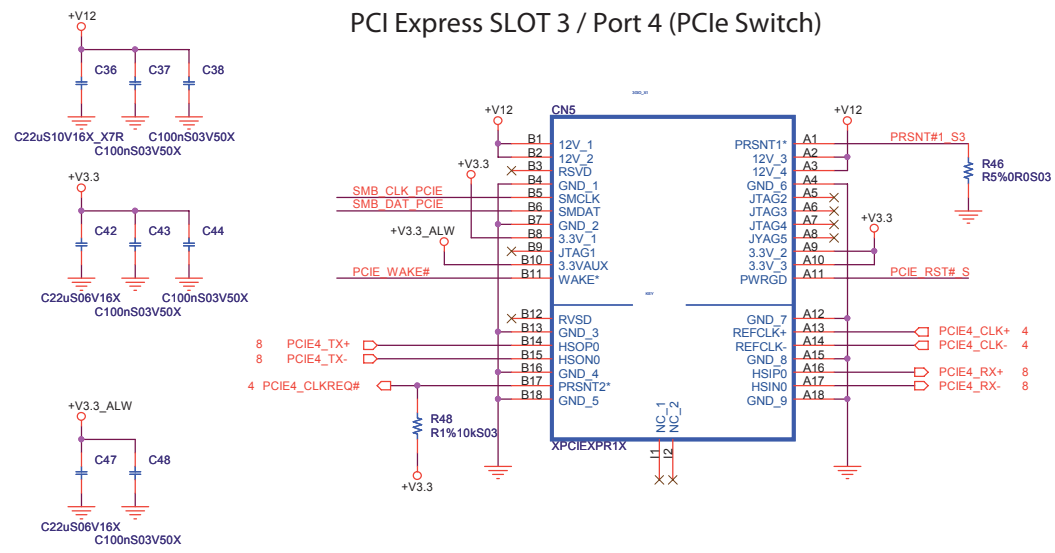
PCI Express SLOT 1 / Port 2



PCI Express SLOT 2 / Port 3



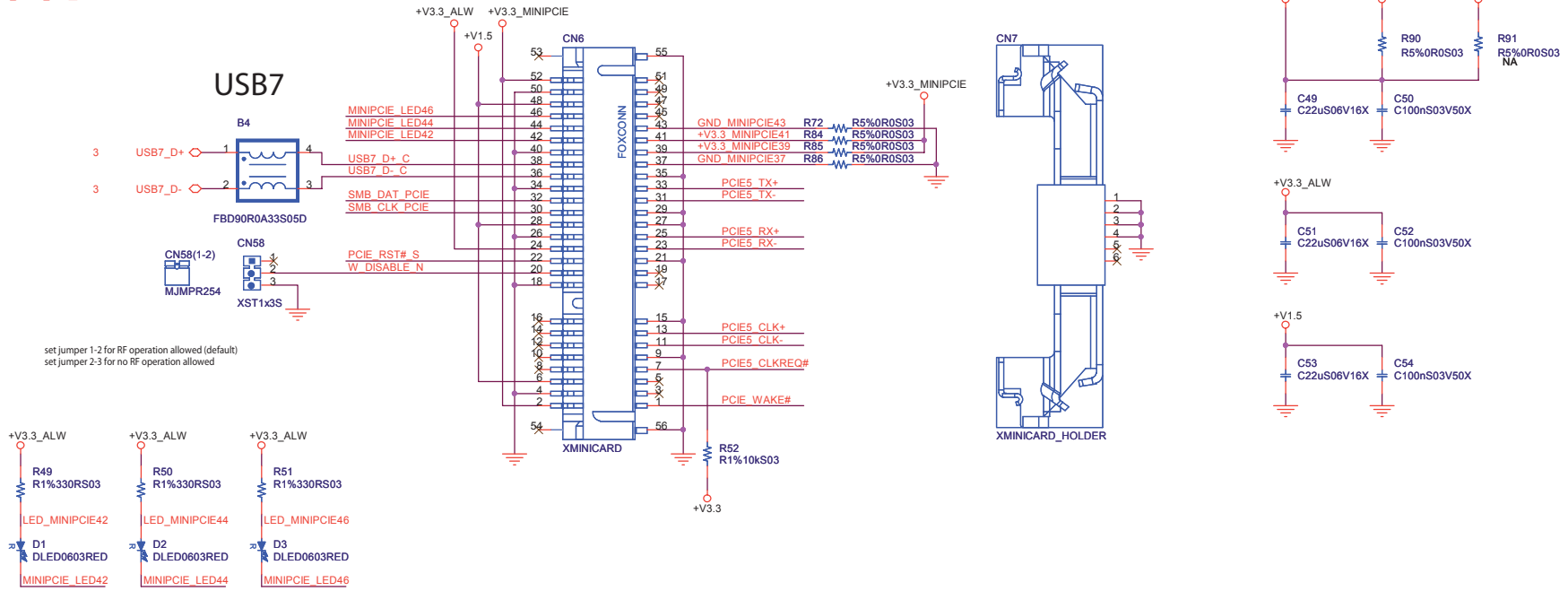
PCI Express SLOT 3 / Port 4 (PCIe Switch)



Title				
PCIe x1 Slots				
Size	Document Number	Created	Rev	
A3	QEVASB0		B.0	
Date:	Friday, February 18, 2011	Sheet	5	of 22

- 8 PCIE5_TX+ > PCIE5_TX+
- 8 PCIE5_TX- > PCIE5_TX-
- 8 PCIE5_RX+ > PCIE5_RX+
- 8 PCIE5_RX- > PCIE5_RX-
- 4 PCIE5_CLK+ > PCIE5_CLK+
- 4 PCIE5_CLK- > PCIE5_CLK-
- 4 PCIE5_CLKREQ# > PCIE5_CLKREQ#
- 4,5,7 SMB_CLK_PCIE > SMB_CLK_PCIE
- 4,5,7 SMB_DAT_PCIE > SMB_DAT_PCIE
- 3,5,7 PCIE_WAKE# > PCIE_WAKE#
- 4,5,7,10 PCIE_RST#_S > PCIE_RST#_S

PCI Express Mini Card / Port 5 (PCIe Switch)

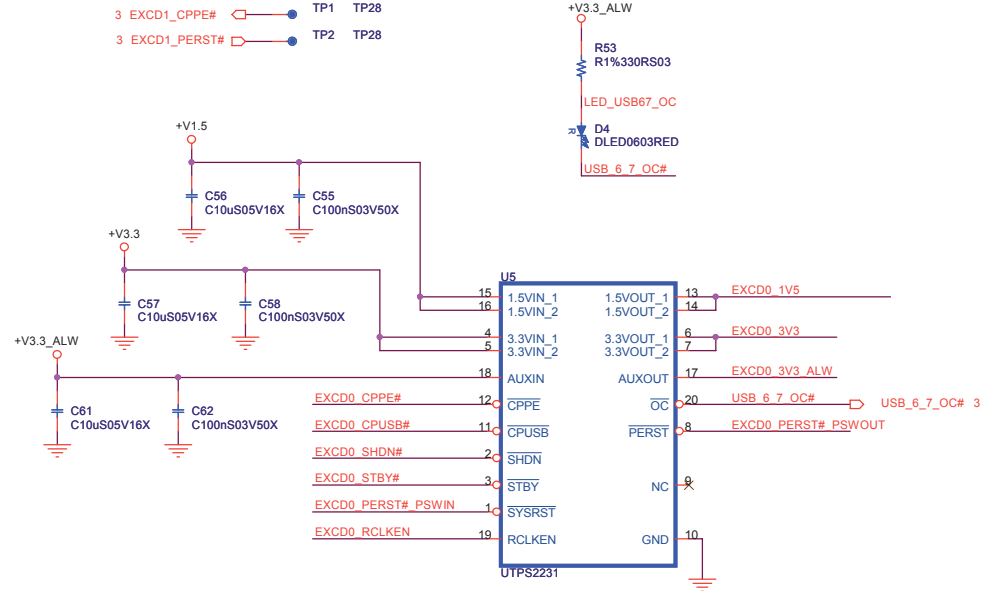


set jumper 1-2 for RF operation allowed (default)
set jumper 2-3 for no RF operation allowed

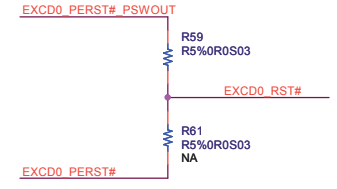
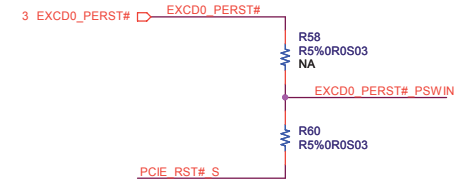
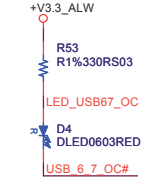
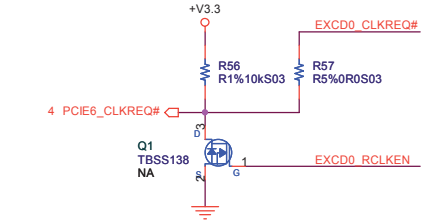
Title			
PCIe Mini Card			
Size	Document Number	Created	Rev
A3	QEVASB0		B.0
Date:	Friday, February 18, 2011	Sheet	6 of 22

4,5,6 SMB_CLK_PCIE ◯ SMB_CLK_PCIE
 4,5,6 SMB_DAT_PCIE ◯ SMB_DAT_PCIE
 3,5,6 PCIE_WAKE# ◯ PCIE_WAKE#
 4,5,6,10 PCIE_RST#_S ◯ PCIE_RST#_S

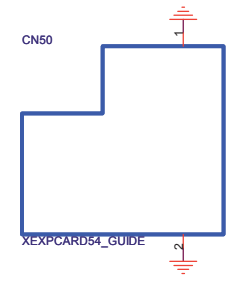
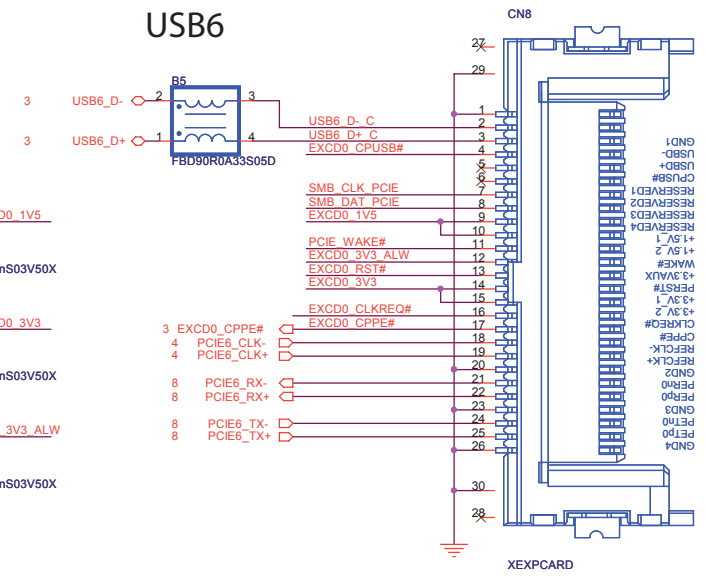
3 EXCD1_CPPE# ◯ TP1 TP28
 3 EXCD1_PERST# ◯ TP2 TP28



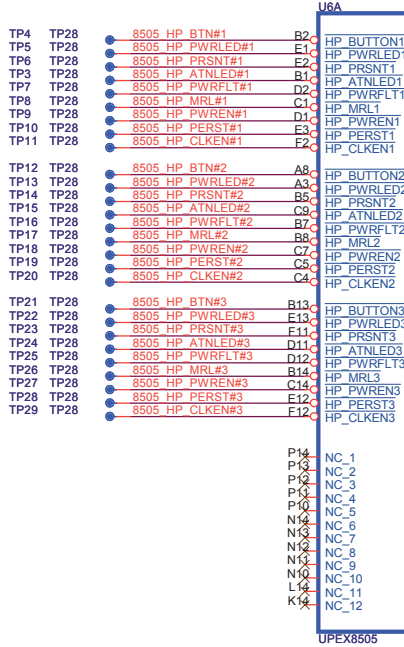
3,19,21 SUS_S5# ◯ R54 R5%0R0S03 EXCD0_SHDN#
 3,19,20,21 SUS_S3# ◯ R55 R5%0R0S03 EXCD0_STBY#



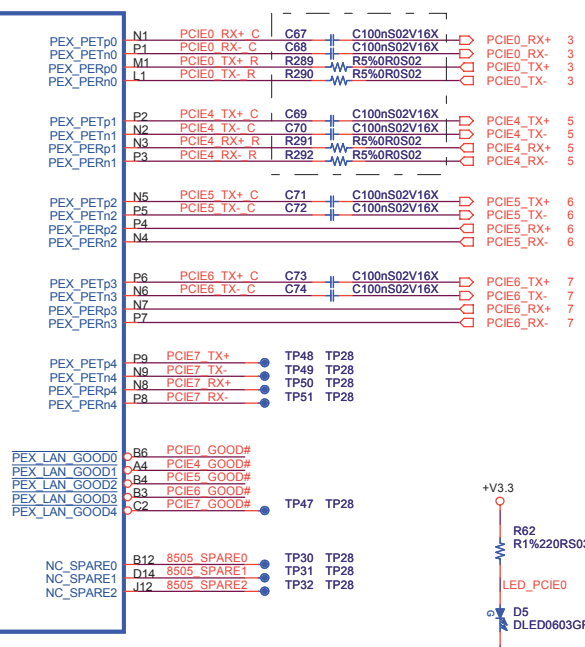
ExpressCard / Port 6 (PCIe Switch)



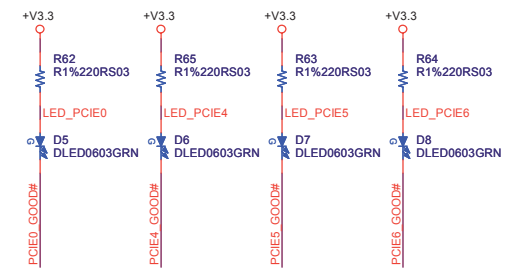
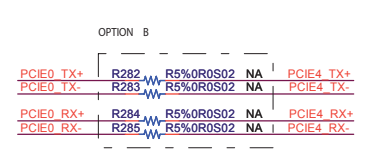
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ExpressCard				
Size	Document Number	Created	Rev	
A3	QEVASB0		B.0	
Date:	Friday, February 18, 2011	Sheet	7	of 22



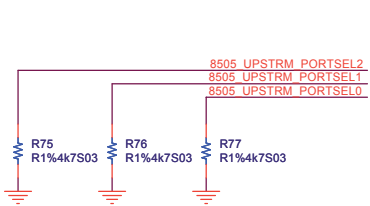
**PEX8505-AA25BIG
PBGA 196**



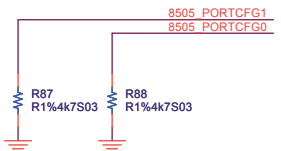
Optional Qseven PCIe0 port / PCIe SLOT 4 connection:
 OPTION A: Qseven PCIe0 port connected to PCIe SWITCH
 PCIe SLOT 4 connected to PCIe SWITCH
 OPTION B: Qseven PCIe0 port connected to PCIe SLOT



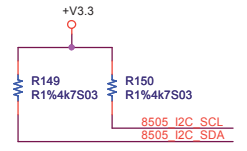
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PCIe Switch			
Size	Document Number	Created	Rev
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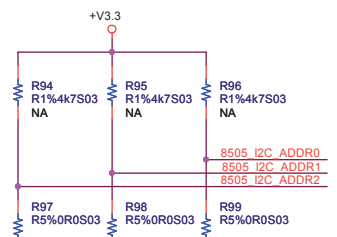
UP STREAM PORT= PORT0 = LLL



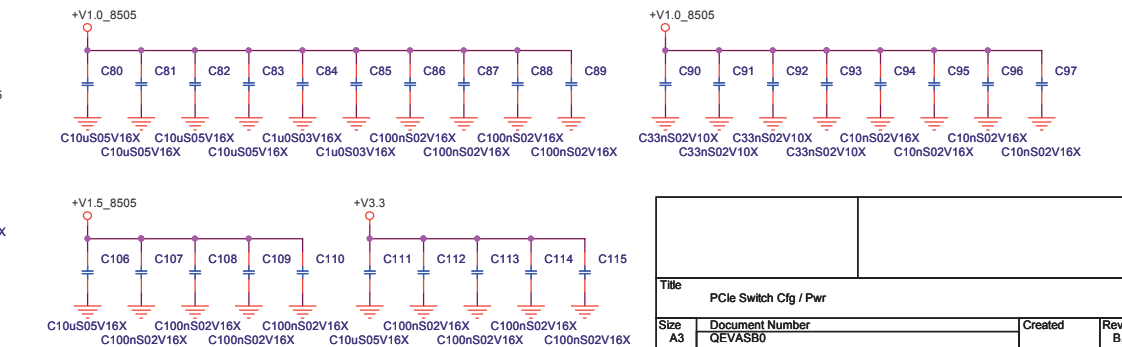
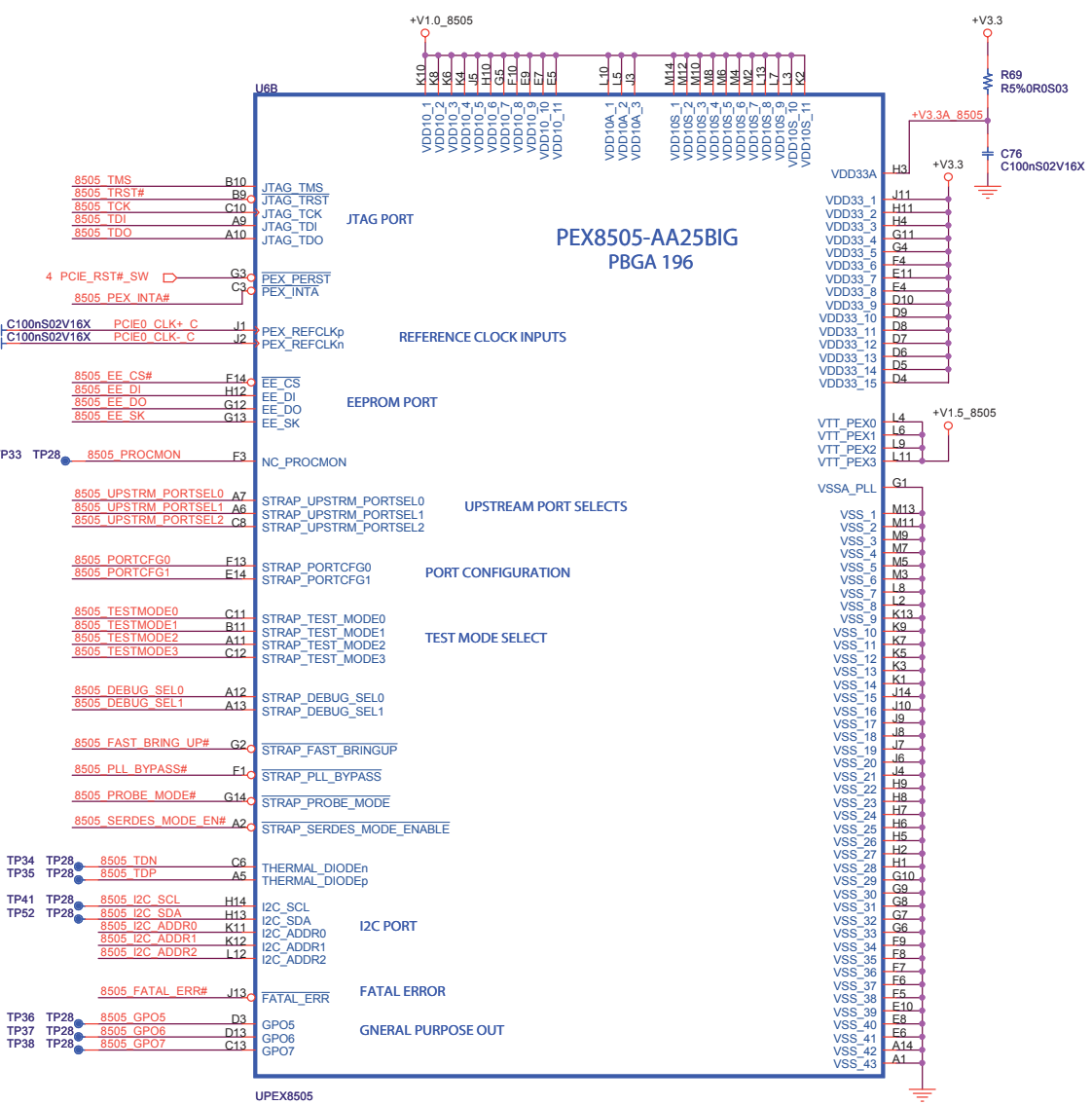
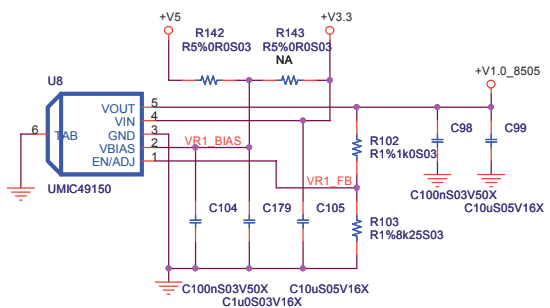
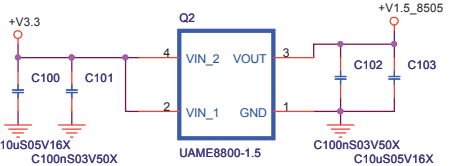
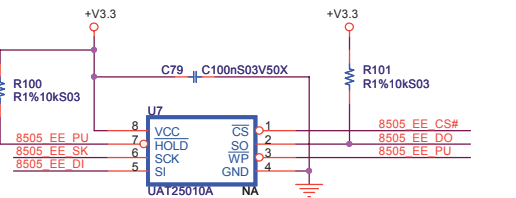
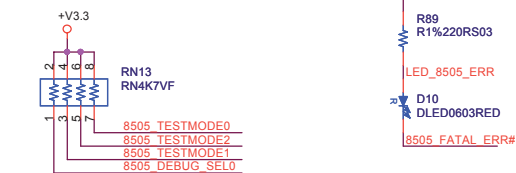
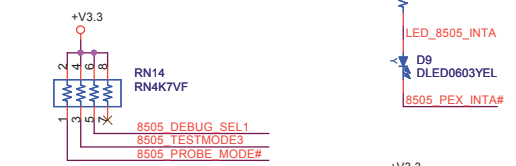
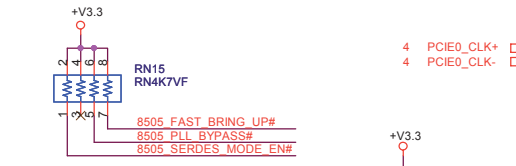
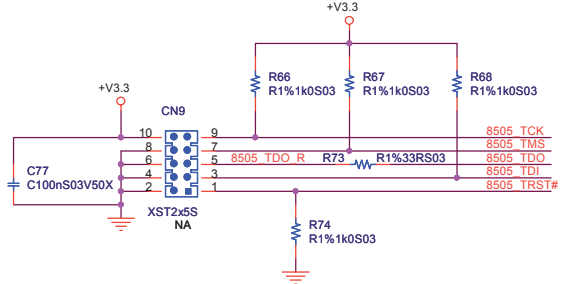
Port Configuration for Station 0 = x1,x1,x1,x1



I2C ADDRESS = 0x70

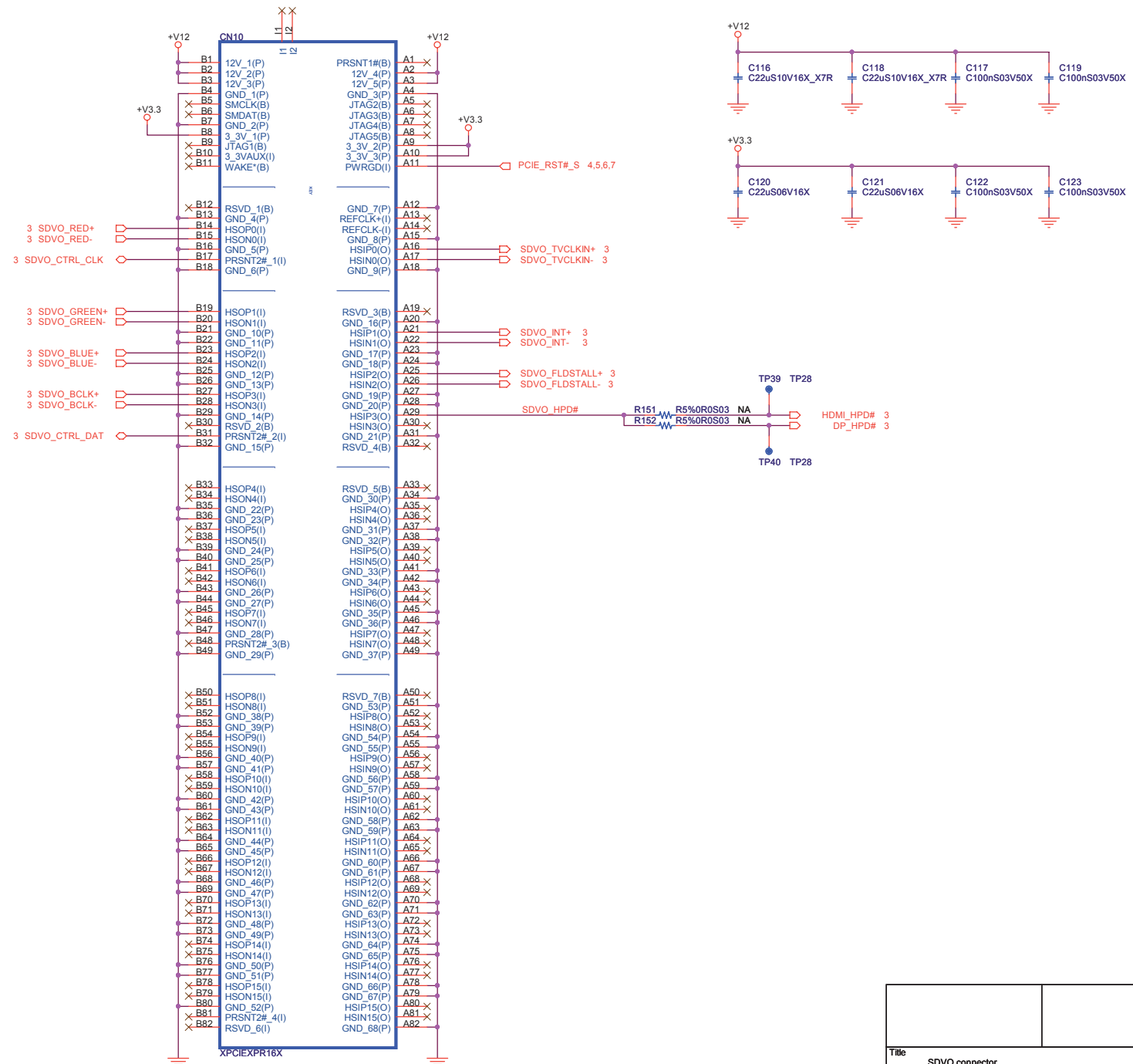


I2C ADDRESS = 0x70

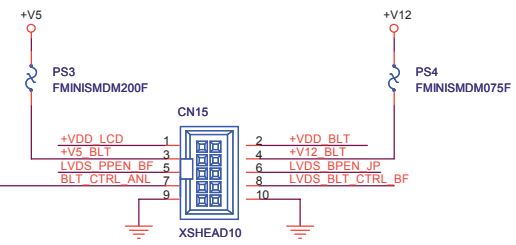
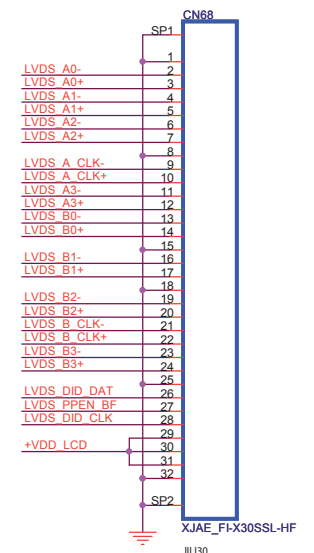
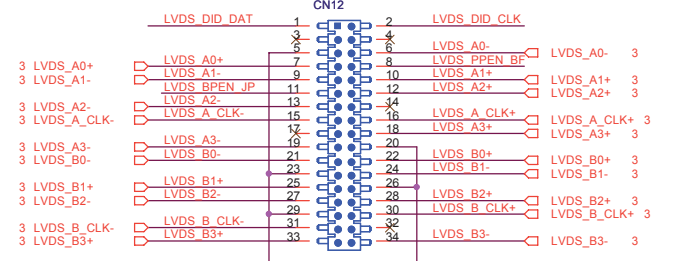
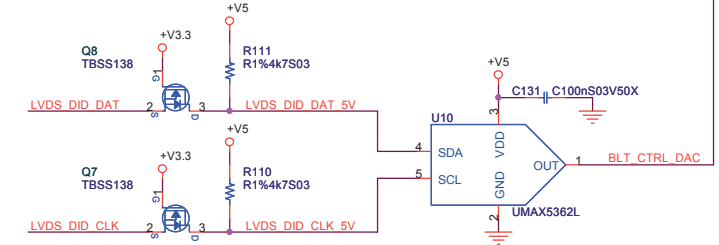
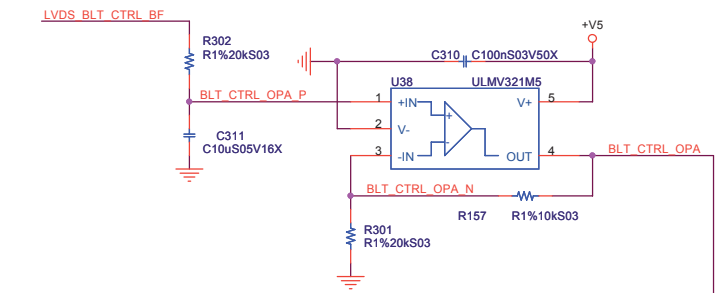
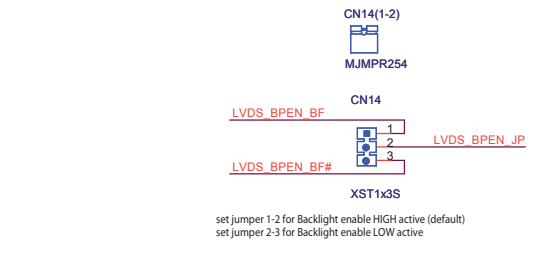
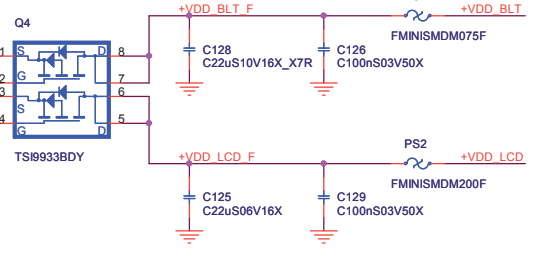
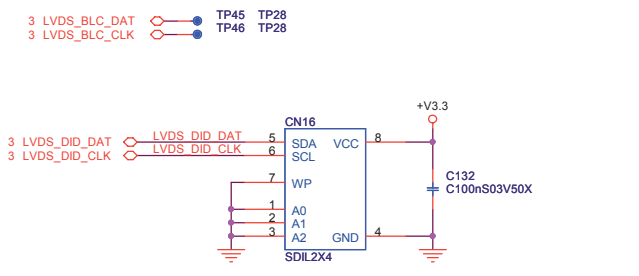
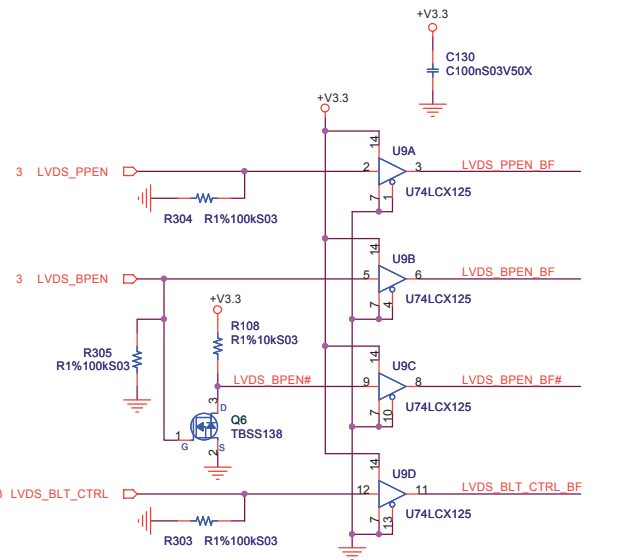
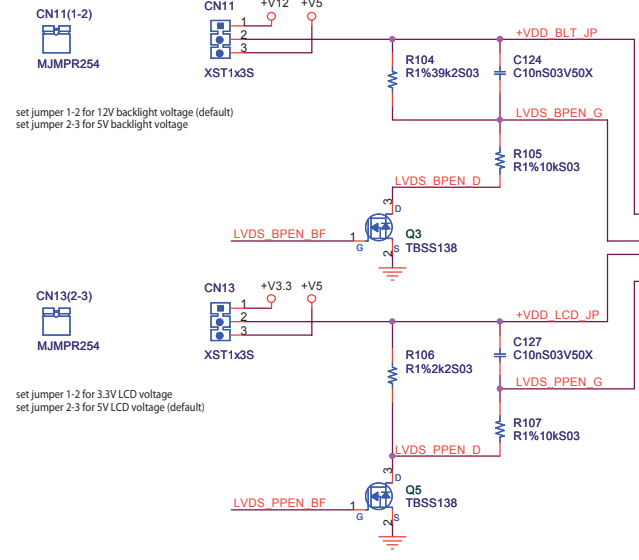


Title			
PCIe Switch Cfg / Pwr			
Size A3	Document Number QEVASB0	Created	Rev B.0
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NOTE: Supports only ADD2-N cards in this slot. ADD2-R cards are not supported.

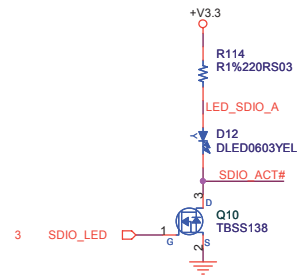
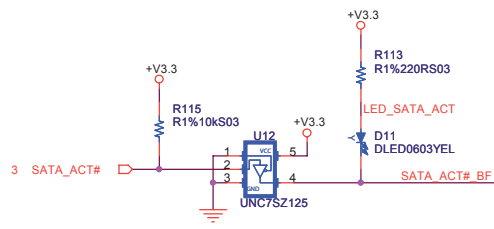
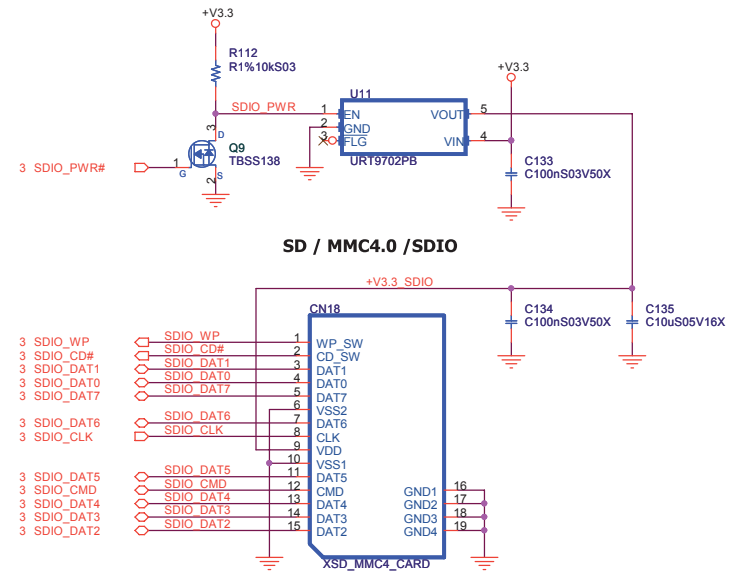
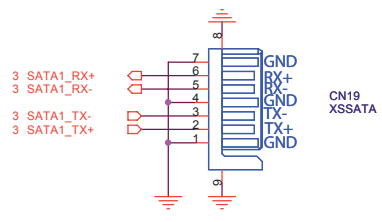
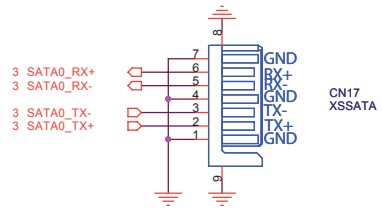


Title			
SDVO connector			
Size	Document Number	Created	Rev
A3	QEVASB0		B.0
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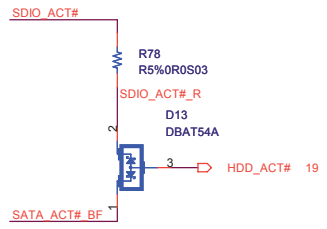


set jumper 1-2 for Backlight control by PWM to ANALOG
set jumper 2-3 for Backlight control by I2C DAC (default)

Title				
LCD LVDS connector				
Size	Document Number	Created	Rev	
A3	QEVASB0		B.0	
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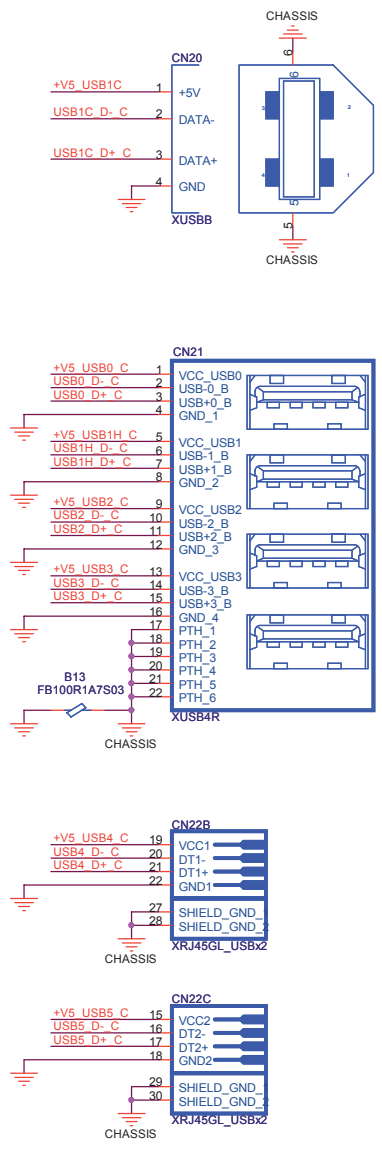
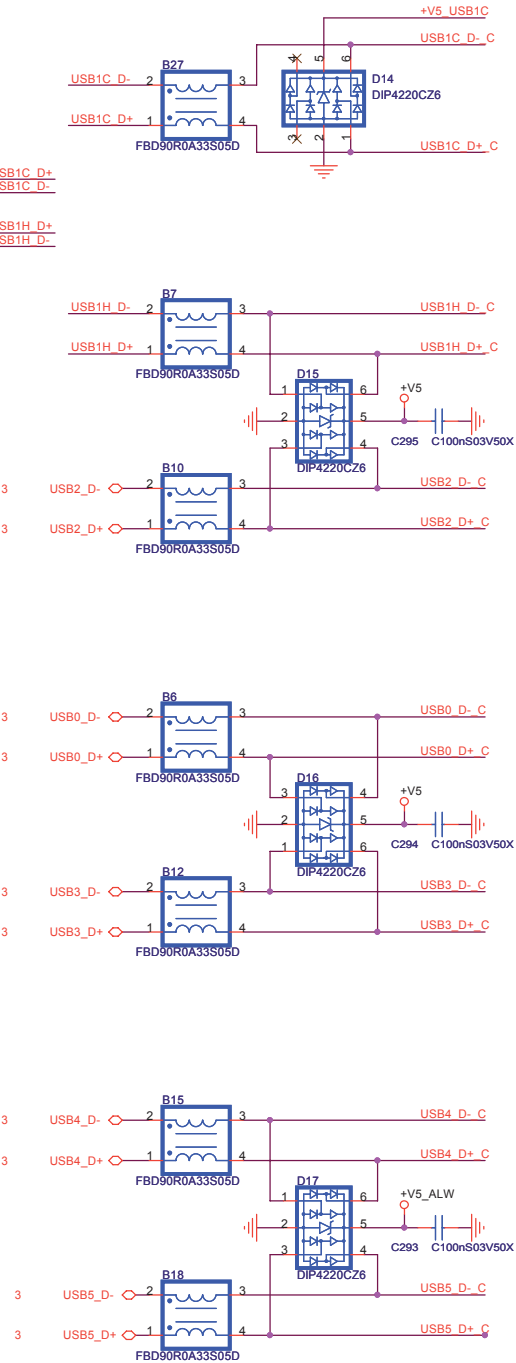
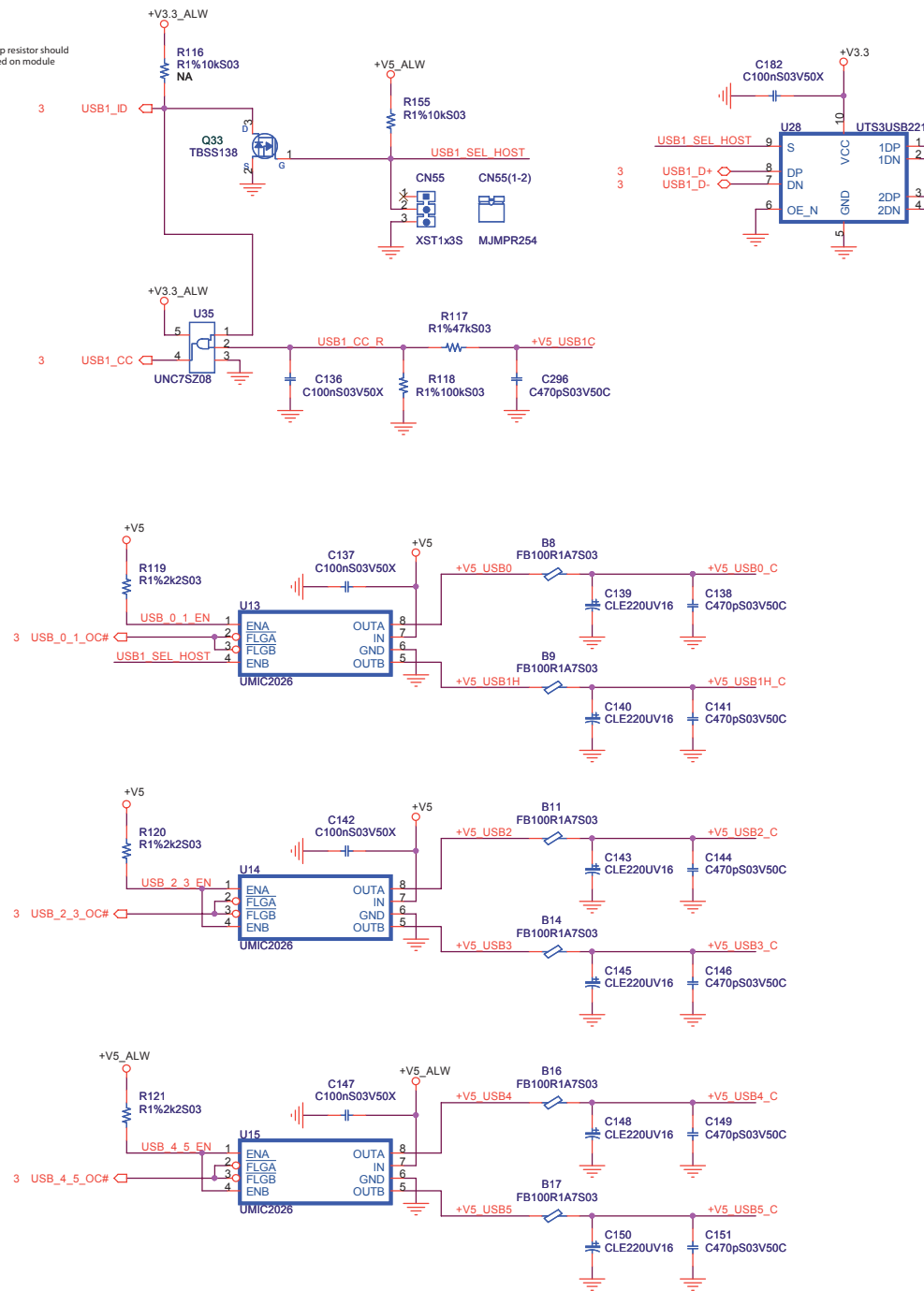
NOTE: remove R78 if SDIO card present is indicated by SDIO LED turned ON



Title			
SATA / SDIO connectors			
Size	Document Number	Created	Rev
A3	QEVASB0		B.0
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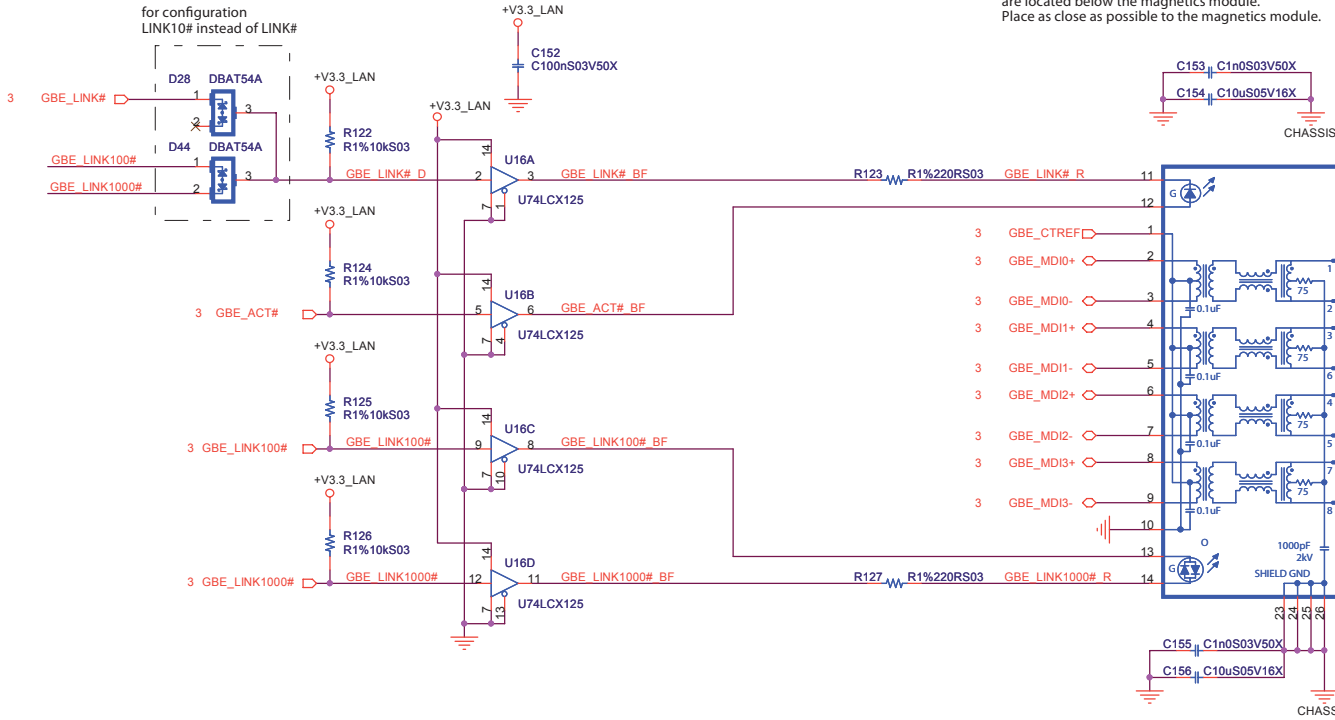
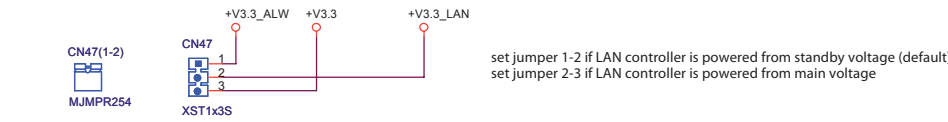
set jumper 1-2 for USB1 as Host USB Port (default)
set jumper 2-3 for USB1 as Client USB Port

Note: pull-up resistor should be integrated on module



Title				
USB connectors				
Size	Document Number	Created	Rev	
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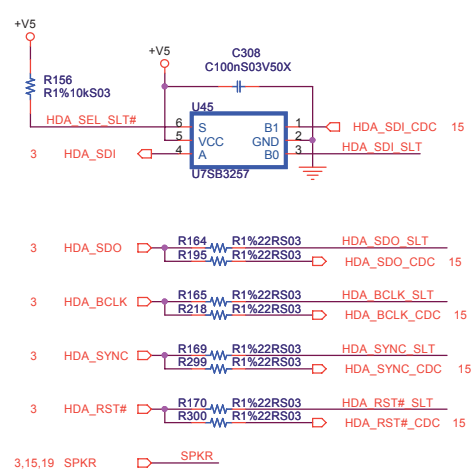
GIGABIT ETHERNET



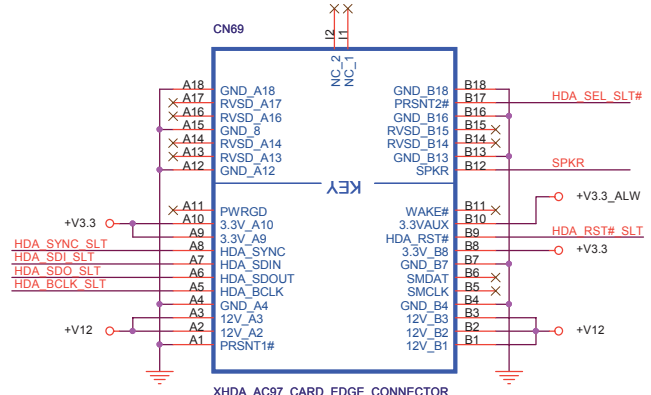
These capacitors across the CHASSIS to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.

LED State	Description
Off	No Link
Steady On	Link established, no activity detected
Blinking	Link established, activity detected

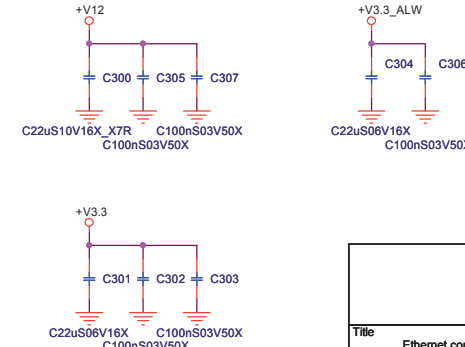
LED State	Description
Off	10 Mbps link speed
Green	100 Mbps link speed
Orange	1000 Mbps link speed



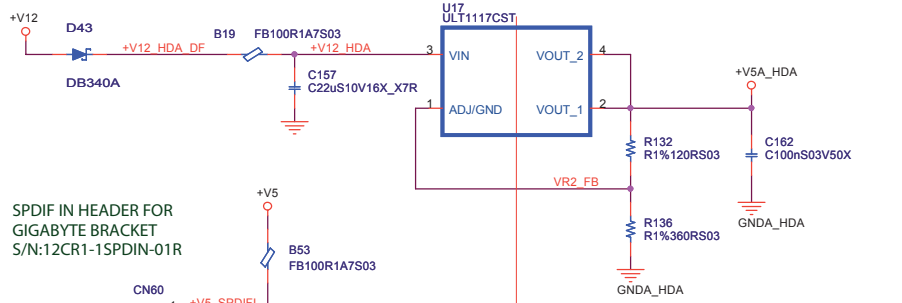
PLACE NEXT TO PCIE4 CONNECTOR
 BACK PANEL SIDE



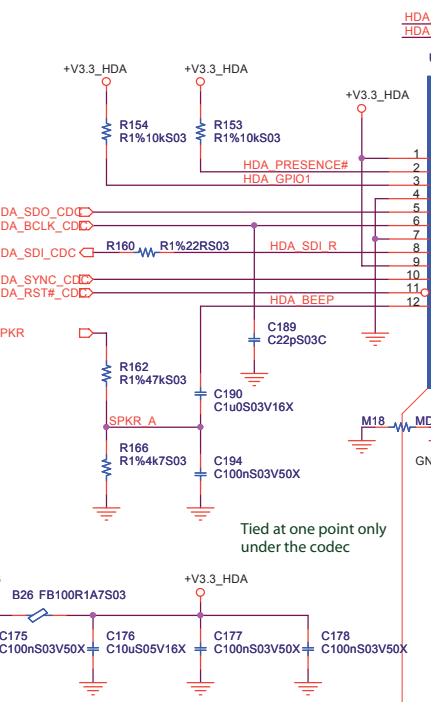
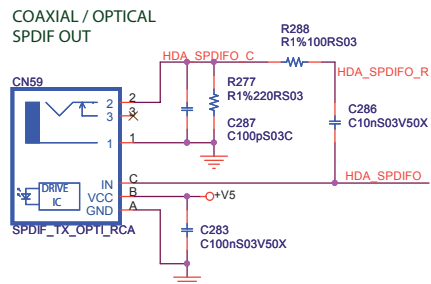
HDA/AC97 CARD EDGE CONNECTOR



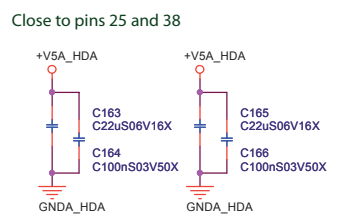
Title			
Ethernet connector / HDA/AC97 CARD EDGE CONNECTOR			
Size	Document Number	Created	Rev
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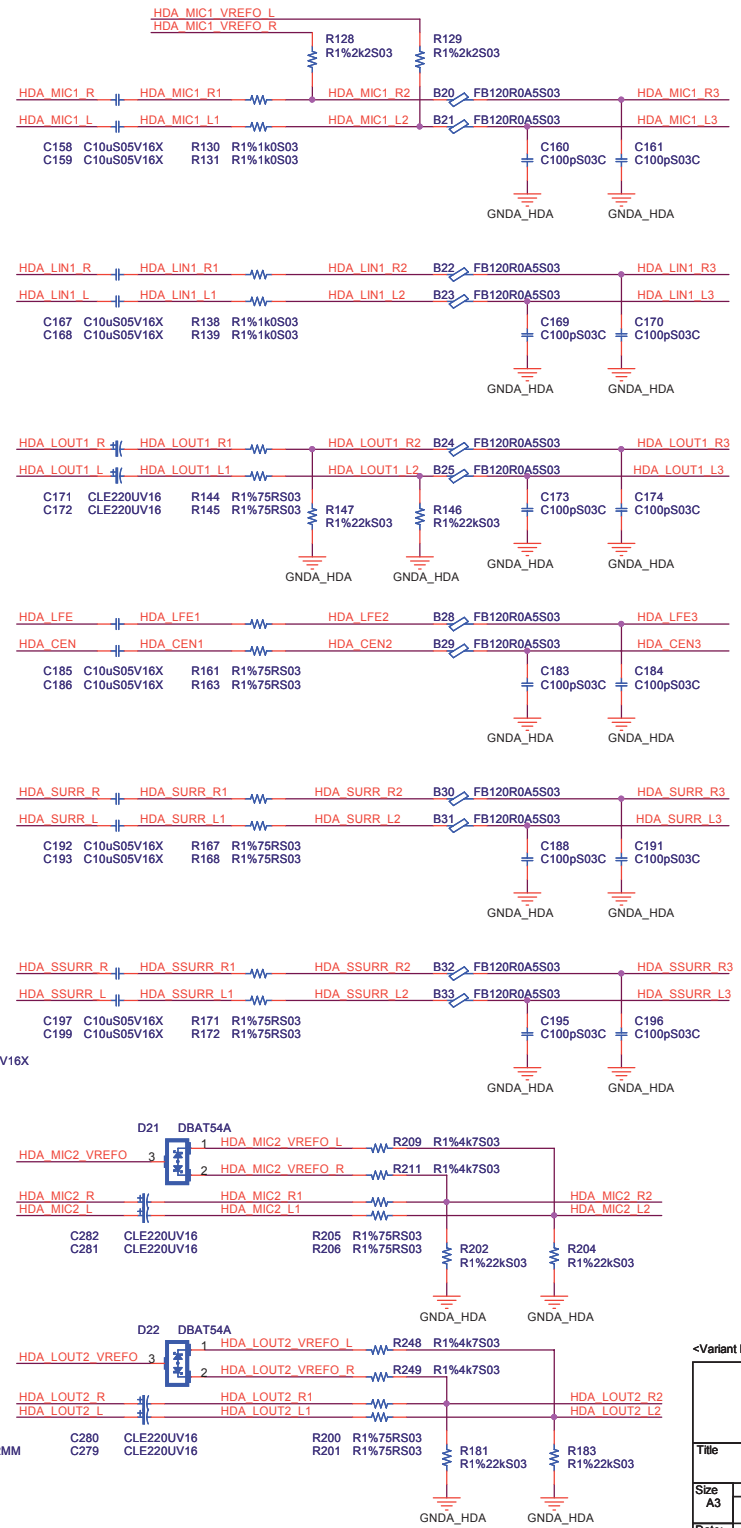
SPDIF IN HEADER FOR GIGABYTE BRACKET
S/N:12CR1-1SPDIN-01R



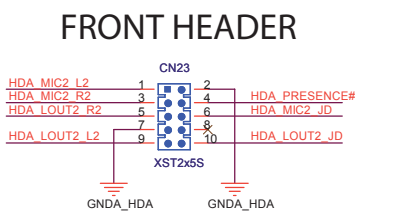
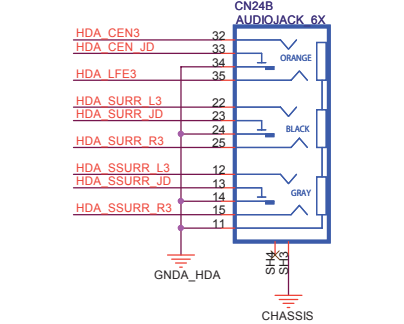
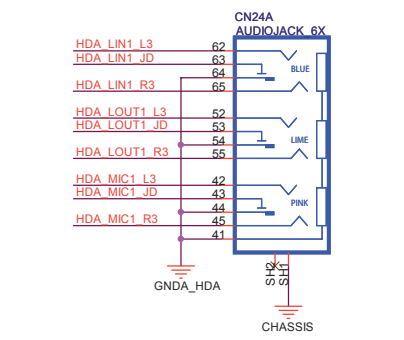
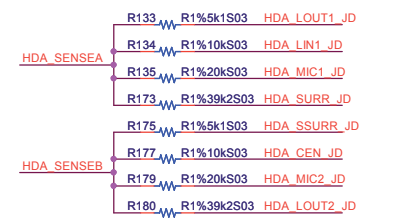
Tied at one point only under the codec



Close to pins 25 and 38

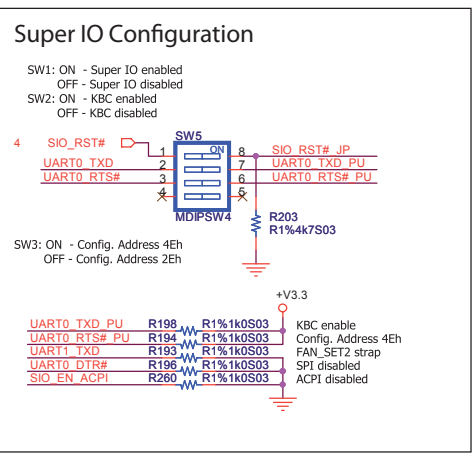
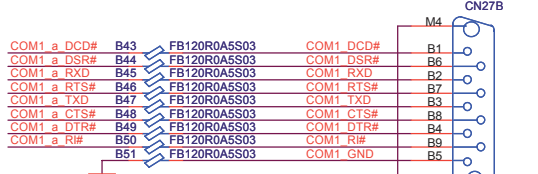
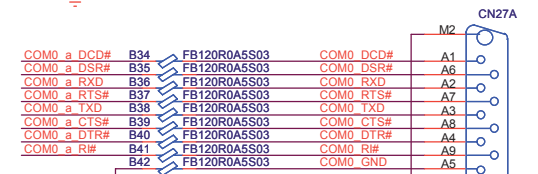
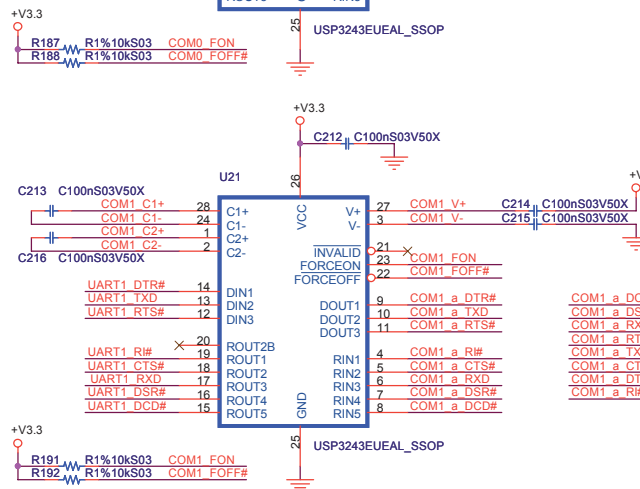
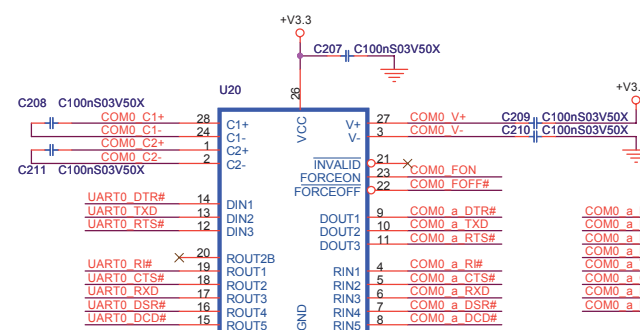
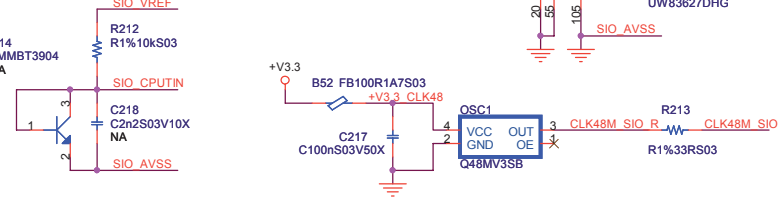
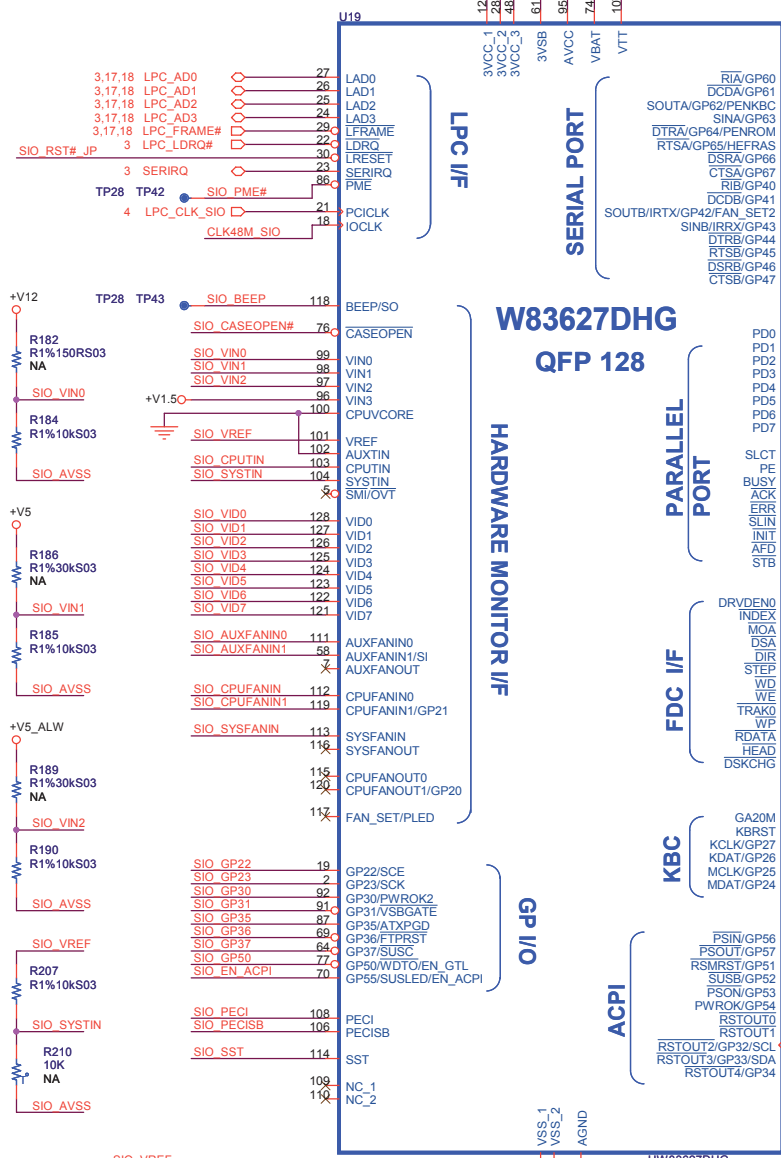
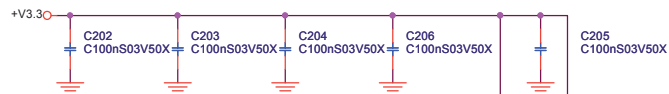


NOTE1. In order to avoid incorrect of JD recognition, all of JD resistors should be placed as close as possible to the sense pin of codec.



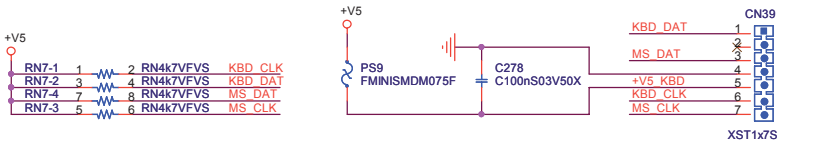
<Variant Name>

Title				
HD Audio				
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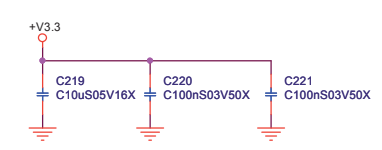
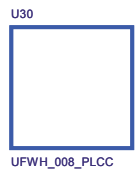
Note: prevent input pins floating

SIO CPUFANIN	RN8-1	2	1	RN4k7VFS	LPT PD3	RN1-1	2	1	RN4k7VFS
SIO SYSFANIN	RN8-2	4	3	RN4k7VFS	LPT PD2	RN1-2	4	3	RN4k7VFS
SIO AUXFANIN0	RN18-4	8	7	RN4k7VFS	LPT PD1	RN1-3	6	5	RN4k7VFS
SIO AUXFANIN1	RN5-2	4	3	RN4k7VFS	LPT PD0	RN1-4	8	7	RN4k7VFS
SIO CPUFANIN1	RN8-4	8	7	RN4k7VFS	LPT PD7	RN2-1	2	1	RN4k7VFS
SIO GP22	RN9-4	8	7	RN4k7VFS	LPT PD6	RN2-2	4	3	RN4k7VFS
SIO GP23	RN9-2	4	3	RN4k7VFS	LPT PD5	RN2-3	6	5	RN4k7VFS
SIO SUSB#	RN11-3	6	5	RN4k7VFS	LPT PD4	RN2-4	8	7	RN4k7VFS
SIO GP35	RN10-2	4	3	RN4k7VFS	LPT SLCT	RN3-1	2	1	RN4k7VFS
SIO GP31	RN10-3	6	5	RN4k7VFS	LPT PE	RN3-2	4	3	RN4k7VFS
SIO GP30	RN10-4	8	7	RN4k7VFS	LPT BUSY	RN3-3	6	5	RN4k7VFS
SIO GP37	RN11-1	2	1	RN4k7VFS	LPT ACK#	RN3-4	8	7	RN4k7VFS
SIO GP36	RN11-2	4	3	RN4k7VFS	LPT SLIN#	RN4-1	2	1	RN4k7VFS
SIO CASEOPEN#	RN11-4	2	1	RN4k7VFS	LPT INT#	RN2-2	4	3	RN4k7VFS
SIO GP50	RN10-1	2	1	RN4k7VFS	LPT ERR#	RN4-3	6	5	RN4k7VFS
SIO GP22	RN5-4	8	7	RN4k7VFS	LPT AFD#	RN4-4	8	7	RN4k7VFS
SIO VID0	RN16-4	8	7	RN4k7VFS	LPT STB#	RN5-1	2	1	RN4k7VFS
SIO VID1	RN16-3	6	5	RN4k7VFS		RN9-1	2	1	RN4k7VFS
SIO VID2	RN16-2	4	3	RN4k7VFS	FDC INDEX#	RN5-3	6	5	RN4k7VFS
SIO VID3	RN16-1	2	1	RN4k7VFS	FDC TRAKO#	RN5-6	5	4	RN4k7VFS
SIO VID4	RN17-4	8	7	RN4k7VFS	FDC WP#	RN6-1	2	1	RN4k7VFS
SIO VID5	RN17-3	6	5	RN4k7VFS	FDC RDATA#	RN6-2	4	3	RN4k7VFS
SIO VID6	RN17-2	4	3	RN4k7VFS	FDC RDAT#	RN6-3	6	5	RN4k7VFS
SIO VID7	RN17-1	2	1	RN4k7VFS	FDC DSKCHG#	RN6-4	8	7	RN4k7VFS
SIO PECISB	RN18-1	2	1	RN4k7VFS					
SIO PECl	RN18-3	6	5	RN4k7VFS					
SIO VTT	RN18-2	4	3	RN4k7VFS					
SIO SST	RN8-3	6	5	RN4k7VFS					



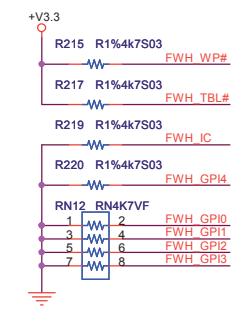
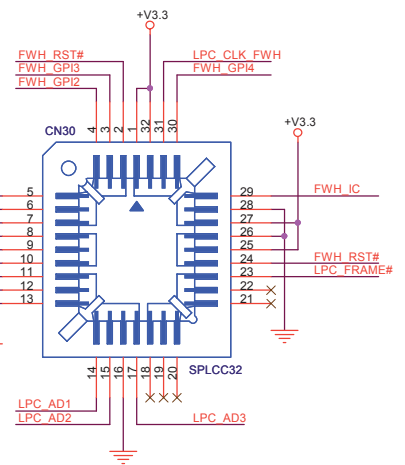
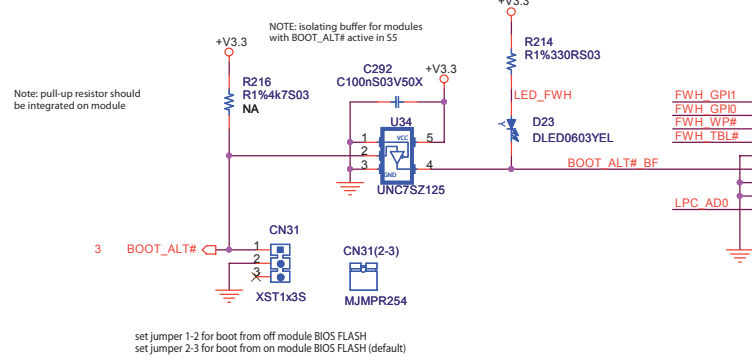
Title		COM ports	
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- 4,18 LPC_CLK_FWH# → LPC_CLK_FWH
- 4,18 FWH_RST# → FWH_RST#
- 3,16,18 LPC_FRAME# → LPC_FRAME#
- 3,16,18 LPC_AD3 → LPC_AD3
- 3,16,18 LPC_AD2 → LPC_AD2
- 3,16,18 LPC_AD1 → LPC_AD1
- 3,16,18 LPC_AD0 → LPC_AD0

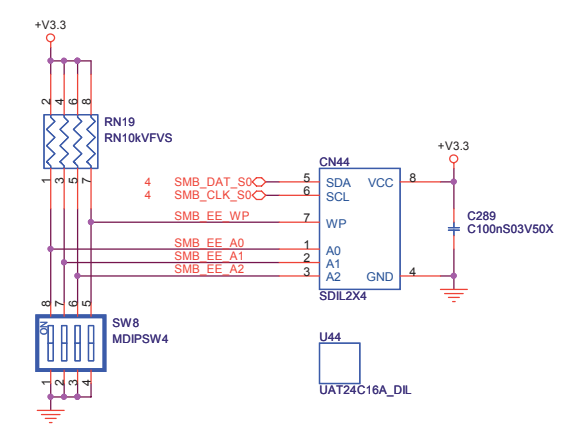


Firmware Hub

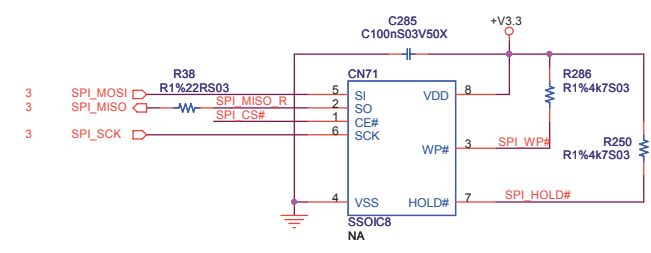
off module BOOT FLASH LED



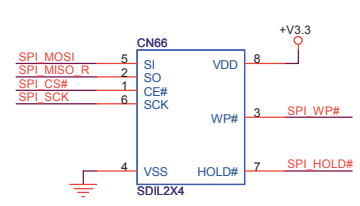
SMBus Eeprom



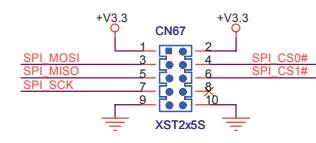
SPI SOIC8W



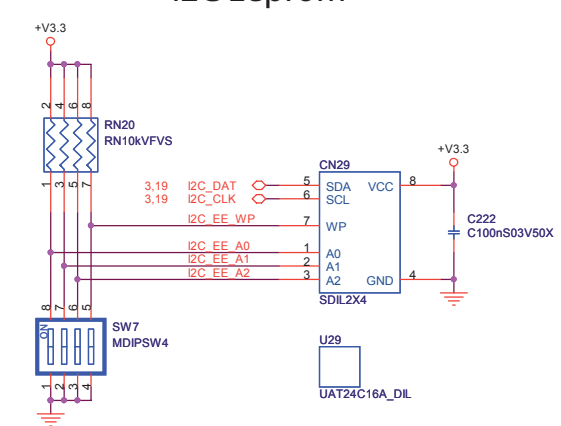
SPI DIP8 SOCKET



SPI HEADER

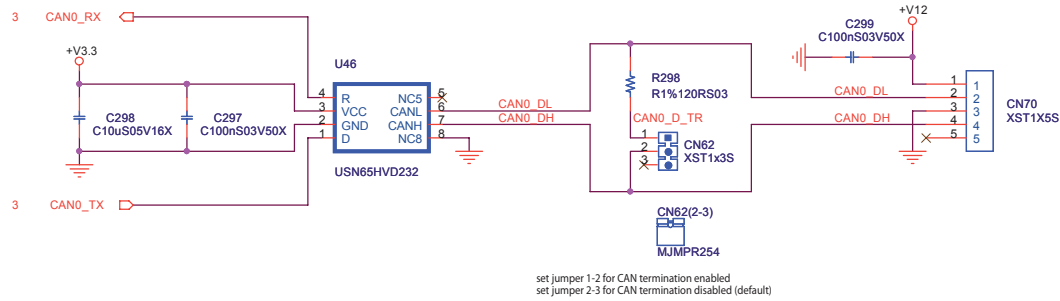


I2C Eeprom



Title			
LPC FWH / SPI / I2C EEPROM / SMB EEPROM			
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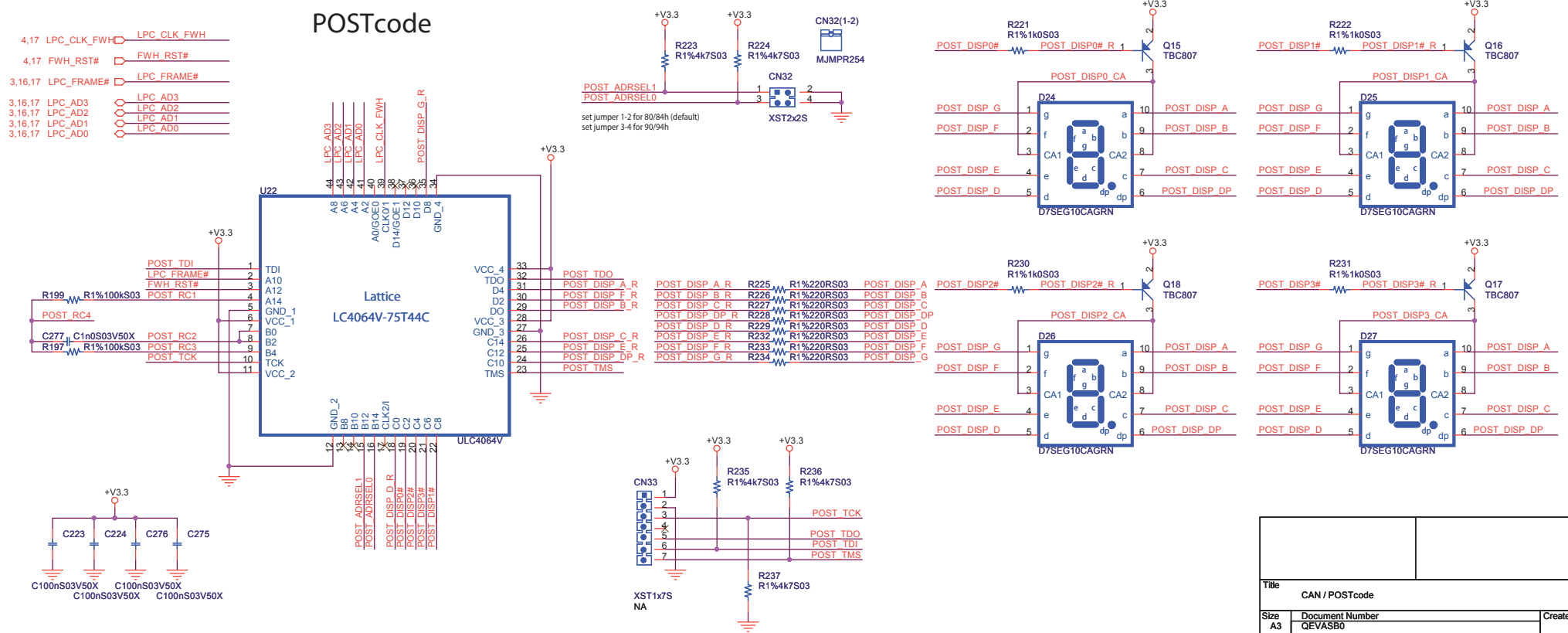
CAN TRANSCEIVER



set jumper 1-2 for CAN termination enabled
set jumper 2-3 for CAN termination disabled (default)

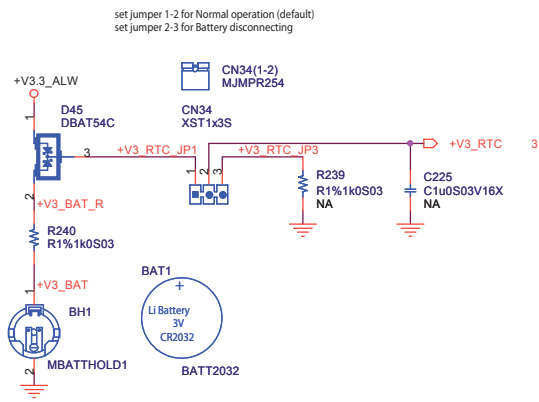
POSTcode

- 4.17 LPC_CLK_FWH# → LPC_CLK_FWH
- 4.17 FWH_RST# → FWH_RST#
- 3.16.17 LPC_FRAME# → LPC_FRAME#
- 3.16.17 LPC_AD3 → LPC_AD3
- 3.16.17 LPC_AD2 → LPC_AD2
- 3.16.17 LPC_AD1 → LPC_AD1
- 3.16.17 LPC_AD0 → LPC_AD0

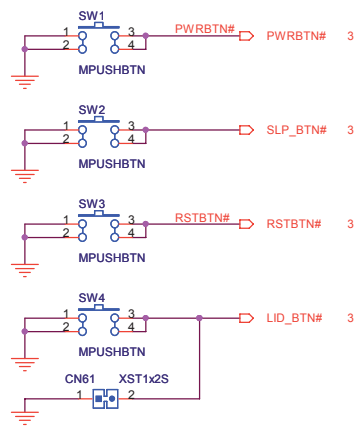


Title			
CAN / POSTcode			
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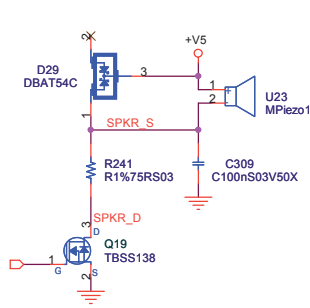
RTC/CMOS BATTERY



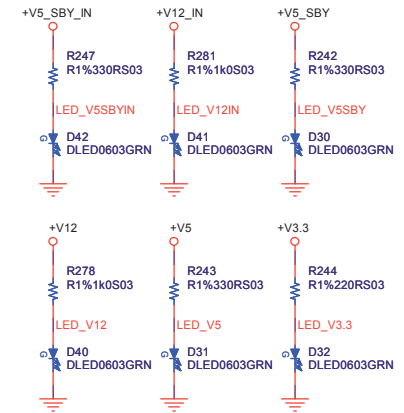
BUTTONS



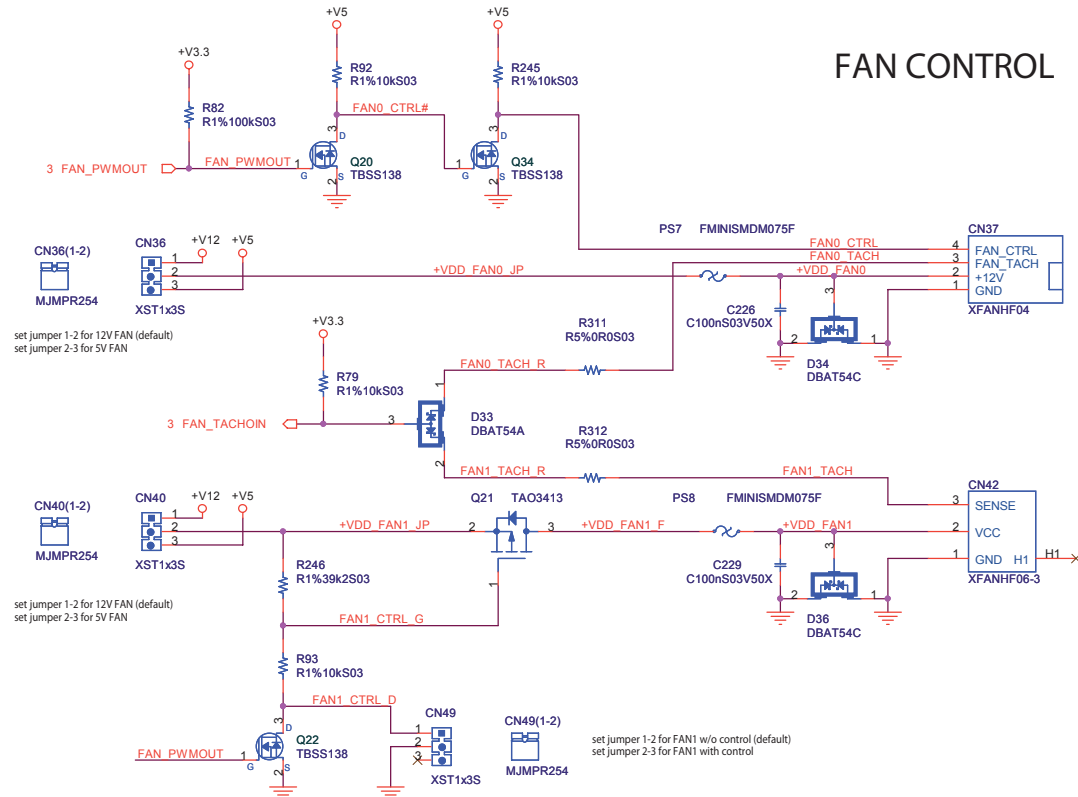
SPEAKER



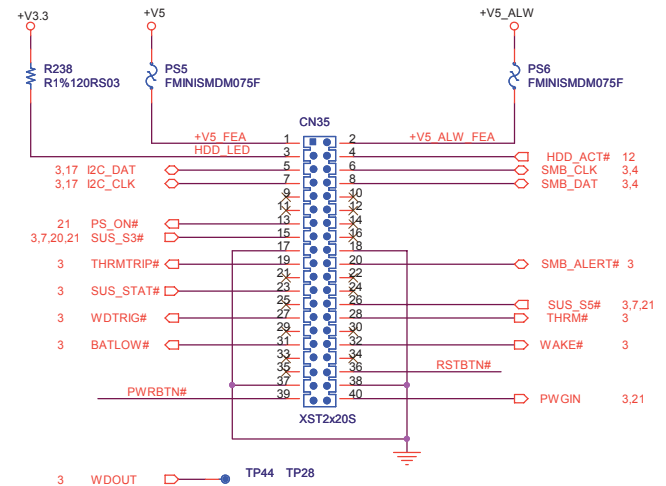
POWER LEDS



FAN CONTROL



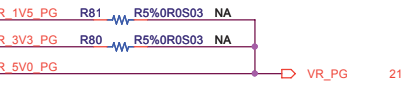
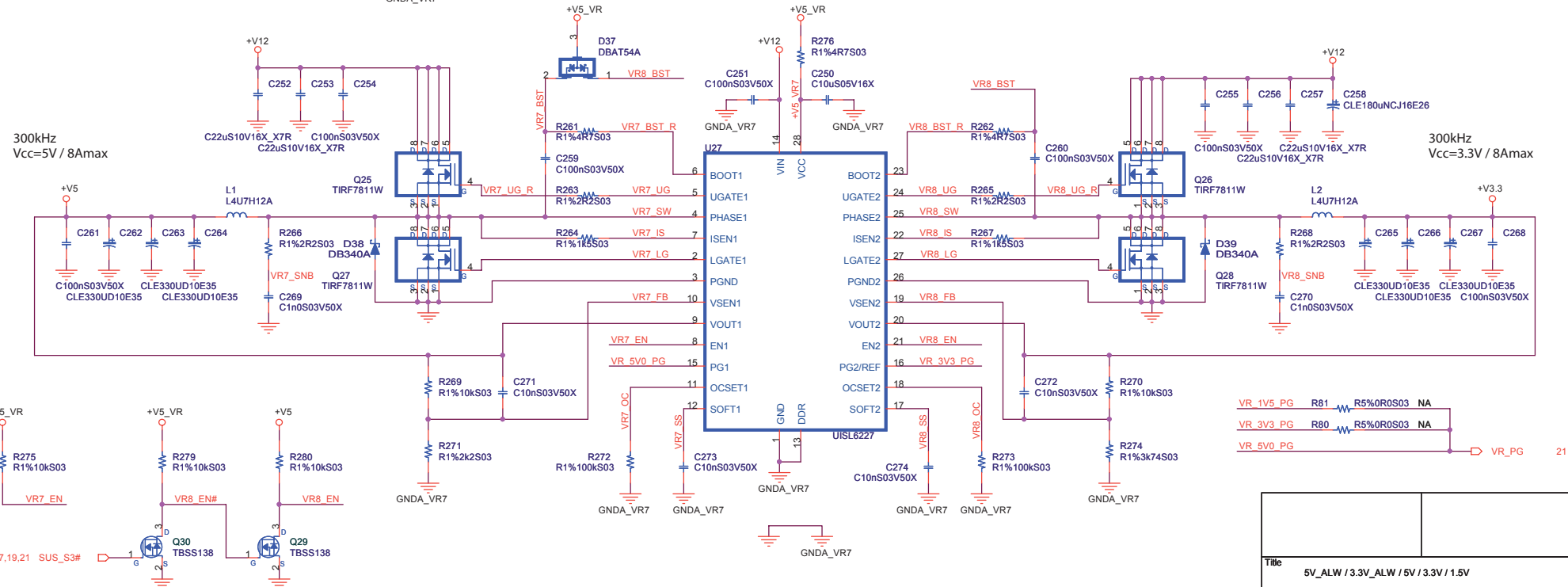
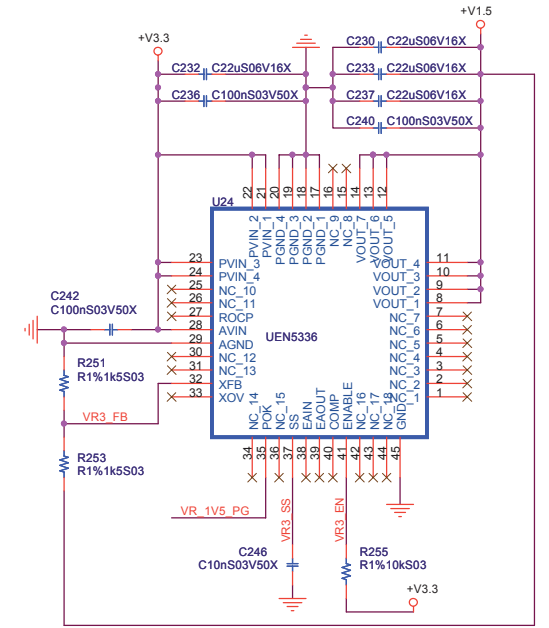
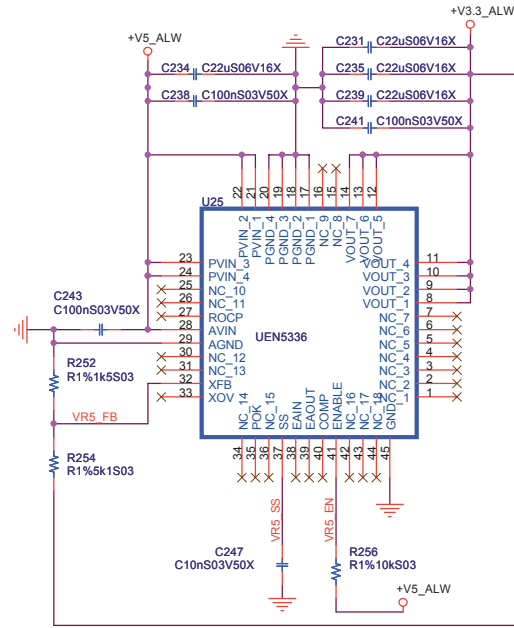
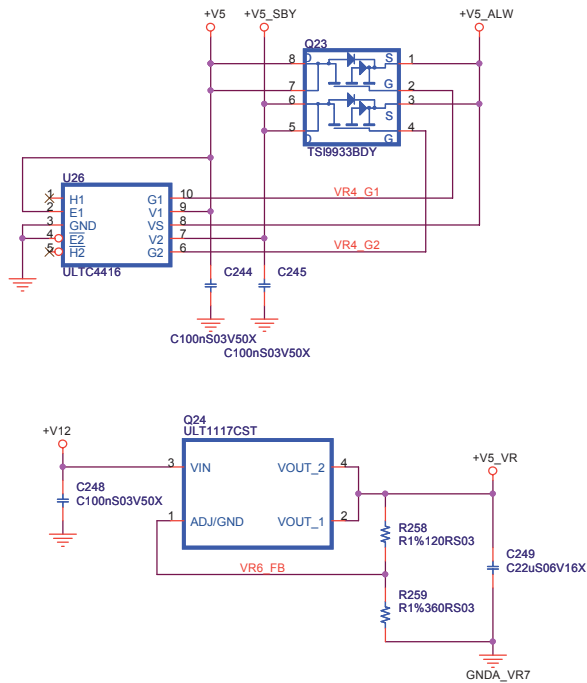
FEATURE



Title			
BATT / SPK / Feature / FAN			
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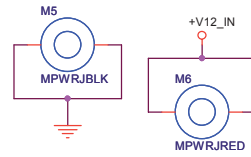
3.3V / 3Amax / 4.5Aoc

1.5V / 3Amax / 4.5Aoc

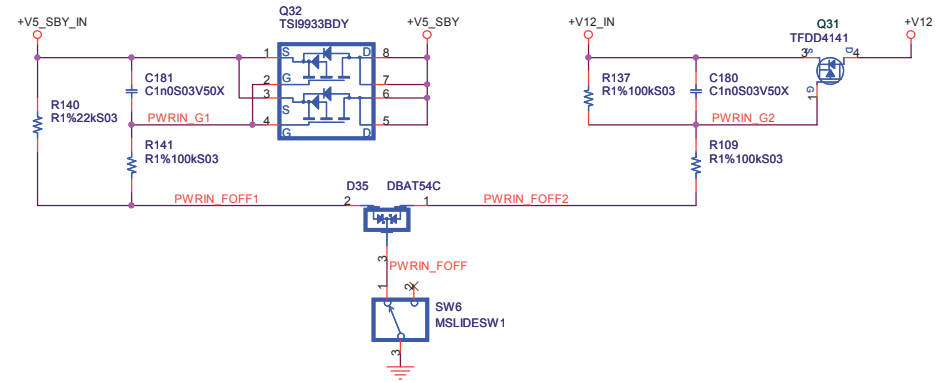


Title			
5V_ALW / 3.3V_ALW / 5V / 3.3V / 1.5V			
Size	Document Number	Created	Rev
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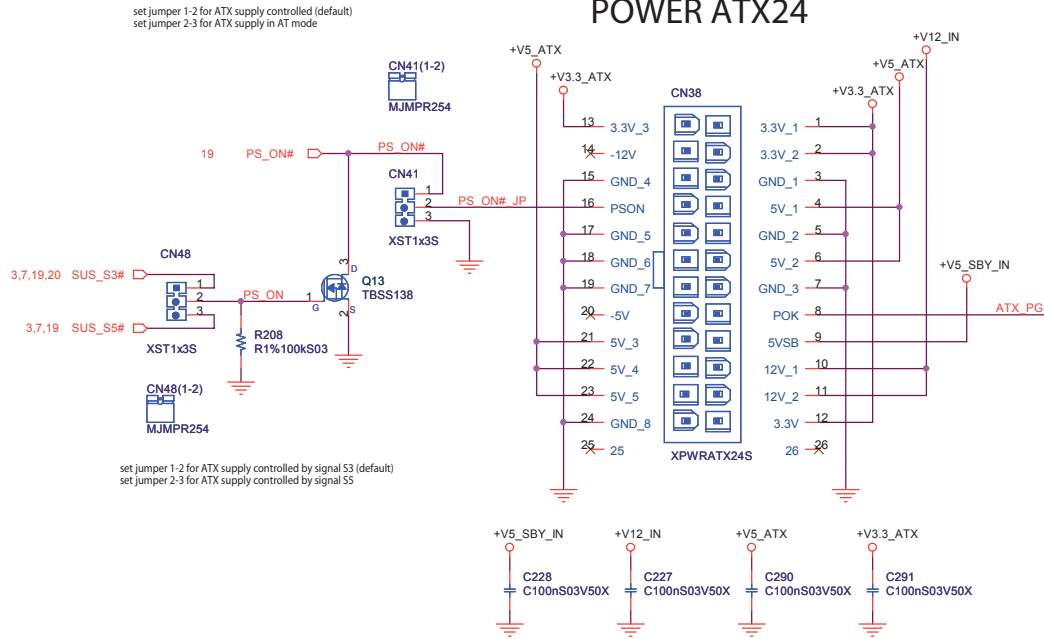
SINGLE +12V POWER IN



INPUT POWER VOLTAGE FORCED OFF



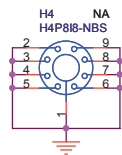
POWER ATX24



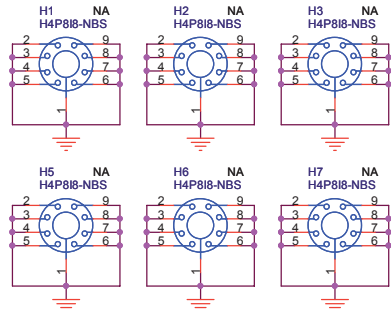
set jumper 1-2 for ATX supply controlled (default)
set jumper 2-3 for ATX supply in AT mode

set jumper 1-2 for ATX supply controlled by signal S3 (default)
set jumper 2-3 for ATX supply controlled by signal S5

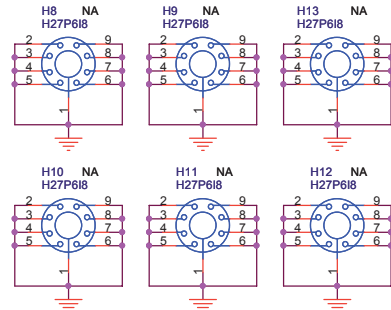
set jumper 1-2 for PU on PWGIN (default)
set jumper 3-4 for PWGIN from ATX
set jumper 5-6 for PWGIN from DC/DC



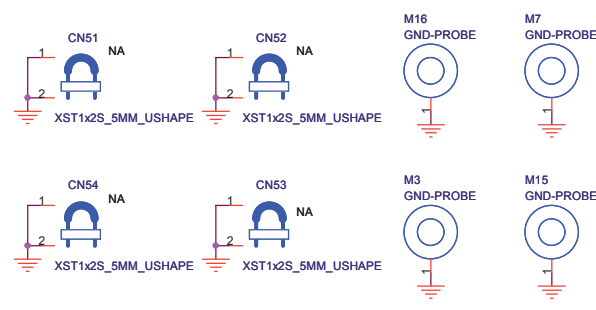
Backplane



Qseven



GND Probe



Title			
ATX24 / +12V POWER IN			
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Revision History

Rev. A.1	JUL\01\2009	DAKO	PG All	design created
Rev. A.2	OCT\01\2009	DAKO	PG All PG9	design converted to Arena U7 changed to ATMEL AT25010AN-10SU-2.7
Rev. B.0	NOV\01\2009	DAKO	PG3 PG3 PG4 PG6 PG7 PG8 PG9 PG12 PG13 PG14 PG15 PG16 PG17 PG20	added current sense resistors R293, R294, CN56, CN57 updated Qseven connector pinout according to specification 1.12; pins 91, 92, CAN0, SPI U4 74CBT3306 changed to 2x BSS138; SMBus for PCI Express connected to suspend powered SMBus miniCard socket connecting updated according to specification 1.2, added assembly option for back compatibility changed connection EXCD0_SHDN# to SUS_S5# and EXCD0_STBY# to SUS_S3# added assembly option for direct connection of Qseven PCIE0 port to PCIE slot removed SMBus connection to PEX8505 I2C interface; added pull-ups and test points to PEX8505 I2C interface updated SD/MMC Card Socket to MMC4.0 type (8bit) updated USB1 Host/Client selection circuit added support for configuration LED LINK10# instead of LINK# added all ALC888 input/output connection added PS/2 Keyboard and Mouse header connector; added KBD enable/disable to SW2 added SPI Flash added current load at ATX 5V and 3.3V
	DEC\23\2010		PG3 PG4 PG10 PG11 PG13 PG17 PG18 PG19 PG21	updated Qseven connector according to specification v1.20; added SPI, CAN connection; moved MFG pins to one head added PD resistors on all PCIE reset signals added DP/HDMI_HPD# connection to SDVO connector added JLL30 connector ; LVDS BKLT PWM to Analog converter changed USB ESD devices; updated USB1_CC circuit added BOOT_ALT# isolation buffer; added I2C EEPROM address DIP switch; added SMB EEPROM socket; added SPI header and DIP socket inserted sheet with CAN transceiver and POST added RTC battery diode; LID header; changed FAN CN37 connector to 4pin type chnaged PWGIN PU to 5V; changed GND probe

Title		Revision History	
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