Smart Mobility ARChitecture
Design Guide

SMARC Design Guide 2.1.1

April 29, 2021

REVISION HISTORY

Revision	Comments	Originator	Date
1.0	Initial Release	S. Milnor / Kontron	July 1, 2013
1.1	Created sharper images for Fig 19, 60, 69 Fixed small typos and grammar mistakes	S. Milnor / Kontron	July 5, 2013
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2.1.1	Update to SMARC 2.1.1 Hardware Specification	C. Rebmann / ADLINK	April 28, 2021

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1 INTRODUCTION

This document is based upon the “SMARC 2.1.1 Specification” document from 2020-05-20.

1.1 General Introduction

SMARC (“Smart Mobility Architecture”) is a computer Module standard maintained by the SGeT e.V. (“Standardization Group for Embedded Technologies”). SMARC Modules are small form factor (82mm x 50mm and 82mm x 80mm), low power computer Modules that are used on a Carrier board that utilizes a 314 pin 0.5mm pitch right-angle memory socket style connector to host the Module. SMARC Modules may utilize ARM, low power RISC or low power x86 CPUs / SOCs.

The SMARC Modules are specified in the SGeT ***Smart Mobility Architecture Hardware Specification 2.1.1***. The specification document is available free of charge from the SGET web site (**www.sget.org**), subject to their terms of use.

Similarly, this ***SMARC Design Guide*** is available free of charge from the SGET web site, subject to the SGET terms of use.

1.2 Purpose of This Document

The primary purpose of this document is to serve as a Design Guide for developers of SMARC Carrier Boards and for SMARC Module customers who wish to have a SMARC based system developed.

A secondary purpose of this document is to serve as a reference to SMARC Module developers, to help them understand the application of the Modules they are developing.

Finally, this document should be valuable to FAEs and Product managers to help them understand the SMARC Module infrastructure.

1.3 Design Help

There are a number of ways to have a SMARC Carrier board developed:

- Design internally, but have your SMARC Module vendor review your design. Make sure to also have the appropriate semiconductor companies review the portions of the design that utilize their components.
- Use a 3rd party firm that specializes in SMARC Carrier development. Such resources may be listed on the SGET web page (**www.sget.org**).
- Contact your SMARC Module vendor. The Module vendor will have an FAE available for advice. Many vendors will also undertake custom Carrier design projects, for significant opportunities.

1.4 Abbreviations and Acronyms Used

- **ADC** Analog to Digital Converter
- **ARM** Advanced RISC Machines _____ **www.arm.com**
- **BCT** Boot Configuration Table
- **BSP** (software) Board Support Package
- **CAD** Computer Aided Design
- **CAN** Controller Area Network
- **CPLD** Complex Programmable Logic Device
- **CODEC** Coder – Decoder
- **CSI** Camera Serial Interface _____ **www.mipi.org**
- **DAC** Digital to Analog Converter
- **DB-9** Connector, D shaped, B shell size, 9 pins
- **DDC** Display Data Channel
- **DDI** Digital Display Interface
- **DE** Differential Ended (signal pair)
- **DNI** Do Not Install (component is not loaded)
- **DP** DisplayPort
- **DP++** Dual-mode DisplayPort
- **DSP** Digital Signal Processor
- **DSI** Display Serial Interface
- **EDID** Extended Display Identification Data _____ **www.vesa.org**
- **EEPROM** Electrically Erasable Programmable Read Only Memory
- **eMMC** Embedded Multi Media Card _____ **www.jedec.org**
- **ESD** Electro Static Discharge
- **FET** Field Effect Transistor
- **FIFO** First In First Out (buffer memory)
- **FS** Full Speed (USB 1.1 12 Mbps)
- **GBE** Gigabit Ethernet _____ **www.ieee.org**
- **Gbps** Gigabit per second
- **GPIO** General Purpose Input / Output
- **GPS** Global Positioning System
- **HDA** High Definition Audio – Intel defined format_____ **www.intel.com**
- **HDMI** High Definition Multimedia Interface _____ **www.hdmi.org**
- **HID** Human Interface Device: USB device class
- **HS** High Speed (USB 2.0 480 Mbps)
- **IC** Integrated Circuit
- **I2C** Inter-Integrated Circuit _____ **www.nxp.com**
- **I2S** Inter-Integrated Circuit – Sound _____ **www.nxp.com**
- **IEEE** Institute of Electrical and Electronics Engineers _____ **www.ieee.org**
- **IO** Input Output
- **ISO** International Organization for Standardization (French) _____ **www.iso.org**
- **JEDEC** Joint Electron Device Engineering Council _____ **www.jedec.org**

- **JPEG** Joint Photographic Experts Group _____ **www.jpeg.org**
- **LED** Light Emitting Diode
- **Li-Ion** Lithium Ion (rechargeable battery technology)
- **LVDS** Low Voltage Differential Signaling
- **M2.5** Metric 2.5mm
- **M3** Metric 3.0mm
- **MAC** Media Access Controller (e.g. logic circuits in GBE)
- **Mbps** Megabit per second
- **MIPI** Mobile Industry Processor Interface_____ **www.mipi.org**
- **MLC** Multi Level Cell (flash memory reference)
- **MOD** Module (the SMARC Module) (schematic notation)
- **MO-297** Module Outline 297 (“Slim SATA” format) _____ **www.jedec.org**
- **MO-300** Module Outline 300 (mini-PCIe Express card format) _____ **www.jedec.org**
- **MPEG** Motion Picture Experts Group _____ **www.mpeg.org**
- **MXM** Mobile pci eXpress Module _____ **www.mxm-sig.org**
- **MXM3** MXM Revision 3
- **NAND** A high density flash memory technology
- **ns** Nano second (10 E -9)
- **NC** Not Connected
- **NXP** A semiconductor company_____ **www.nxp.com**
- **OS** Operating System
- **OTG** On the Go (USB term – device can be host or client)
- **PCB** Printed Circuit Board
- **PHY** Physical (transceiver) – drives cable
- **PICMG** PCI Industrial Computer Manufacturing Group _____ **www.picmg.org**
- **PCI** Peripheral Component Interface _____ **www.pcisig.org**
- **PCIe** PCI Express _____ **www.pcisig.org**
- **PCI-SIG** PCI Special Interest Group_____ **www.pcisig.org**
- **PCM** Pulse-Code Modulation
- **PD** See USB PD
- **PLL** Phase Locked Loop
- **POE** Power Over Ethernet
- **ps** Pico second (10 E -12)
- **PWM** Pulse Width Modulation
- **RGB** Video data in Red Green Blue pixel format
- **RISC** Reduced Instruction Set Computing
- **ROM** Read Only Memory
- **RS232** Recommend Standard 232 (asynchronous serial ports)
- **RS485** Asynchronous serial data, differential, multidrop
- **RTC** Real Time Clock (battery backed clock and memory)
- **SAR** Successive Approximation Register
- **SATA** Serial ATA (serial mass storage interface) _____ **www.sata-io.org**
- **SD** Secure Digital (memory card)

- **SE** Single Ended (signal, as opposed to differential)
- **SGeT** Standardization Group for Embedded Technologies _____ **www.sget.org**
- **SLC** Single Level Cell (flash memory reference)
- **SMARC** Smart Mobility Architecture _____ **www.sget.org**
- **SOC** System On Chip
- **S/PDIF** Sony/Philips Digital Interconnect Format
- **SPI** Serial Peripheral Interface
- **SSD** Solid State Disk
- **TI** Texas Instruments – semiconductor company _____ **www.ti.com**
- **TIM** Thermal Interface Material
- **UART** Universal Asynchronous Receiver Transmitter
- **UL** Underwriters Laboratories _____ **www.ul.com**
- **USB** Universal Serial Bus _____ **www.usb.org**
- **USB PD** USB extension specification for Power Delivery _____ **www.usb.org**
- **VESA** Video Electronics Standards Association _____ **www.vesa.org**
- **WEC7** Windows Embedded Compact 7 (an OS)
- **YUV** Video data format, more common in television
- **X5R** Ceramic capacitor dielectric – good quality
- **X7R** Ceramic capacitor dielectric – best quality
- **X86** Intel architecture (80x86) CPUs

1.5 Document References

1.5.1 SGET Documents

- ***Smart Mobility Architecture Hardware Specification***, V 2.1.1, May 20, 2020 © SGET (Standardization Group For Embedded Technologies) **www.sget.org**

1.5.2 Industry Standards Documents

- ***BT.656*** ("Recommendation ITU-R BT.656-5 Interface for digital component video signals in 525-line and 625-line television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601"), International Telecommunications Union, December 2007 (**www.itu.int**)
- ***CAN*** ("Controller Area Network") Bus Standards
  ISO 11898-1:2015 Road vehicles - Controller area network (CAN) - Part 1: Data link layer and physical signaling, (**https://www.iso.org**)
  ISO 11992-1:2019 Road vehicles - Interchange of digital information on electrical connections between towing and towed vehicles - Part 1: Physical and data-link layers (**https://www.iso.org**)
  SAE J2411: Feb 14, 2000, Single Wire CAN Network for Vehicle Applications (**https://www.sae.org**)
- ***MIPI CSI-2*** (Camera Serial Interface version 2) The MIPI CSI-2 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)
- ***MIPI CSI-3*** (Camera Serial Interface version 3) The MIPI CSI-3 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)
- ***COM Express*** – the formal title for the COM Express specification is "PICMG® COM.0 COM Express Module Base Specification", Revision 3.0, March 31, 2017. This standard is owned and maintained by the PICMG ("PCI Industrial Computer Manufacturer's Group") (**www.picmg.org**)
- ***DisplayPort and Embedded DisplayPort*** These standards are owned and maintained by VESA ("Video Electronics Standards Association") (**www.vesa.org**)
- ***MIPI DSI*** (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)
- ***eMMC*** ("Embedded Multi-Media Card") The eMMC electrical standard is defined by JEDEC JESD84-B51A and the mechanical standard by JESD84-C44 (**www.jedec.org**)
- ***eSPI*** ("Enhanced Serial Peripheral Interface") The eSPI Interface Base Specification is defined by Intel (**https://www.intel.com**)
- ***Fieldbus*** - this term refers to a number of network protocols used for real – time industrial control. Refer to the following web sites: **www.profibus.com/download/** and **www.can-cia.org**
- ***GBE MDI*** ("Gigabit Ethernet Medium Dependent Interface") this is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (**www.ieee.org**)
- ***HDA (HD Audio)***, High Definition Audio Specification, Intel, Revision 1.0a, June 17, 2010 (**http://www.intel.com**)
- ***HDMI Specification***, Version 2.1, November 28, 2017 (**www.hdmi.org**)
- ***I2C Specification***, Version 6.0, April 4th 2014, Philips Semiconductor (now NXP) (**www.nxp.com**)
- ***I2S Bus Specification***, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (**www.nxp.com**)
- ***IEEE1588 - 2008***. IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems (***http://standards.ieee.org***)

- ***JEDEC MO-300 (mSATA)*** defines the physical form factor of the mSATA format (**www.jedec.org**). The electrical connections are defined in the Serial ATA document.
- ***JTAG*** ("Joint Test Action Group") This is defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (**https://ieeexplore.ieee.org**)
- ***MXM3*** Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.1, NVidia Corporation
- ***PICMG® EEEP*** Embedded EEPROM Specification, Rev. 1.0, August 2010 (**www.picmg.org**)
- ***PCI Express*** Specifications (**www.pci-sig.org**)
- ***RS-232*** (EIA "Recommended Standard 232") this standard for asynchronous serial port data exchange dates from 1962. The original standard is hard to find. Many good descriptions of the standard can be found on-line, e.g. at Wikipedia, and in text books.
- ***Serial ATA*** Revision 3.1, July 18, 2011, Gold Revision, © Serial ATA International Organization (**www.sata-io.org**)
- ***SD Specifications*** Part 1 Physical Layer Simplified Specification, Version 6.00, Aug 29, 2018, SD Group and SD Card Association ("Secure Digital") (**www.sdcard.org**)
- ***SM Bus*** – "System Management Bus" Specification Version 3.1, March 19, 2018, System Management Interface Forum, Inc. (**http://www.smbus.org**)
- ***SPI Bus*** – "Serial Peripheral Interface" – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (**http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus**)
- ***UL 1642 Lithium Batteries –*** safety standard governing the use of lithium batteries (**www.ul.com**)
- ***USB Specifications*** (**www.usb.org**).
- ***VESA Enhanced Extended Display Identification Data Standard,*** Rev. 1, Feb 9, 2000, VESA (**www.vesa.org**) See also the "EDID" page on Wikipedia.

1.6 Schematic Example Correctness

The schematic examples shown in this Design Guide are believed to be correct, but correctness cannot be guaranteed. Most of the examples have been pulled from designs that have been built, tested, and are known to work. Most of them have been re-formatted to fit better in this design guide.

Note: The selection of the proper power domain (Sleep/ Standby/ RunTime) may not be reflected in the schematic parts. Please make sure to connect the needed power source in your design as your application requires it. If in doubt, please also consider the SMARC Hardware Specification for additional input and to prevent back powering to the Module.

1.7 Software Support

Many hardware examples and suggestions are given in the following pages. SMARC Carrier hardware design is generally straightforward. However, before committing to a particular hardware selection, it is wise to check out the software driver support. A particular device may be supported in, say, for example, Linux but not in Windows. Your overall project may go smoother if you pick out hardware that already has software support in your target OS.

There are various possible sources for software drivers for a particular IC: the IC vendor, the OS vendor, the OS community, your Module vendor, your Carrier design partner, other independent sources and of course writing your own.

Most SMARC Module vendors offer a BSP (Board Support Package) for their Module. Your target Carrier device may be supported in the BSP – check this angle out as well.

1.8 Schematic Example Conventions

Some of the conventions used in the schematic examples are described below. Note off-page connections that tie directly to the SMARC Module have the notation “MOD” in the off-page connect symbol.

Note: The “DNI” designation on the schematics stands for “Do Not Install” – i.e. the part is not loaded, in the example.

Figure 1 Schematic Symbol Conventions

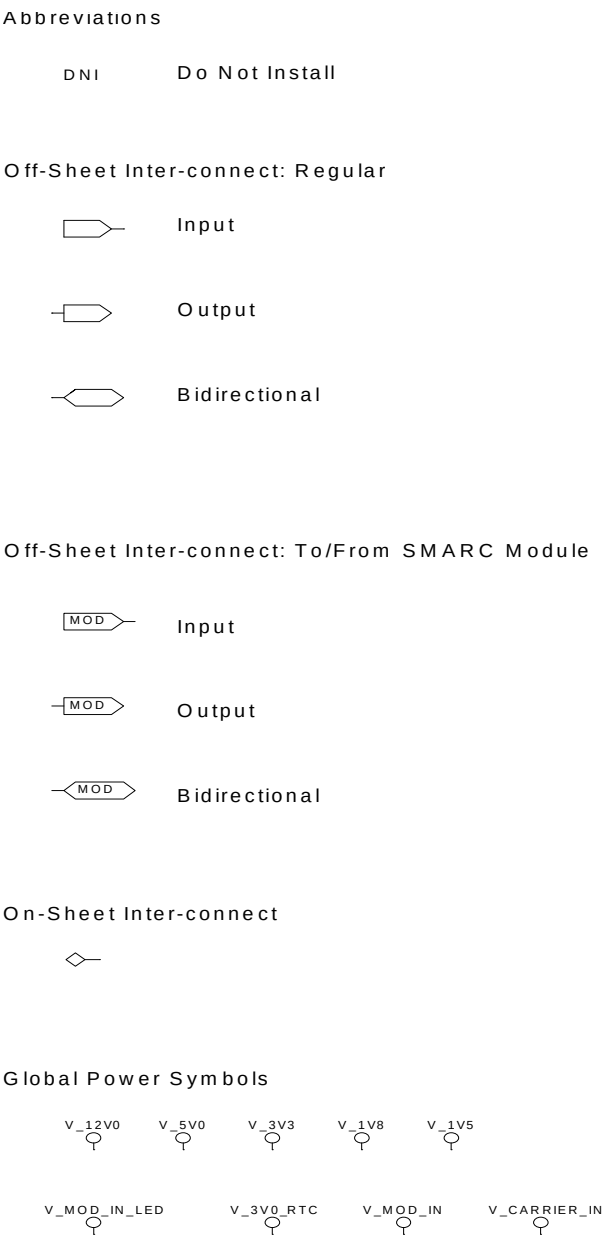


Table 1 Schematic Power Net Naming

V_IN_RAW	Power-In to the overall system, before any filtering, fusing, polarity or rise time protection.
V_IN	Power-In to the overall system, after (optional) filtering, fusing, polarity or rise time protection.
V_MOD_IN	Power into the SMARC Module VDD_IN pins (pins P148-156). It must be within the 3.0V to 5.25V or 4.75V to 5.25V range defined by the SMARC specification and the Module vendor.
V_CARRIER_IN	Power into the Carrier Board. It may be the same as V_MOD_IN, depending on the design at hand. On SMARC Evaluation Carrier boards, V_CARRIER_IN is sometimes kept separate from V_MOD_IN to allow easier measurements and tracking of where the power goes.
V_5V0	5V supply on the Carrier Board
V_3V3	3.3V supply on the Carrier Board
V_1V8	1.8V supply on the Carrier Board
V_1V5	1.5V supply on the Carrier Board
V_3V0_RTC	Supply voltage from the Carrier Board to the SMARC VDD_RTC pin (pin S147) This is a low voltage, low current supply separate from V_MOD_IN, used to supply the Module RTC (Real Time Clock) in the absence of V_MOD_IN.
V_MOD_IN_LED	Same as V_MOD_IN except isolated by a series jumper – used for power status LEDs – jumper can be removed to prevent status LEDs from consuming power.

2 INFRASTRUCTURE: CONNECTOR, POWER DELIVERY, SYSTEM MANAGEMENT

2.1 Module Connector

The SMARC Module connector is well described in the ***Smart Mobility ARChitecture Hardware Specification 2.1.1*** and the complete description is not repeated here.

Briefly, the SMARC Module connector is a low profile, right angle 314 pin memory – socket style connector. The same connector is commonly used for MXM3 graphics cards. However, it is important to understand that the SMARC usage and pin-out of this connector is totally different from the usage as graphics card.

The SMARC Module connector is available from multiple sources, including at least one vendor that has qualified their offering for automotive use.

Various height profiles are available for the SMARC Module connector. The lowest profile available has a Carrier Board PCB top-side to Module PCB bottom-side separation of 1.5mm, and a connector body height of 4.3mm.

Figure 2 Module Connector Pins P1-74 and S1-75

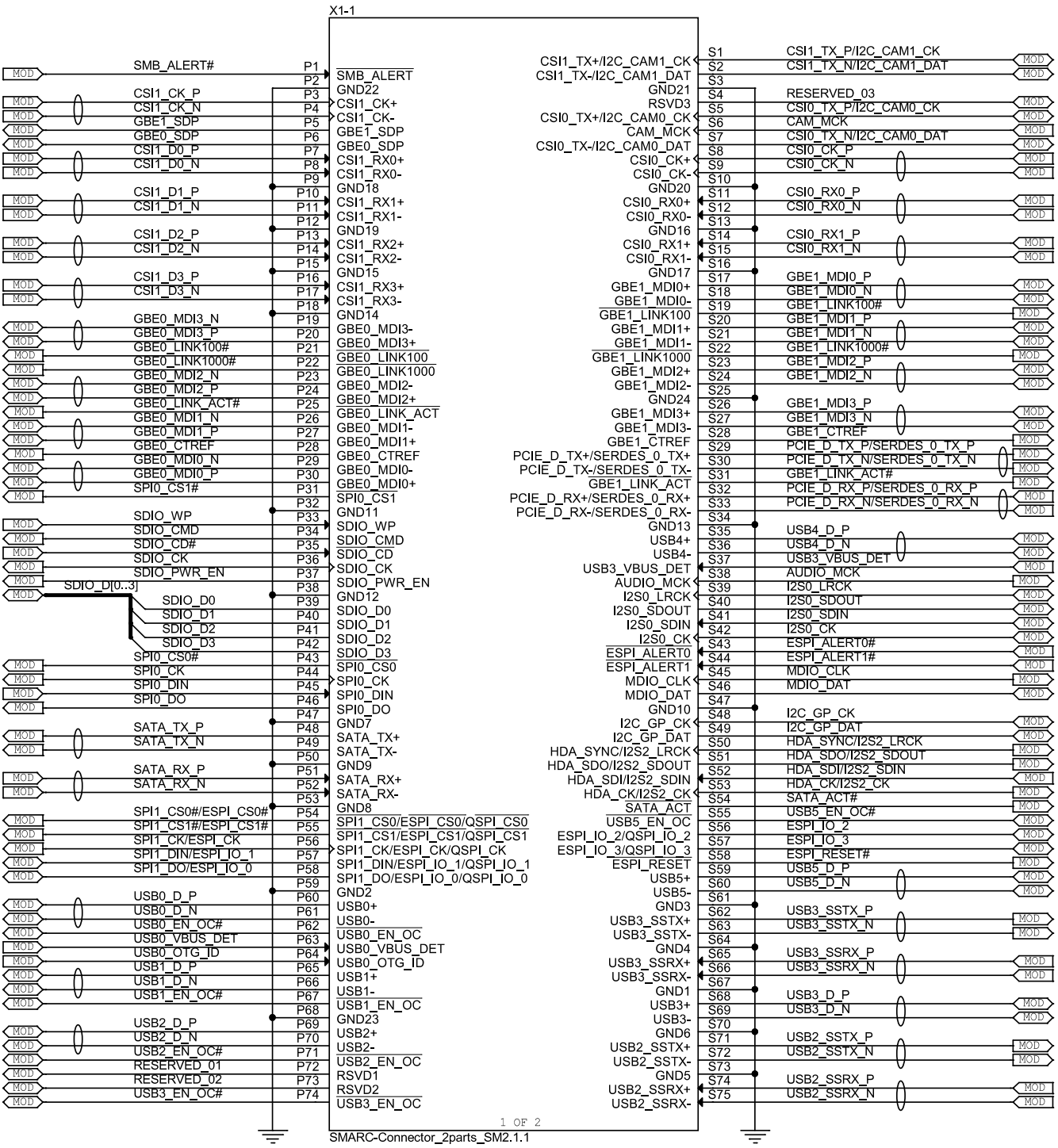
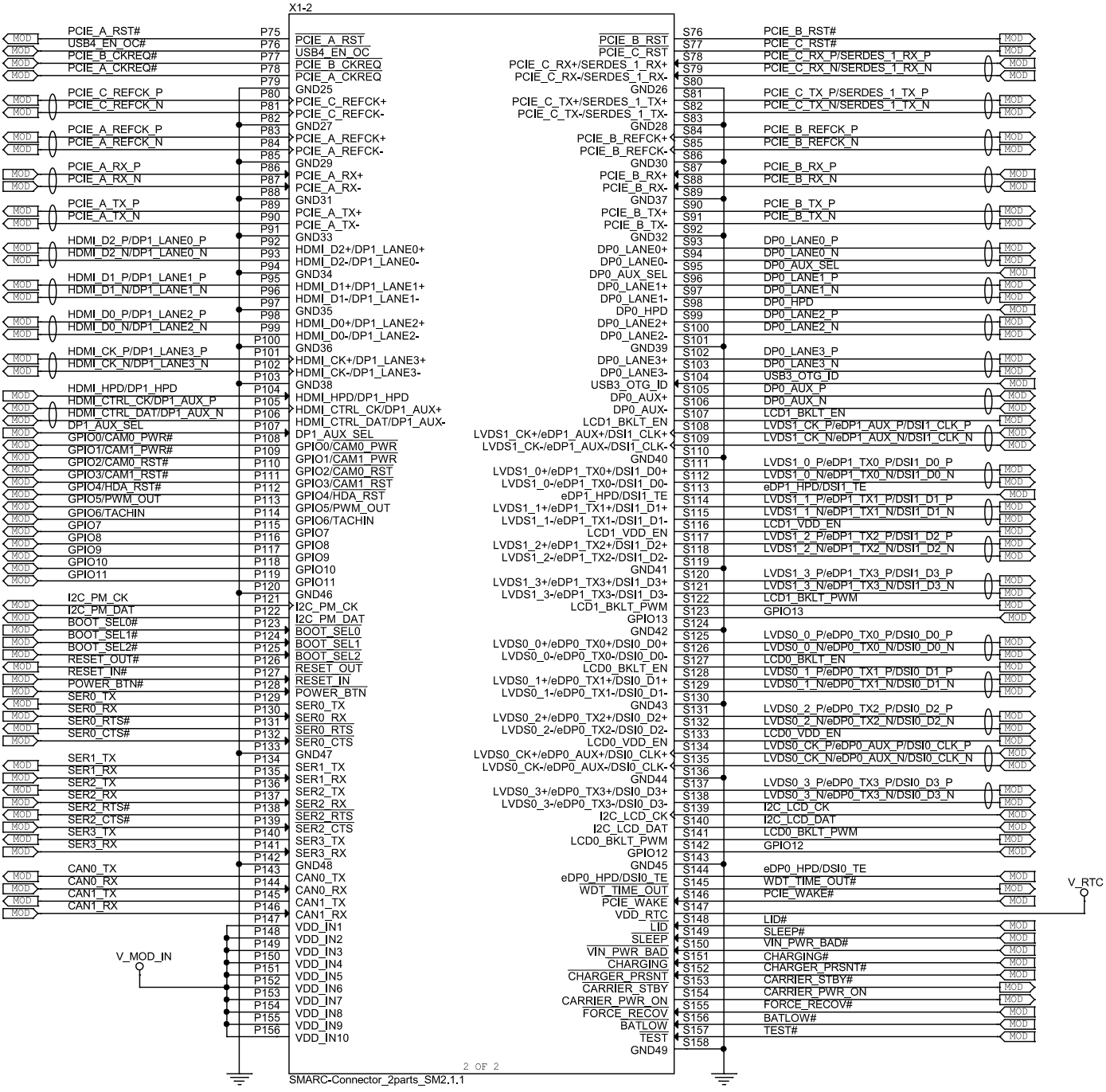


Figure 3 Module Connector Pins P75-156 and S76-158



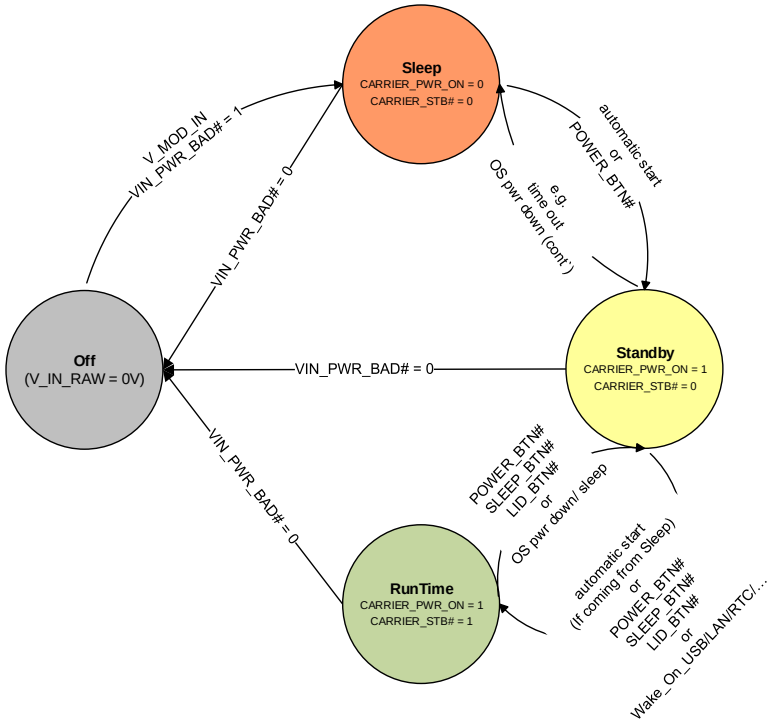
2.2 Module Power

With the SMARC Module specification 2.1.1 the power up process of the module was updated. The new version separates now 4 power states:

- Sleep
  As soon as the VIN_PWR_BAD# signal is high the SMARC module will enter the Sleep state. Depending on the module design and settings (for example BIOS configuration) the module will automatically continue to enter the Standby state automatically or will wait for a PWR_BTN event.
- Standby
  The CPU on the SMARC module is in a power saving mode. Please refer to the SMARC module product manual what states are supported and how to achieve them or contact your module vendor.
- RunTime
  The SMARC module is fully operational and can be controlled from OS level. The OS or external events (such as PWR_BTN#, …) can issue a state change to one of the other states.
- Off
  The SMARC module will be in “Off” state as long as the VIN_PWR_BAD# signal is held low.

The following state machine provides an overview of the different states and dependencies between them:

Figure 4 Module (System) power state diagram



Note: Some of the reference schematics in later chapters of this document might show power rails that will disable the function in Standby or Sleep states. For example SPI devices should be connected to

xVx_STB rails but are shown on a RunTime voltage. Please consider the proper voltage per your design. (I.e. Wake on USB is only possible, when USB is powered during Standby. If that is not needed a RunTime voltage is usable to reduce the power consumption during Standby and Sleep.)

2.2.1 Input Voltage Range

Per the SMARC Module Hardware Specification, the SMARC Modules may accept input power over the voltage range 3.0V to 5.25V for “low power” platforms. This voltage range coincides with the range of a single-level lithium – ion cells and allows the use of common 5V or 3.3V fixed DC supplies.

For “high power” platforms the Module may be designed to accept 4.75V to 5.25V. Please check the Module documentation or contact you SMARC Module vendor which supply range applies to a specific Module.

2.2.2 Input Voltage Rise Time

There are currently no limits in the SMARC Module Hardware Specification on the Module power supply rise times. In general, it is not wise to expose the Module and Carrier electronics to extremely fast power supply rise times (as may be the case if a low impedance power source such as a battery pack or power brick is “hot-plugged”). Input power supply rise times faster than 50V / millisecond to the Module should be avoided.

If a unit is to be “hot-plugged” to a low impedance power source, then the Carrier should implement measures to slow the power rise time as seen by the Module and Carrier circuits. The Carrier can do this by implementing a FET and hot-swap controller in the input power path. This is discussed in **section 9.5 Power Hot Swap Controller**.

2.2.3 Module Maximum Input Power

The SMARC V2.1.1 specification document states that the allowable input voltage range is 3.0V to 5.25V for low power modules or 4.75V to 5.25V for Modules that are using higher power CPUs/ SOCs. The rationale for the wide range input is that this range coincides with the voltage range of single level lithium-ion cells, and that it also allows the use of common 5V or 3.3V bench supplies. However, it is not mandatory in the V2.1.1 specification that Modules need to work at the lower end (3.0V) of this range.

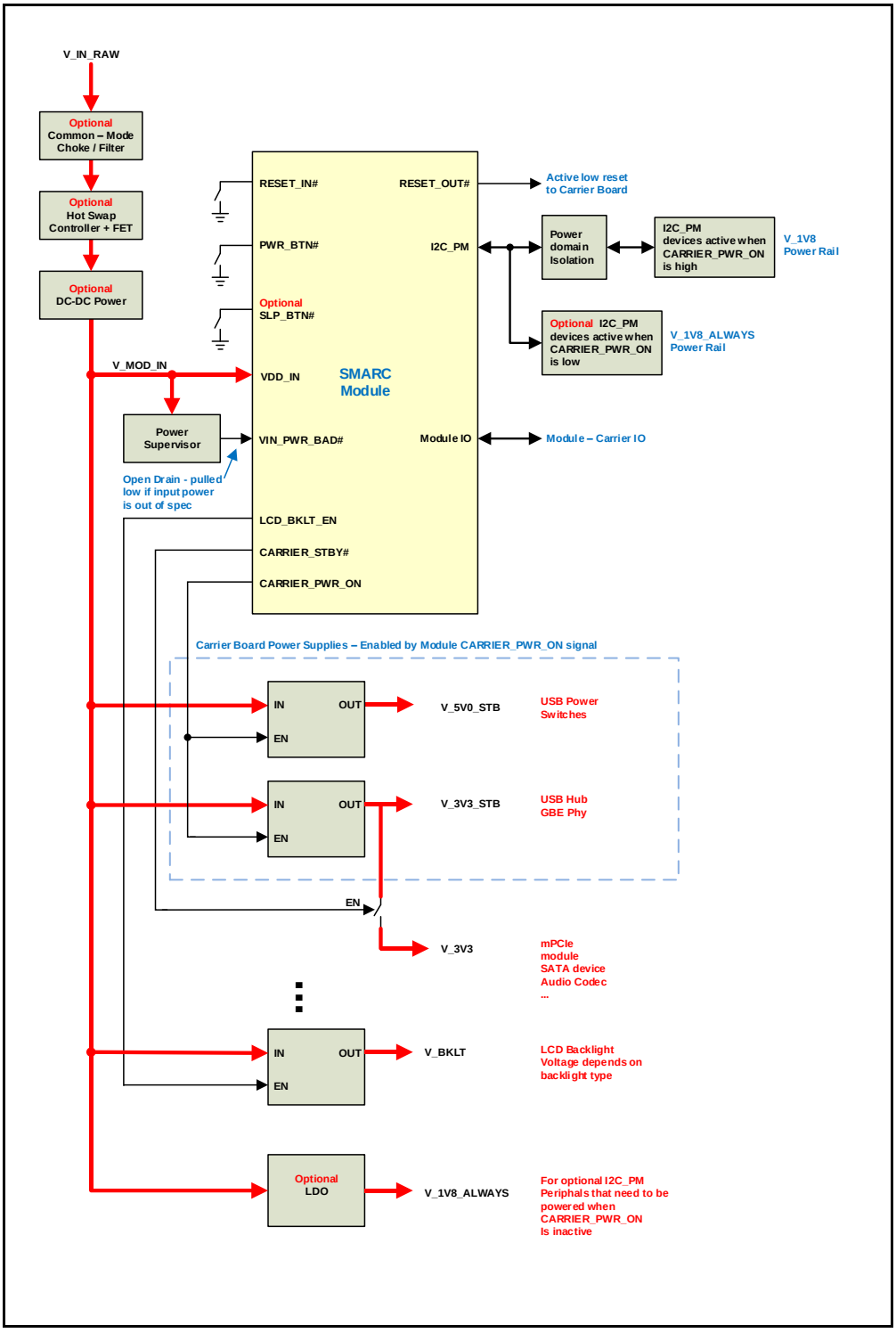
The SMARC Module physical connector is a MXM3 connector (although the pinout is completely different). The MXM3 specification document requires that the MXM3 connector pins be able to carry a minimum of 0.5A current per pin. SMARC Modules allocate 10 pins for input power (and 49 GND pins for signal and power return). Thus, per the MXM3 connector requirement, the 10 pins should be capable of handling 5A. This allows a maximum power input range of 15W (for 3.0V power in) to 26W (for 5.25V power in). However modern CPUs with dynamic power limits might have peak power requirements that go up to 28W and above.

Depending on the use case of the product and carrier it is suggested to develop the carrier power supply for the SMARC module with some overhead in order to be able and use multiple platform generations with one design. Please refer to the SMARC module datasheet and manuals or contact your module vendor for more information.

2.2.4 Power Path

The power path for a basic, fixed input voltage arrangement SMARC Module and Carrier board system is shown in **Figure 5 Basic Module and Carrier Power Path** below. A number of features in the figure are optional and may be omitted (and bypassed) in a minimal implementation. The figure also shows Carrier power supply sections assuming a typical system powered by a power source in the 3.0V to 5.25V range

Figure 5 Basic Module and Carrier Power Path



Note:

- V_xVx_ALWAYS power rails can be used to power circuitry that also shall be enabled during the Sleep state
- V_5V0_STB and V_3V3_STB define the power rail of the peripherals that are defined under a STANDBY power domain (i.e. SPI, QSPI, USB, GBE,…) and they are enabled by the CARRIER_PWR_ON signal.
- V_3V3 in **Figure 5 Basic Module and Carrier Power Path** represents the power supply of all the peripherals that are defined under the RUNTIME power domain : (ex: I2S interface) and that should be unpowered during STANDBY power state. They are enabled by CARRIER_STBY# signal. Some special “Enable” signals (example: LCB_BKLT_EN) should be combined with the CARRIER_PWR_ON signal so that unintentional enables during power up/ down are avoided (such as backlight flickering during power up at displays). Please check the interface chapters for more details.
- The real implementation of the voltage rails is Carrier Board dependent. This figure shall only illustrate how the different signals are used to control the power rails.

2.3 Module I/O Voltage

The SMARC Module Hardware Specification specifies the use of 1.8V Module I/O.

I/O at 1.8V is used in general for low power interfaces. Many contemporary peripherals of interest are available with I/O interfaces that support 1.8V and 3.3V; some are available at 1.8V only, and others at 3.3V only. Specific examples are given in various document sections below.

If devices that support only 3.3V are implemented, a level shifter has to be used to interface them to the SMARC Module. This is discussed in section **4.2.1. I2C Level Translation, Isolation and Buffering** below.

Note: Some signals also might be in use on the SMARC module so that Inputs (to the Module) that are not needed on the Carrier should be left floating from the Carrier side.

2.4 VIN_PWR_BAD#

This signal has to be used to tell the Module that the input power to the Module (V_MOD_IN) is not ready. An open-drain driver should be used.

Note: The VIN_PWR_BAD# signal status should match the used SMARC Module specification. A Module that is designed to operate with 4.75V to 5.25V shall not receive a VIN_PWR_BAD# = 1 when 3.0V is reached but only when 4.75V is reached.

2.5 CARRIER_PWR_ON

The CARRIER_PWR_ON signal is driven by the Module at a 1.8V level. It is a signal to Carrier that the Carrier specific power supplies that shall be powered during standby may be enabled. If standby power save state is implemented at the Carrier this signal enables the standby voltage rails. This is illustrated in **Figure 5 Basic Module and Carrier Power Path** above.

2.6 CARRIER_STB#

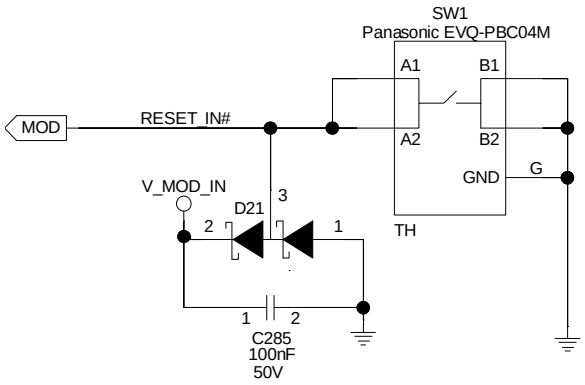
The CARRIER_STB# signal is driven by the Module at a 1.8V level. If the power save state standby mode is implemented at the Carrier the runtime voltage rails are enabled with this control signal from the Module. The Module drives this signal high to enable runtime power rails. If no separate standby mode is

implemented all rails are enabled with CARRIER_PWR_ON signal. This signal is driven high by the Module at runtime.

2.7 RESET_IN#

The SMARC RESET_IN# signal may be used to force the Module to stay in reset. This allows a device on the Carrier to pre-load its content (such as an FPGA) and to setup strap options before the Module is latching the boot straps or executes any code. It is an input to the Module but pulled up from the Module to a voltage in the range between 1.71V and 5.25V and is level sensitive at the power on. If used, by the Carrier, then an open drain device or switch to GND should be used. A switch example is shown in **Figure 6 Reset Switch**. The signal is ESD protected in this example, as the switch (and the switch interaction with humans) introduces an ESD hazard.

Figure 6 Reset Switch



Note: Repeatedly use of the RESET_IN# signal while the Module is already performing a reset cycle might lead to unknown behavior of the Module and therefore shall be avoided.

Note: During the Power Up Sequence the RESET_IN# signal may be released from the Carrier at any time. For more details please refer to chapter **2.11 Power Up Sequence**.

2.8 RESET_OUT#

The RESET_OUT# is a 1.8V signal that indicates to the Carrier HW if the Module wants to hold IC´s in reset while booting. It also can be used to re-initialize Carrier HW during a module reboot and is typically connected to the PLT_RST for x86 platforms in example.

The RESET_OUT# signal shall be use at the Carrier board for all devices addressed by the Module interfaces if possible. Due to SW defined pin function, signal level and SOC internal pull-up / -down resistors a safe signal state cannot be proven before the Module SW startup. Only after the initial power on event dedicated pull resistors can generate a resistor divider with the SOC internal default pull resistors. The finished Module (interface-) initialization is noted by the RESET_OUT# signal.

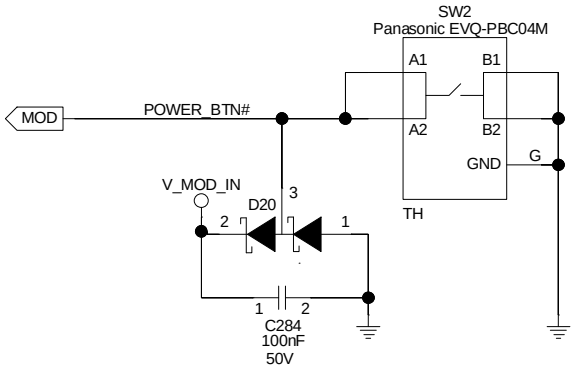
2.9 POWER_BTN#

SMARC defines a pin to allow the implementation of a Carrier based power button. However **- caution -** the SMARC Hardware Specification does not define the power up behavior of a Module. The following possibilities exist after a cold power on:

a) Module boots
b) Module waits for a Power Button press to boot
c) The Module is configurable – either behavior a) or behavior b) may be configured

Users are advised to check with your Module vendor on this topic. A Power Button switch example is shown in the **Figure 7 Power Button Switch below**. If your Module waits for a Power Button press on power up and you want it to always boot on power up, you have to arrange for a “power button press” on power up, using an open drain device to interface to the SMARC Module.

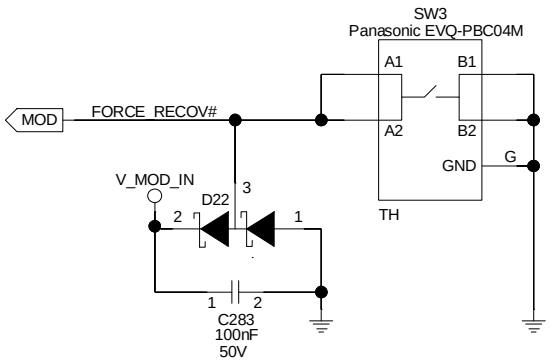
Figure 7 Power Button Switch



2.10 Force Recovery

Some Modules support a “force recovery” function in which the primary boot media can be re-initialized over a designated I/O interface, such as a USB client interface, asynchronous serial port, or Ethernet port. This is Module specific; refer to your Module documentation for further details.

Figure 8 Force Recovery Switch

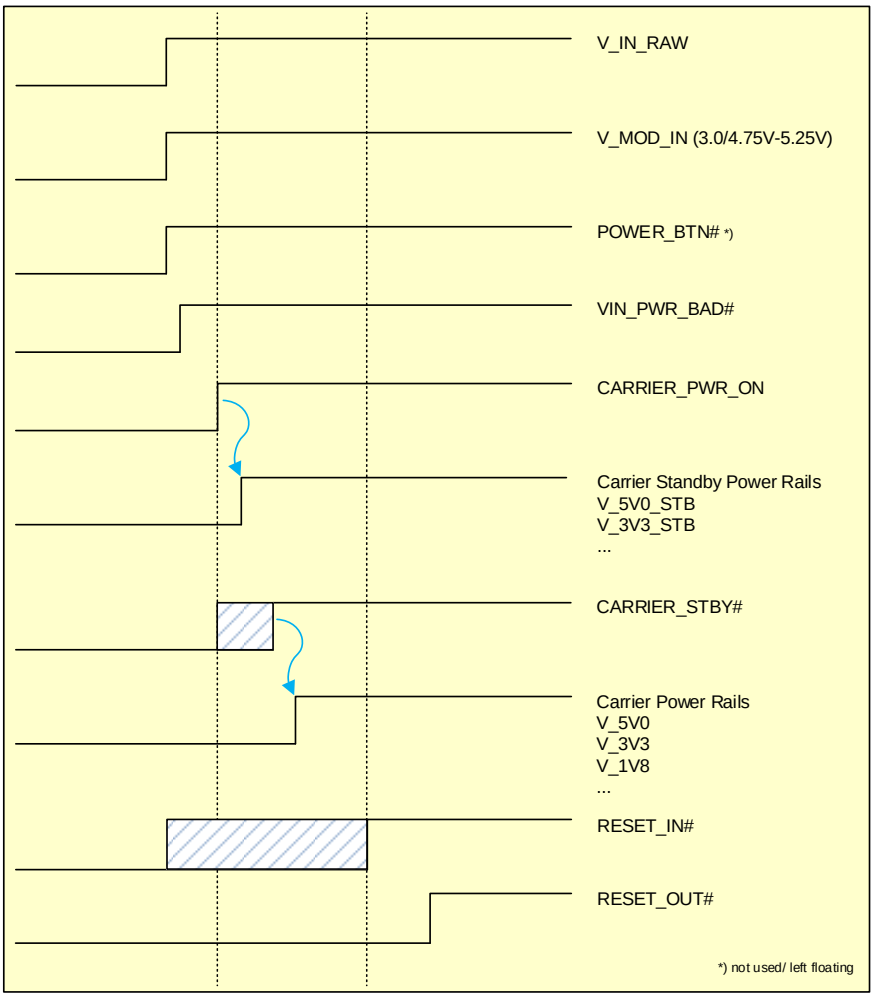


2.11 Power Up Sequence

The basic power up sequence for SMARC Modules and Carriers is shown in the following two figures. There is a Module design and / or configuration dependence with regard to the power button behavior. Depending on design and / or configuration, the Module may always boot without waiting for a power button press, or it may wait for a power button press. These cases are shown in below figures.

It is recommended to arrange that the main Carrier power supplies do not come up until the Module asserts the CARRIER_PWR_ON signal. When this is high, you know that the Module power supplies are all up. If the Carrier power is up before the Module supplies are up, there is a risk that the Carrier circuits will back-feed power to the Module I/O pins, which might interfere with a Module boot.

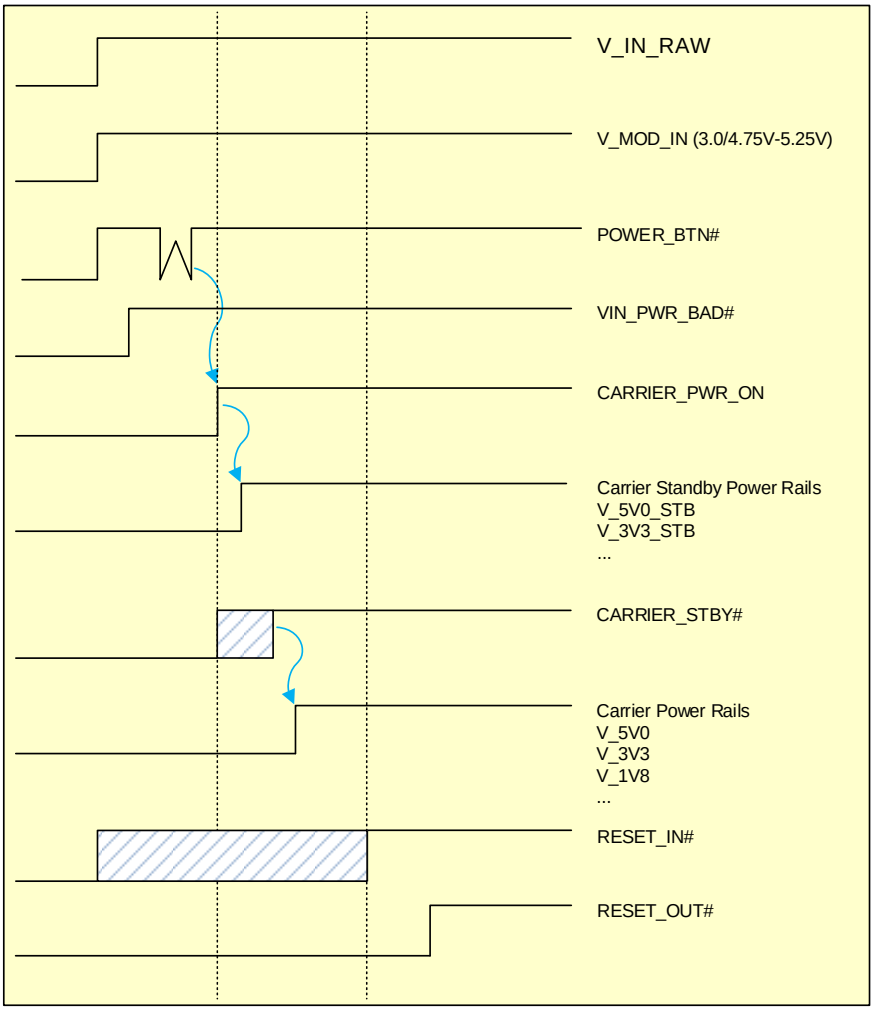
Figure 9 SMARC Carrier Power Up Sequence - No Power Button Case



The diagram below reflects the case of a Module that is designed or configured to wait for a power button press before it comes up. When power is applied to the Module, in this case, only a small portion of the Module is using that power – typically, the Module Power Management section – and that circuitry waits for a power button press. When it sees one, the Module proceeds with the boot. When the main Module

power rails are up, the Module asserts CARRIER_PWR_ON. The Carrier should use this signal to enable the various Carrier power rails. However, the Carrier circuits that are involved in power management (battery charge level, reset monitors, etc.) may be powered ahead of CARRIER_PWR_ON, coincident with the Module power.

Figure 10 SMARC Carrier Power Up Sequence - With Power Button Case



If the implementation is working with the POWER_BTN# signal as shown in **Figure 10 SMARC Carrier Power Up Sequence - With Power Button Case** than there are two possible implementations. The first one is that the Module is waiting in Sleep Mode for a Power Button event before it asserts the CARRIER_PWR_ON and sequential the CARRIER_STBY# signals to the Carrier. The second possible implementation is that the Module is waiting in the Standby Mode for a Power Button Event before it asserts the CARRIER _STBY# signal to the Carrier. In this case the CARRIER_PWR_ON signal is already asserted earlier.

Note: The **Figure 9 SMARC Carrier Power Up Sequence - No Power Button Case** shows the implementation for the Power Up scenario 2 and 4 from the SMARC Module specification. **Figure 10**

SMARC Carrier Power Up Sequence - With Power Button Case correlates with scenario 3 of the SMARC Module specification.

2.12 Sleep Mode

Some SMARC Modules will implement the Sleep Mode for a deep power saving mode. In this case the CARRIER_STBY# and the CARRIER_PWR_ON signals will be hold low from the Module to indicate to the Carrier that the Sleep Mode is active.

In order to prevent back powering from the Carrier to the Module all interfaces/ ICs that are not needed in this mode should be powerless on the Carrier.

In Order to Wake from the Sleep state the POWER_BTN# and if implemented the BATLOW# and the SMB_ALERT# signals can be used. Please refer to your Module documentation about the implementation of your Module.

2.13 Standby Mode

A low level on CARRIER_STBY# indicates that the system did enter the Standby state, where only power management functions, wake up functions and system memory are powered. The ACPI equivalent is “suspend to ram” (S3). This signal can be used to switch off power supplies on the Carrier board that are not necessarily needed during Standby.

Any devices that should be able to wake the system out of the Standby state should use power rails that are “on” when the CARRIER_PWR_ON signal is present. These can be besides the POWER_BTN# also Wake on USB or Wake on LAN for example.

Please also refer to the SMARC Module specification for power domain selection.

Note: If the CARRIER_STBY# is not used on the Carrier then OS/ SW shall take care that the Module is not going to a standby state. Back powering can prevent correct function of state changes if this is not implemented.

2.14 Boot Selection

2.14.1 Boot Definitions

Most SOCs used on SMARC Modules have the following attributes:

1) An internal ROM exists. The internal ROM code is executed after the SOC comes out of reset. This ROM code is provided by the silicon vendor and is generally not available or visible to users.
2) A set of SOC strap pins is used to select what SOC physical device interface (SD Card, SPI, eMMC, etc.) will be used for the second – stage boot process (also known as BCT or Boot Configuration Table boot). There is no commonality between various SOCs as to how the strap pins are defined.
3) The SOC pin configuration is very flexible – most SOC pins can be used for several functions, and the SMARC Module designer must choose a pin configuration that works for the design at hand. The SOC pin configuration is set by a Boot Configuration Table that is read out from the external boot media (SD Card, SPI, eMMC, etc.).

There are several stages in the boot process:

1) Internal SOC ROM execution
2) Second stage boot, from non-volatile memory external to the SOC: BCT is loaded and various other system parameters are set
3) Operating System load

The Operating System load may occur from the same memory as the second stage BCT boot, or the second stage code may pass the Operating System load off to another device, such as a USB drive or SATA drive.

2.14.2 SMARC BOOT_SEL Pins

The SMARC Hardware Specification defines 3 SMARC pins, designated BOOT_SEL0# through BOOT_SEL2#, which may be used to tell the Module what physical device to do a BCT boot from. The SMARC BOOT_SELx# pins serve to abstract the SOC – dependent strap definitions into a common SMARC definition. The table below is reproduced from the SMARC Hardware Specification document.

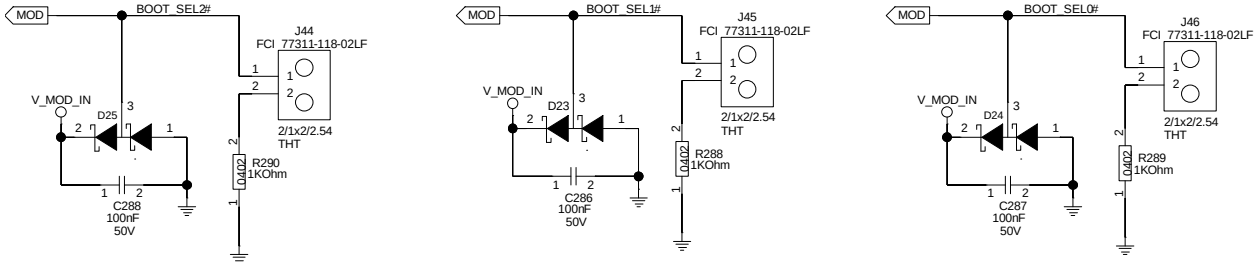
Table 2 Boot Select Pins

	Carrier Connection			Boot Source
	BOOT_SEL2#	**BOOT_SEL1#**	**BOOT_SEL0#**	
0	GND	GND	GND	Carrier SATA
1	GND	GND	Float	Carrier SD Card
2	GND	Float	GND	Carrier eSPI
3	GND	Float	Float	Carrier SPI
4	Float	GND	GND	Module device (NAND, NOR) – vendor specific
5	Float	GND	Float	Remote boot (GBE, serial) – vendor specific
6	Float	Float	GND	Module eMMC Flash
7	Float	Float	Float	Module SPI

The Module BOOT_SELx# pins may be set by jumpers on the Carrier Board, as shown in the **Figure 11 Boot Selection Jumpers** below. The diodes and capacitors are for ESD protection, as the jumpers may experience ESD events.

Alternatively, the BOOT_SELx# pins can be set by low value option resistors to GND on the Carrier. The resistors are either installed (for a GND connection) or not installed, per the **Table 2 Boot Select Pins above.**

Figure 11 Boot Selection Jumpers



Note: The Boot Select implementation off the Modules may not be available on all Modules. It is platform and vendor specific if none, some or all of above mentioned options are available. Also it might be that the Boot Select will work so that the first code fetch from the Module is on the listed device or that the SOC is always fetching the first code lines from a fix device and only then reacts on the pin selection. Please get in contact with your Module vendor for more details about a specific product.

2.15 RTC Backup Power

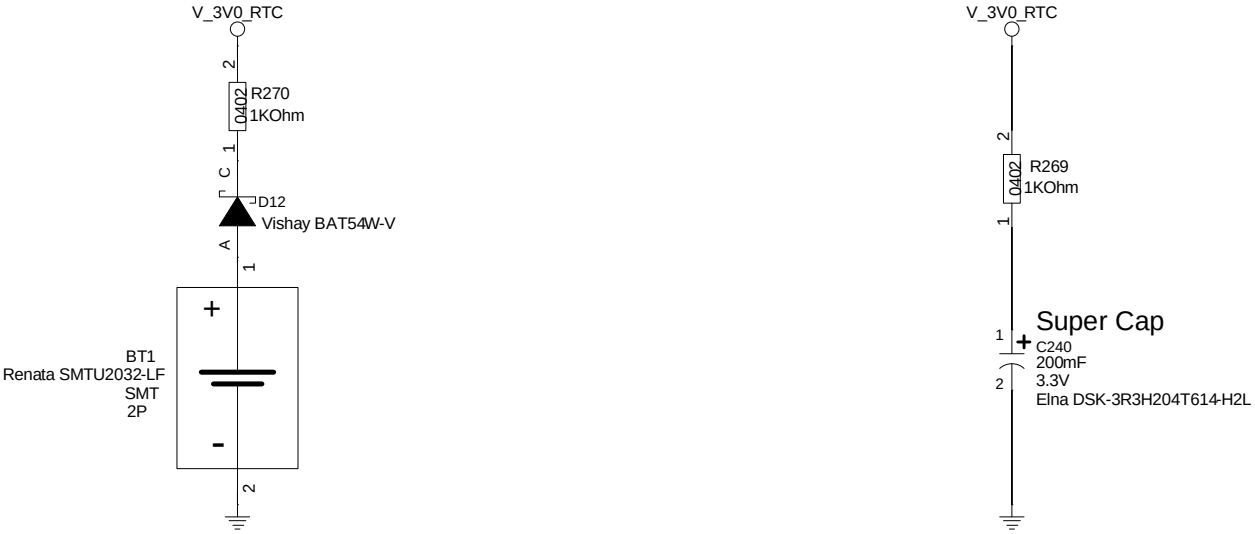
The Module RTC (Real Time Clock) circuit requires a backup power source if the Module RTC circuit is expected to keep time in the absence of the primary power source (i.e. the power to Module V_MOD_IN pins, P147 through P156). The RTC backup power, if used, is applied to the Module VDD_RTC pin, pin S147. The RTC backup power may be provided by a battery or by a large value capacitor, known as a "Supercap".

If a battery is used, the battery is typically a small lithium coin cell with a capacity of a few hundred mAh. Lithium coin cells offer a high energy density, low self-discharge rate, and are not rechargeable. For safety reasons, they must be protected against charging **on the Carrier board** by a redundant set of circuit elements – typically either two diodes in series or a diode and a resistor. The resistor, if used, must be large enough to limit the battery charging current to be equal to or lower than the amount specified as allowable by the battery vendor. The safety aspects of lithium battery use is governed by a UL document (***UL 1642 Lithium Batteries***, **www.ul.com**).

The Supercap solution differs from the lithium battery solution in that it needs to be charged by the Module (when the Module has its primary power source); hence a blocking diode should not be used with the Supercap.

The time period over which the RTC backup power is effective depends on the Module RTC backup current draw, the exact voltage range over which the Module RTC circuit is functional, on the capacity characteristics of the battery or Supercap, on the drops incurred across the Carrier board circuit protection elements, and on the operating temperature. In general terms, a suitable lithium battery solution can provide RTC backup current on a scale of years whereas the Supercap solution on a scale of days to weeks.

Figure 12 RTC Backup: Coin Battery / Super Cap



Coin Battery Holder, R/A, SMT

2.16 Reserved / Test Interfaces

The Module TEST# pin (pin S157) should normally be left not connected. If pulled low, then Module specific test function(s) may be enabled.

Reserved pins should be left not connected and may be used in future revisions of the SMARC specification.

3 DISPLAY INTERFACES

The module can support up to 3 display outputs following the standards DP++. eDP, HDMI, MIPI DSI and LVDS.

3.1 Primary Display Interface

The primary display interface can be one of the following three interface standards:

- LVDS Interface
- Embedded DisplayPort (eDP)
- MIPI DSI

3.2 Secondary Display Interface

The secondary display interface can be one of the following two interface standards:

- HDMI
- HDMI over DP++
- DP++ Interface

Note: Please check with your Module vendor for the supported modes if not described in the Module datasheet or manual. The native HDMI implementation is different from the HDMI over DP++ implementation.

3.3 Third Display Interface

The third display interface is defined as DP++ interface and therefore can support:

- HDMI over DP++
- DP++ Interface

Note: A native HDMI implementation is not supported. Please use the HDMI over DP++ implementation in the carrier.

3.4 LVDS Interface

The Module LVDS interface may be used with single or dual channel LVDS displays. The dual channel LVDS may also support the use as two single channel interfaces. The following two chapters describe the differences of the implementations.

3.4.1 NEC 1280 x 768 Single Channel LVDS Example

SMARC Modules typically support LVDS 18 bit single channel operation (three data pairs plus one clock pair). They may also support LVDS 24 bit single channel operation (four data pairs plus one clock pair). Recall that there are two 24 bit color mappings in common use: most significant color bits on fourth data pair (sometimes referred to as the standard 24 bit mapping), and least significant color bits on the fourth LVDS data pair (referred to as 24 bit / 18 bit compatible or as 24 bit / 6 bit pack or similar). The standard 24 bit color mapping is more common but is incompatible with the 18 bit packing.

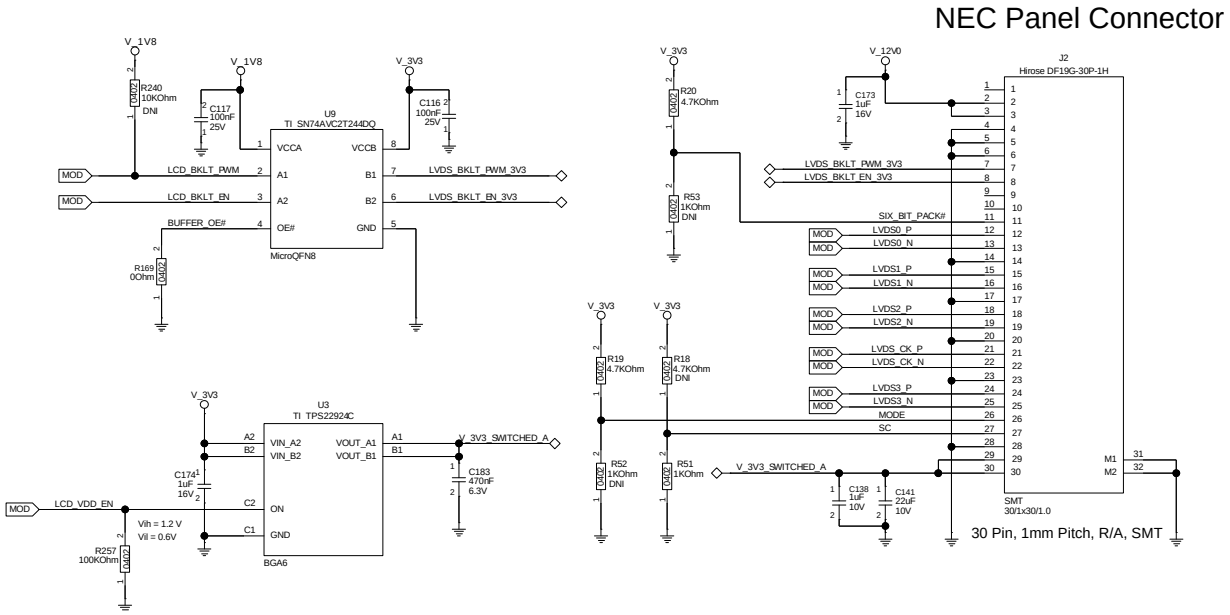
The example below shows an implementation used with an NEC 1280 x 768 single channel LVDS panel (NL 12876AC18-03). This panel uses a discrete wire 30 pin Hirose DF19 series connector. The panel

backlight electronics accepts a 12V supply, and panel brightness is controlled by a 3.3V PWM signal. There is no EDID EEPROM on this particular NEC display.

This display happens to support 18 bit, 24 bit / 18 bit compatible and standard 24 bit LVDS packings. The panel also allows the image to be reversed. This can be useful if you find the panel connector orientations to be inconvenient – you can rotate the display 180 degrees, alter the scan direction strap, and have the image appear in the correct orientation. These options are set by pull-up and pull-down choices on connector pins 11, 26 and 27 in the image below. Refer to the display data sheet for further information.

The display LVDS data and clock differential pairs may be connected directly to the SMARC Module. The backlight PWM and panel enable need level translation and / or buffering as shown in the figure.

Figure 13 Module LVDS: NEC Single Channel Display



Power for the display's logic is gated by the Module LCD_VDD_EN signal, as shown above.

The NEC LVDS display in the example above accepts a 12V feed to power the display's LED backlight. The SMARC Module provides two backlight control signals, LCD_BKLT_EN and LCD_BKLT_PWM (enable and brightness).

Some displays require a higher voltage feed to their LED backlight electronics. An example of this is given in section **9.6 High Voltage LED Supply**.

3.4.2 LVDS Dual Channel example

The schematic example below shows an implementation on the Carrier that can be used either for a dual channel LVDS display or two single channels LVDS displays with common supply voltage. The LVDS signals are routed through common mode chokes to the LVDS connector. All display signals include ESD devices. Supply voltage for LVDS display and backlight can be selected by jumper settings. The control signals for backlight, LVDS display and I2C bus are routed over level shifters from 1.8V on SMARC connector side to the display I/O voltage.

Additional comments to schematic example:

- Signal LVDS_VDDEN:

  If FET power switching is used this signal pin can also be connected to EN_PANELPOWER instead of PG_VPANEL. In this case PU resistor R15 and diode D1 can be removed.

- LVDS connector type:

  Neither connector type nor pinout of the connector underlies any standards specification. So everyone is free to select a suitable LVDS connector for best application fit.

- Comment on jumper settings:

  CN1-JP1:

  Default: JP1 shorting 1-2 => Panel supply = 3.3V

  Alternate: JP1 shorting 5-6 => Panel supply = 5.0V

  CN2-JP2:

  Default: JP2 shorting 3-4 => Backlight voltage = 12.0V

  Alternate: JP2 shorting 5-6 => Backlight voltage = 5.0V

- Comment on alternate power switching:

  If leakage currents are not considered as an issue for the design, the load switch might be replaced by a P-Channel FET and N-Channel FET for the Gate control.

- Comment on different power rails for both LVDS channels:

  It might be considered to implement different voltage rails for both channels, which is not covered with this design example.

- Comment on ESD-Devices:

  Place the ESD device close to the LVDS connector and close to the backlight pin header.

In a LVDS implementation with two single LVDS channels, the panel EDID EEPROMs would be in conflict and measures need to be taken to avoid this. One possible solution is that the second LVDS EDID EEPROM could be read over the I2C_GP pin pair rather than the I2C_LCD pin pair.

Figure 14 LVDS Dual Channel

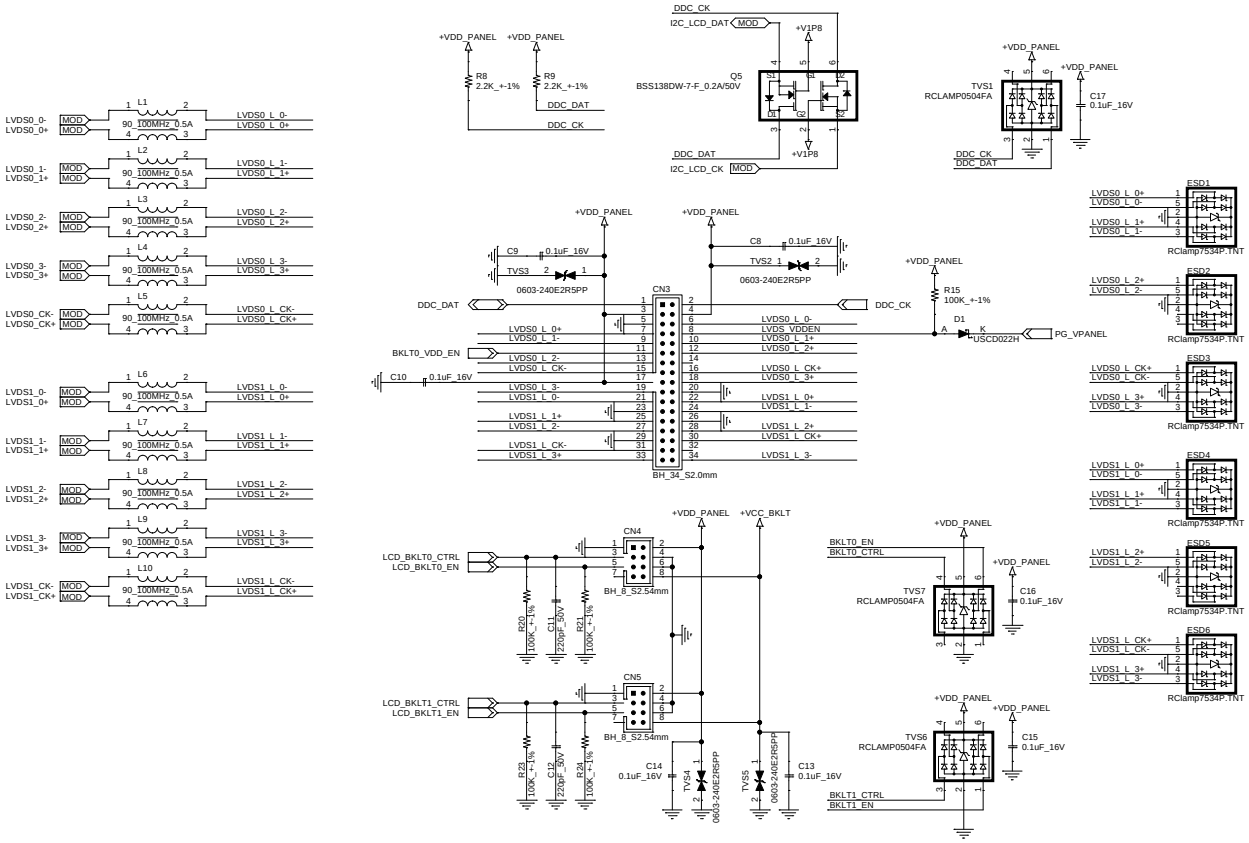
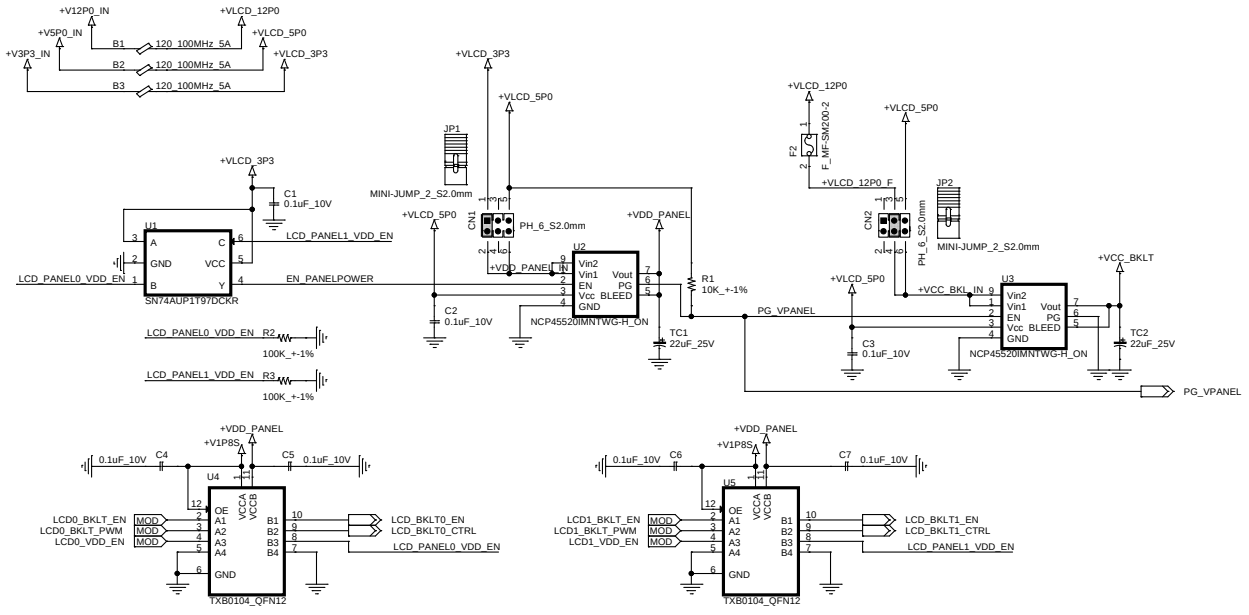


Figure 15 LVDS Dual Channel Power Supply



3.4.3 LVDS Display Parameters and EDID

Flat panel display parameters (horizontal resolution, vertical resolution, pixel clock rate, blanking periods, etc.) may be hard-coded into a boot-loader or they may be read by boot-loader code from an industry standard data structure known as EDID (Extended Display Identification Data). EDID data is stored in an EEPROM accessed via I2C. The EDID EEPROM may reside on the display assembly or elsewhere in the path between the SOC and the display – on the Carrier or on a display adapter assembly.

If the EDID EEPROM resides on the display, then the cabled interface to the display must include the SMARC Module I2C_LCD interface. The interface should be level translated and possibly buffered. The I2C voltage levels on the display are most likely to be at 3.3V levels. A set of back-to-back FETs may be used for I2C level translation, as shown in the figure immediately below. Alternatively, a device such as the Fairchild FXMA2102 I2C buffer / level translator may be used. There is a circuit example using the FXMA2102 later in this document.

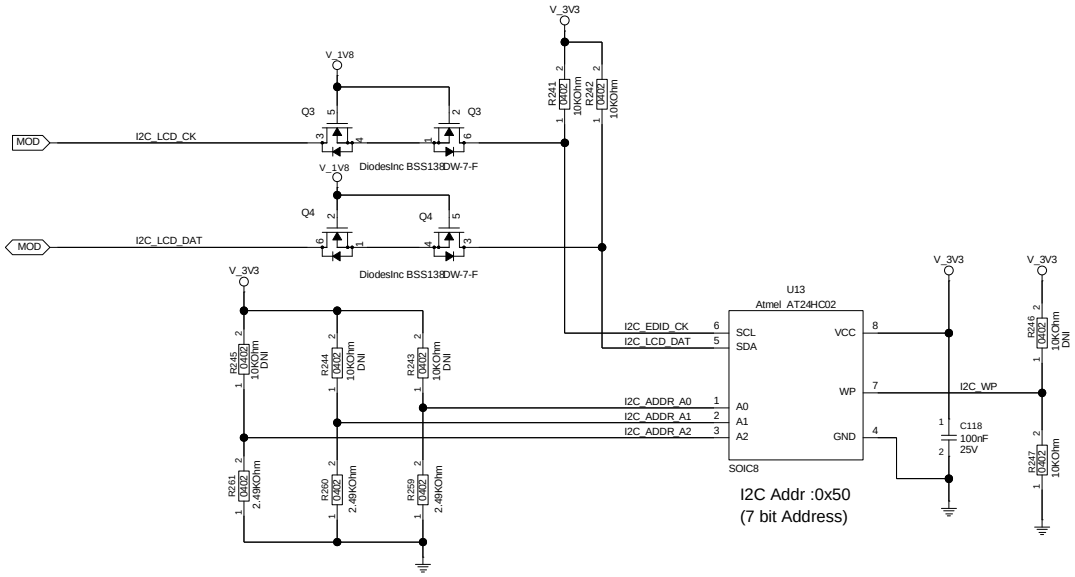
In the display interface example above, with the 30 pin Hirose DF19 series connector, pins 9 and 10 could be used for the buffered I2C_LCD clock and data, respectively.

The figure below shows an EDID EEPROM implementation that may be used on a Carrier. It might be advantageous to use a socket for the EEPROM to allow display parameters to be swapped out. Alternatively, system software could update the EEPROM if the EEPROM WP (Write Protect) pin is set to enable writes. Or, the system designer could implement an EEPROM programming header for update purposes.

Caution: If there is an EDID EEPROM on the Carrier and on the display, there will be an I2C address conflict unless one of the two is disabled or set to an alternate address. VESA EDID EEPROMs are expected at 7 bit I2C address 0x50.

There are many EDID editors available, some for free. It can be very useful to have access to one if you are trying to adapt a new panel, and if your SMARC Module software knows what to do with EDID data. Alternatively, your SMARC Module and / or Carrier vendor may well be able to help with display adaptations.

Figure 16 Carrier EDID EEPROM



3.5 Embedded DisplayPort (eDP)

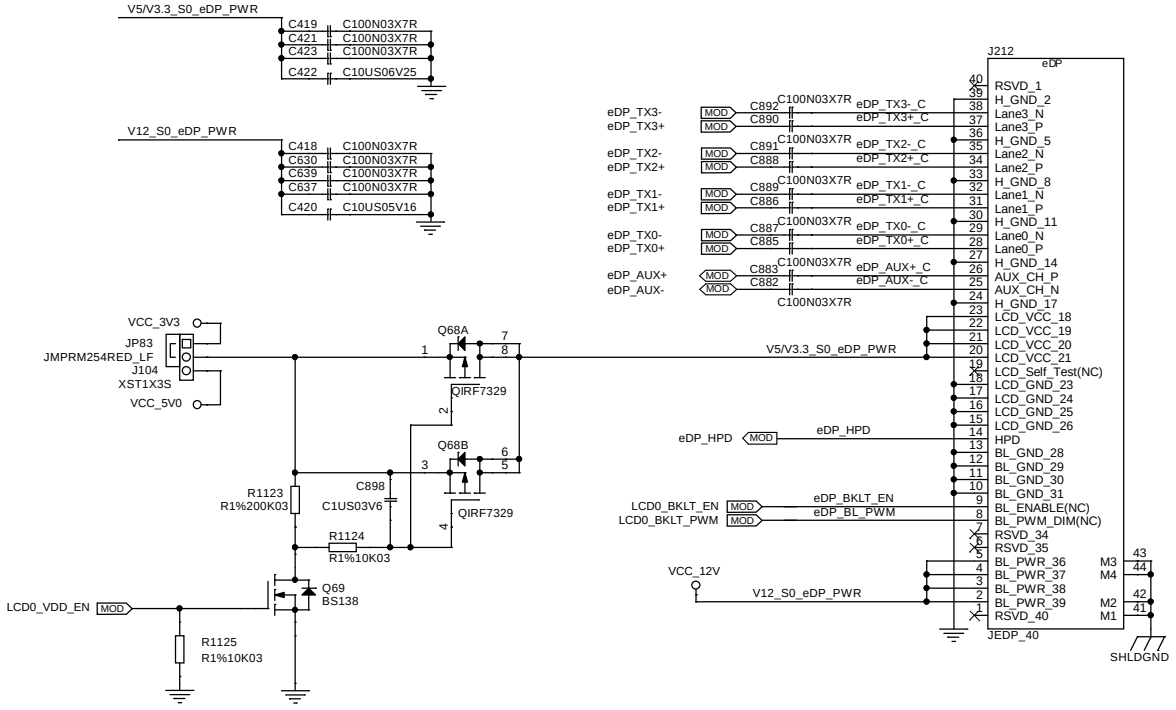
The reference schematic provides a generic eDP interface. The eDP connector used in the design is an example only. Other connectors can be used based on the design requirements. JP83 selects 3.3 or 5V for the panel power. R1125 ensures that panel power is disabled when the Module is powering up and before the signal is actively driven. The panel control signals eDP_BKLT_EN, eDP_BKLT_CTRL as well as eDP_HPD are 3.3V level signals, check your panel specifications for correct voltage levels and provide translation if necessary. The reference design supports individual backlight control signals. It should be noted that some panels handle these functions over the AUX channel.

The traces from JP83 and associated FETs to the eDP connector carry power to the panel. The traces should be routed with appropriate thickness to handle the current expected.

eDP_TX[0:3] and eDP_AUX differential pairs should be routed as high speed differential pairs.

The panel control signals are low speed and do not require any additional care.

Figure 17 Embedded DisplayPort (eDP)



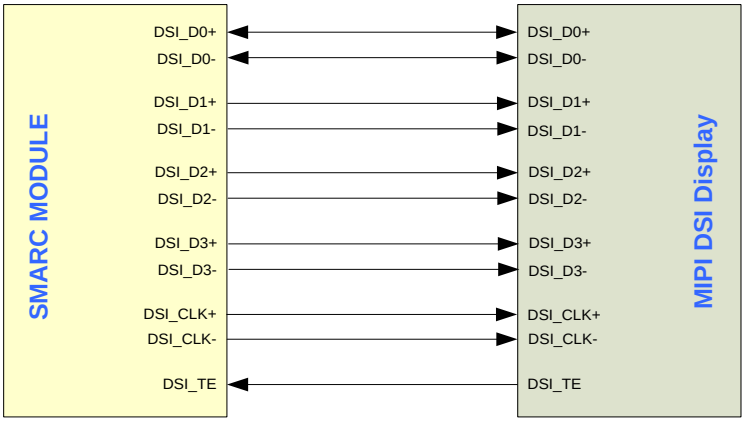
3.6 MIPI DSI

The LVDS signal lines may alternatively be used to support up to two MIPI DSI (Display Serial Interface) displays. DSI is a high-speed differential bus and includes one clock lane and up to four data lanes. There is no AC coupling required.

VDD and Backlight signals are the same is in LVDS mode.

It is recommended to check with your SMARC Module vendor if MIPI DSI is supported by the used SMARC Module.

Figure 18 MIPI DSI



3.7 HDMI

Note: A license may be needed to market HDMI capable products. Check with the HDMI organization (**www.hdmi.org**) and with your SMARC Module vendor.

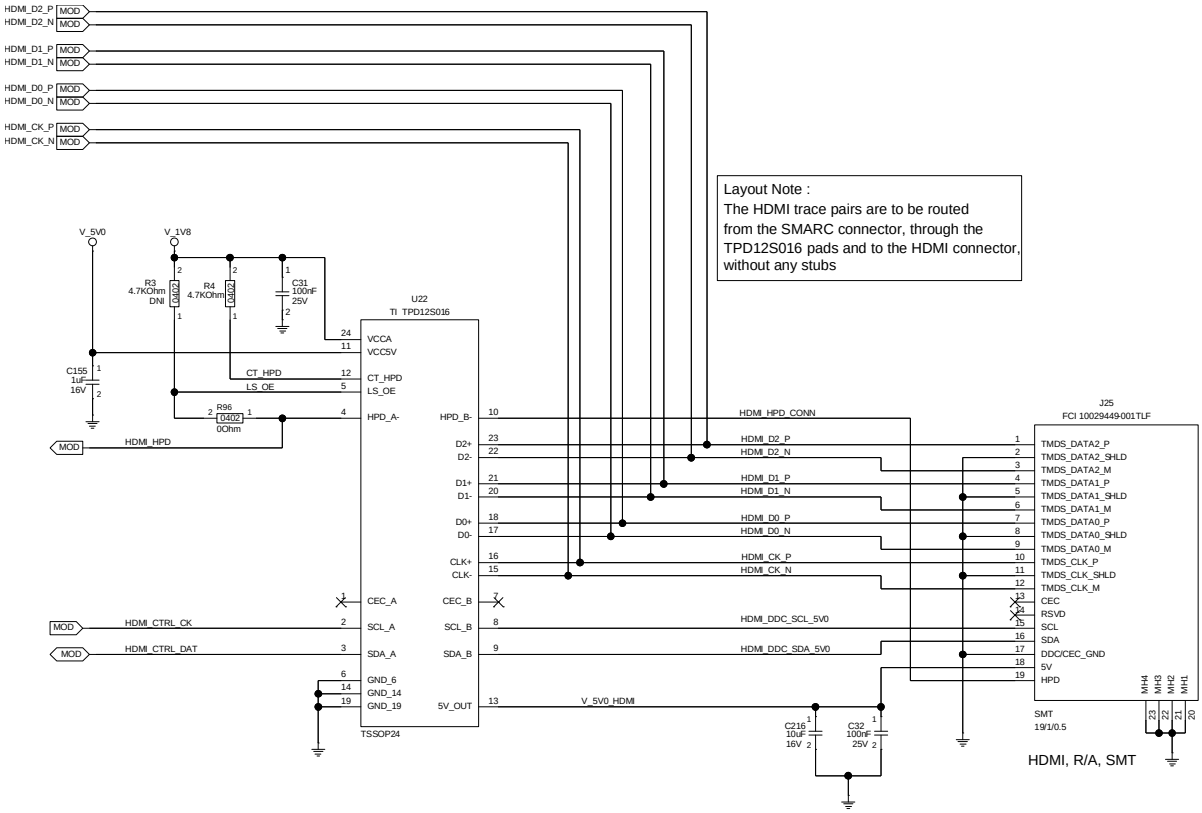
Note: Please refer to **3.8.2 HDMI over DP++** when creating an HDMI port from a DP++ interface. Please check the Module documentation or check with your SMARC Module vendor.

The SMARC HDMI data pairs may be routed directly from the SMARC Module pins to a suitable Carrier HDMI connector. Since HDMI is a hot-plug capable interface, it is important for the Carrier to implement ESD protection on all of the HDMI lines. The ESD protection on the data lines must be low capacitance so as not to degrade high speed signaling. The data lines must route through the ESD protection device pins in a no-stub fashion. The ESD protection should be located close to the HDMI connector.

The SMARC pins HDMI_CTRL_CK and HDMI_CTRL_DAT require level translation from V_1V8 to the 5V levels that HDMI uses on those pins. These lines also require pull-up resistors to V_1V8 (the pull-ups are not included on the SMARC Module, because integrated HDMI protection devices such as the Texas Instruments TPD12S016 include the pull-ups in their parts). And, finally, 5V power switching / current limiting to the HDMI connector is required on the Carrier.

The ESD protection, level translation and power switching / limiting are all dealt with in integrated devices such as the TI TPD12S016. A circuit diagram is shown in the following figure. The TPD12S016 must be placed close to the HDMI connector, and the HDMI data traces routed in daisy chain fashion (and as differential pairs) from the SMARC Module pins, to and through the TPD12S016 pins, and on to the HDMI connector pins. The TPD12S016 pin-out is specifically designed to facilitate this.

Figure 19 HDMI Implementation



3.8 DP++ Interface

The DP++ interface can be either used as DP or HDMI interface. It also allows the use of DP++ to HDMI dongles.

3.8.1 DP over DP++

DisplayPort is directly supported by a dual-source DDI. ESD protection, DC blocking capacitors and hot plug detect are the only components required.

The DisplayPort differential data pairs (Lane [0..3]) are AC coupled off Module with capacitors C19-C26. Place the AC blocking capacitors close to the DisplayPort connector. The Aux differential pair is AC coupled on the Module. ESD clamping diodes D1, D2 and D3 protect the Module from external ESD events and should be placed near the DisplayPort connector. The pin-out of the ESD clamp diodes allows for a trace to run under the chip connector to two pins.

The Carrier provides up to 500 mA of 3.3V power to the DisplayPort connector. Diode D71 prevents back feeding of power in the event that the monitor is powered up when the Carrier is powered down.

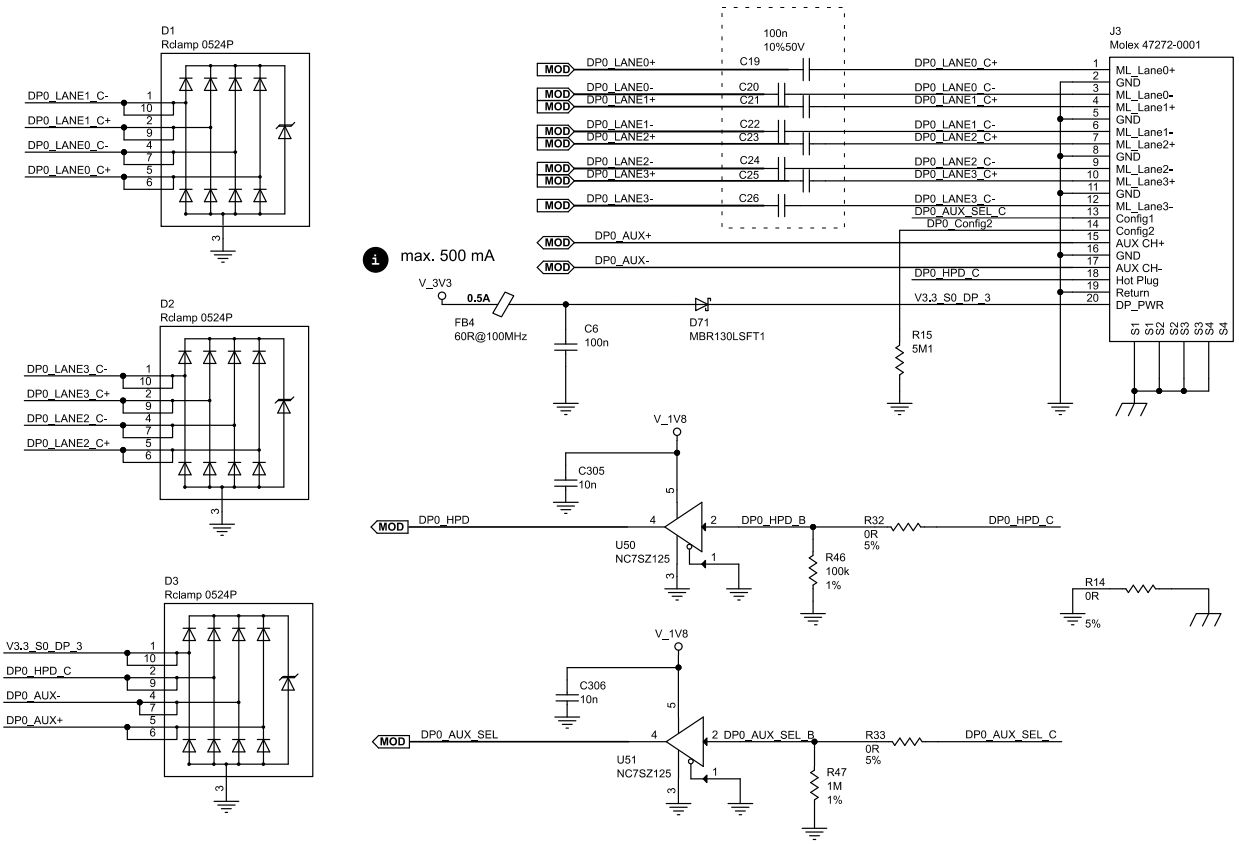
Config lines 1 and 2 are pulled to ground per the VESA specification.

The DisplayPort Hot Plug Detect signal is buffered by U50 which prevents back feeding of power from the display to the Module as well as level translation to 3.3V levels.

R14 connect logic and chassis ground together. Other techniques may be used depending on the overall grounding strategy.

Note: The reference schematics assume that the Module's DisplayPort is dual-source capable – dual source indicates that the Module can output DisplayPort or HDMI/DVI based on the DDC_AUX_SEL signal.

Figure 20 DisplayPort ++



3.8.2 HDMI over DP++

A Dual-mode source Module requires level shifters on the Carrier to convert the low-swing AC coupled differential pairs from the video source to HDMI compliant current mode differential outputs. The example schematics use a Chrontel CH7318C translator which supports data rates up to 1.65GB/s per lane. FET based passive level translators can be used for lower data rates.

The DisplayPort AUX channel is configured as a DDC interface for HDMI. Further information on pre-emphasis as well as output current trim capabilities of the CH7318C can be found in the Chrontel datasheet.

ESD clamping diodes D159, D160 and D161 protect the Module from external ESD events and should be placed near the HDMI connector. The pin-out of the ESD clamp diodes allows for a trace to run under the chip connector to two pins.

HDMI uses I2C signaling for the DDC. Resistors R1319 and R1322 provide the necessary pull-up.

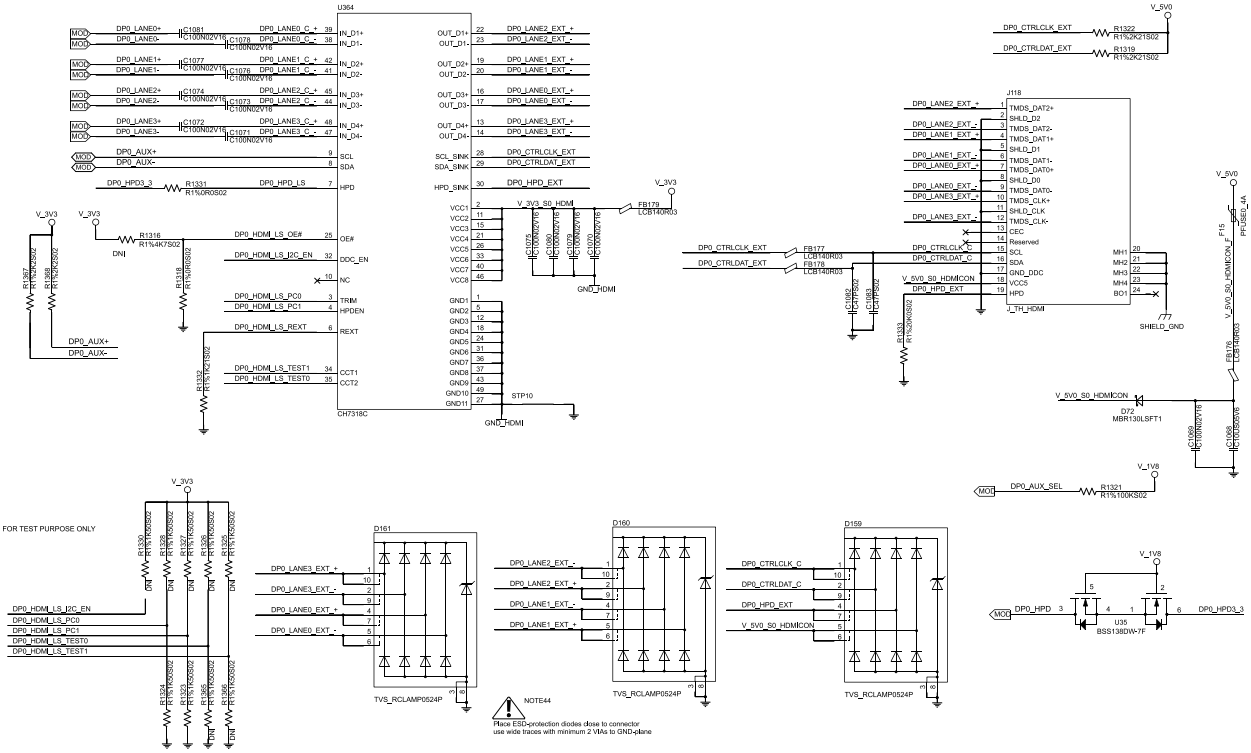
The FET U35 provides the Hot Plug Detect signal

The Carrier provides 5V power to the HDMI connector. A series diode (D72) should be used to prevent back feeding of power in the event that the monitor is powered up when the Carrier is powered down.

The HDMI Hot Plug Detect signal is buffered by two FETs U32 and U33 which prevent back feeding of power from the display to the Module as well as level translation to 3.3V levels.

Note: The reference schematics assumes that the Module's DDI ports are dual-source capable – dual source indicates that the Module can output DisplayPort or HDMI/DVI based on the DDC_AUX_SEL signal.

Figure 21 HDMI over DP++



4 Low / Medium Speed Serial I/O Interfaces

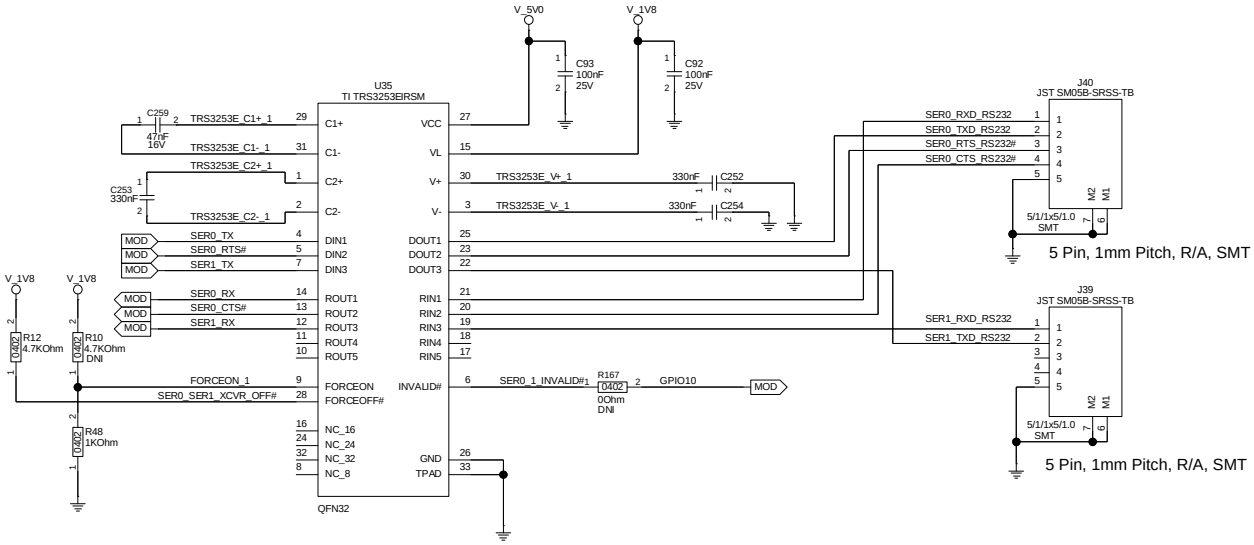
4.1 Asynchronous Serial Ports

The SMARC Module asynchronous serial ports run at 1.8V logic levels. The transmit and receive data lines from and to the Module are active high, and the handshake lines are active low, per industry convention.

4.1.1 RS232 Ports

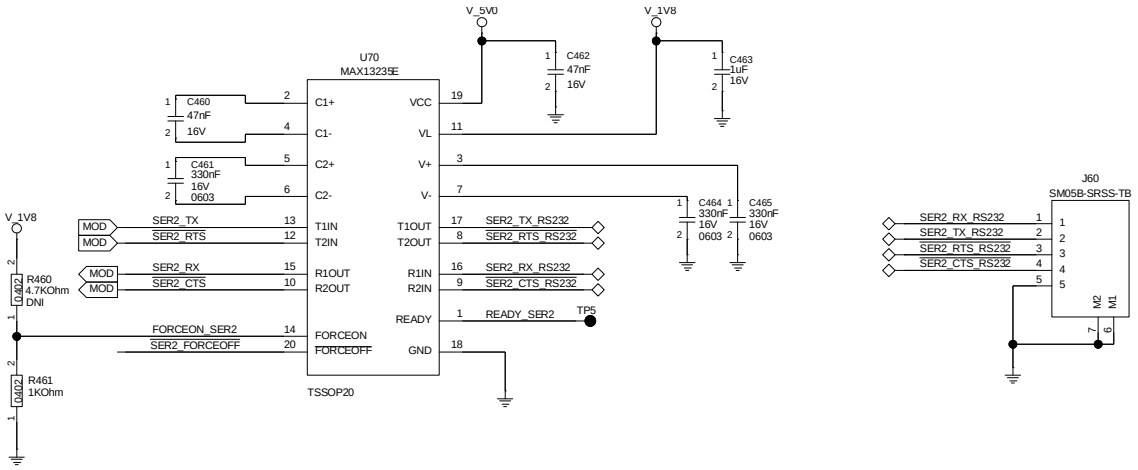
If the asynchronous ports are to interface with RS232 level devices, then a RS-232 transceiver is required on the Carrier board. The logic side of the transceiver must be able to run at 1.8V levels. The selection of 1.8V compatible transceivers is a bit limited, although more are appearing with time. Two such devices are the Texas Instruments TRS3253E, and the Maxim MAX13235E, illustrated in the figures below. The TI part is more cost effective, but has a top speed of 1 Mbps. The MAX13235E can operate at maximum speeds over 3 Mbps (but your SMARC Module may or may not - check with your Module vendor). The transceivers invert the polarity of the incoming and outgoing data and handshake lines.

Figure 22 Asynchronous Serial Port Transceiver – RS232 – TRS3253E



Pin 6 of U35 (INVALID#) may be connected to a GPIO of the SMARC Module (GPIO10 in this example) but it has to be checked if this GPIO is not needed for another function.

Figure 23 Asynchronous Serial Port Transceiver – RS232 – MAX13235E



4.1.2 RS485 Half Duplex

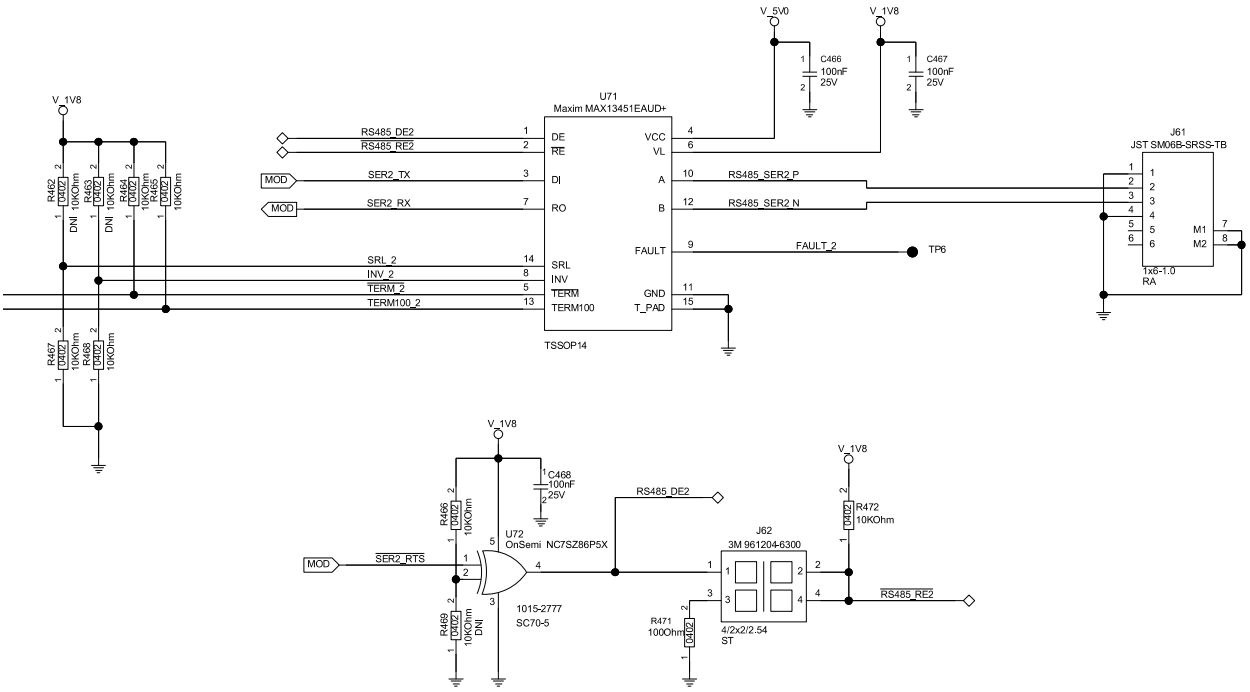
A half-duplex RS485 asynchronous serial port implementation is shown below. This hardware implementation is suitable for multi-drop RS485 networks. The Maxim MAX13451E transceiver accepts 1.8V logic I/O and has other, flexible features of interest such as internal termination options.

Multi-drop RS485 nodes should be strung together in daisy chain fashion using shielded twisted pair cable with a defined differential impedance (usually 120 ohms; sometimes 100 ohm cables are used). The two end-points of the system should be resistively terminated across the pair. The termination value should equal the differential impedance of the twisted pair cable used. The Maxim transceiver allows the termination to be enabled or disabled on the TERM# pin, and can be selected to be 100 ohms or 120 ohms via the TERM100 pin state. These pins can be controlled by Carrier GPIOs if desired.

The RS485 driver is enabled when the SMARC SER2_RTS# signal is asserted low (if the resistor options in front of the XOR gate are loaded as shown, such that the XOR gate inverts the SER2_RTS2# signal for the RS485_DE2 function).

A suitable, likely application specific, software driver is required to make the multi-drop RS485 network work.

Figure 24 Asynchronous Serial Port Transceiver - RS485 – Half Duplex



Jumper 01-02	Jumper 03-04	State
Open	Open	RS485 receiver disabled
Open	Closed	RS485 receiver always enabled
Closed	Open	RS485 receiver enbled when transmitter disabled
Closed	Closed	Invalid

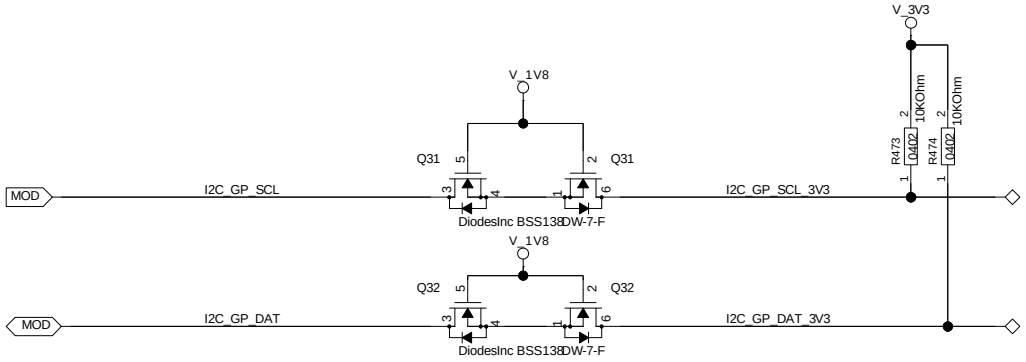
4.2 I2C Interfaces

The I2C bus is a versatile low bandwidth multi-drop bus originally defined by Philips (now NXP). It is a two wire bus (clock and data) that relies on the use of open-drain drivers and passive pull-ups. The bus can be single master or multi-master. SMARC Modules are always I2C masters. Whether or not they allow other masters is Module implementation dependent. Most SMARC systems use the I2C bus as a way for the SMARC I2C Masters to interface to a variety of I2C Slave peripherals. The standard I2C interface operation speeds are 100 kHz and 400 kHz. Some implementations allow faster speeds.

4.2.1 I2C Level Translation, Isolation and Buffering

FETs may be used to perform I2C level translation, as shown in Figure 25 I2C Power Domain Isolation – using FETs. This arrangement provides no buffering. It can provide isolation to prevent one side of the bus dragging down the other if one of the rails is collapsed. The rail that is to collapse should be the rail driving the FET gates.

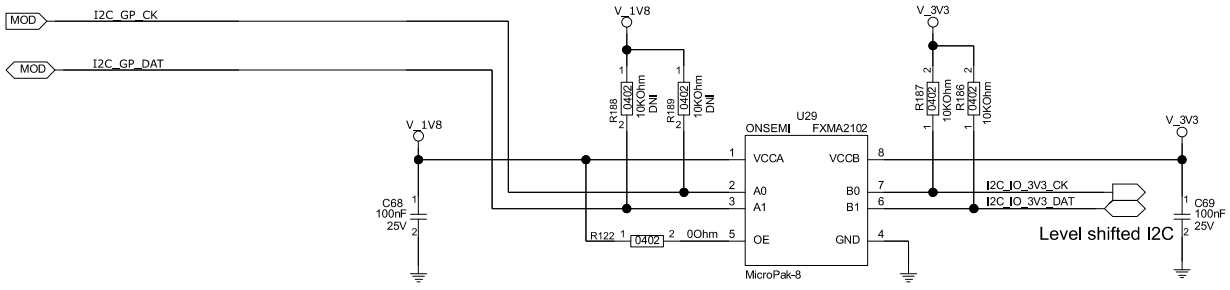
Figure 25 I2C Power Domain Isolation – using FETs



The circuit shown in Figure 26 I2C Power Domain Isolation and Buffer – ONSEMI FXMA2102 can provide power domain isolation, voltage level shifting and I2C bus buffering. The ONSEMI FXMA2102 power rails VCCA and VCCB can be at the same voltage level or at different levels, over a range of 1.65V to 5.5V. Either rail can come up before the other.

If you have many I2C devices, it is a good idea to split them up into segments with up to about 6 devices on each segment and isolate the segments with a bi-directional I2C buffer such as the FXMA2102. I2C bus performance degrades with too much capacitive loading.

Figure 26 I2C Power Domain Isolation and Buffer – ONSEMI FXMA2102



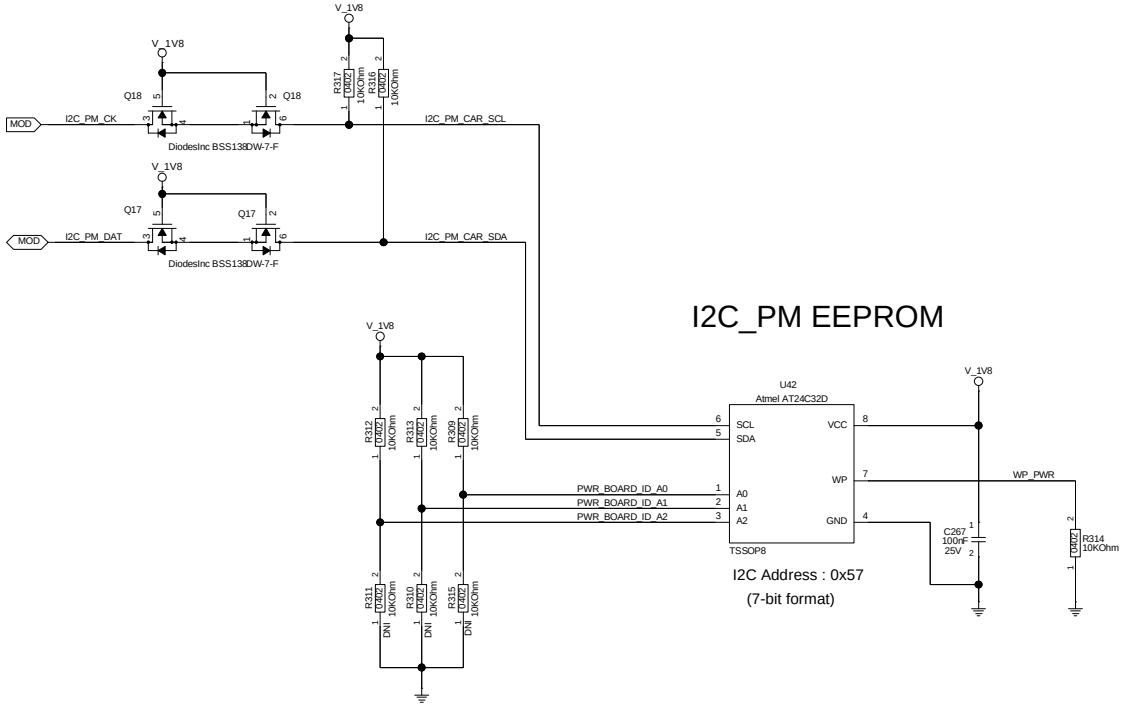
4.2.2 I2C_PM Bus EEPROMs

The SMARC I2C_PM bus is special in that it is used on the Module for power management functions, and it always runs from a 1.8V rail on the Module. The 1.8V voltage rail requirement on the I2C_PM bus allows it to be powered from a simple, low quiescent current linear or buck switching regulator from V_MOD_IN.

On the Module, since it is used for power management, it is “on” even when the Carrier power may be off (i.e. the CARRIER_PW_ON signal may be low, and Carrier circuits that are not involved in power management are powered off).

If the I2C_PM bus is used on the Carrier for functions that are not power management functions, then it needs to be isolated from the Module by a set of back to back FETs, as shown in the Figure 27 I2C_PM EEPROM: Carrier Power Domain. The V_1V8 in the figure is a Carrier board power rail that may be collapsed; the Module side of the I2C_PM must not be dragged down.

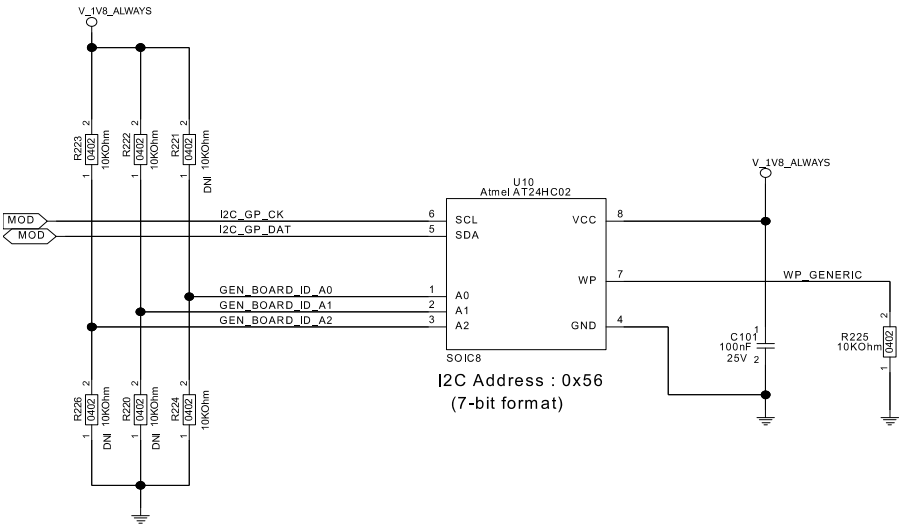
Figure 27 I2C_PM EEPROM: Carrier Power Domain



The SMARC I2C_PM bus may be used on the Carrier for power management functions, such as interfacing to a battery charger or battery fuel gauge. In this case, the power circuits and the I2C_PM interface to the SMARC Module need to be powered whenever power is on.

A local low quiescent current low drop out linear regulator is needed to provide 1.8V for the Carrier board “Module domain” devices.

Figure 28 I2C_PM EEPROM: Module Power Domain

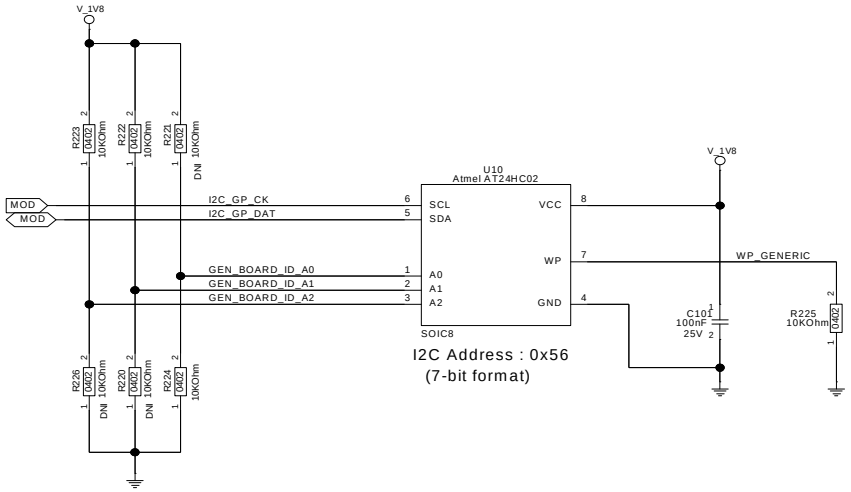


The SMARC Module specification recommends - but does not require - that Carriers have a parameter EEPROM on the I2C_PM bus, preferably configured as shown here, in the “Module Power Domain”. This, in principle, allows the Module to query the Carrier I2C_PM EEPROM before asserting the CARRIER_PWR_ON signal that enables the main Carrier board power feed.

4.2.3 General I2C Bus EEPROMs

The other SMARC I2C buses (I2C_LCD, I2C_GP, I2C_CAM) operate at 1.8V. The power domain isolations described in the previous section do not apply. A simple sample EEPROM circuit is shown in Figure 29 I2C_GP EEPROM for reference.

Figure 29 I2C_GP EEPROM

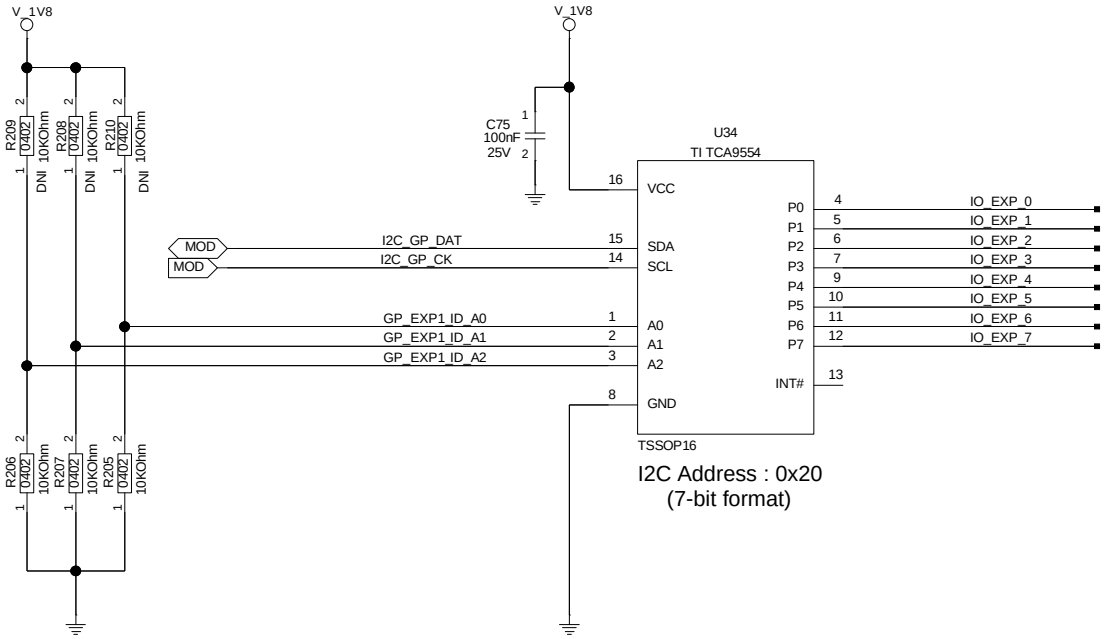


4.2.4 I2C Based I/O Expanders

I2C based “I/O Expanders” are available from Texas Instruments, NXP and others. Multiple expanders may be put onto the same I2C bus by configuring the I/O expander I2C address straps. These devices are an easy and cost effective way to realize additional I/O on SMARC systems.

On the device shown in Figure 30 I2C Device: I/O Expander, the I/O ports on the right are all in a high impedance “tri-state” mode when the device powers up. This allows the designer to tie the I/O lines through resistor pull-ups or pull-downs to define a power up state for these lines, before the I2C interface and before software are active. Wider (x16) devices are also available.

Figure 30 I2C Device: I/O Expander



4.2.5 Other I2C Devices

There is a very wide variety of I2C peripherals available on the market. Since SMARC Modules offer up to four I2C buses (not counting the HDMI private I2C bus), it is easy to incorporate I2C devices into a SMARC system. A few schematic examples are given here, and further suggestions are listed in the table at the end of this section.

Figure 31 I2C Device: Accelerometer

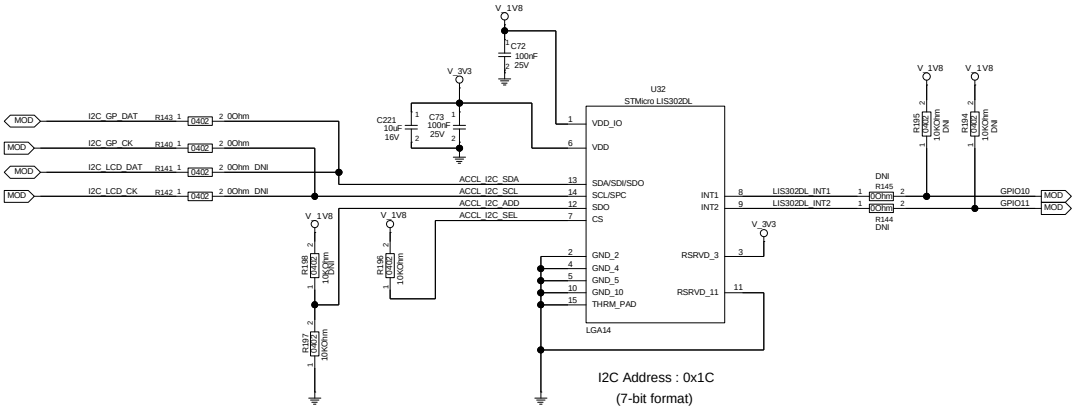


Figure 32 I2C Device: Accelerometer and Magnetometer

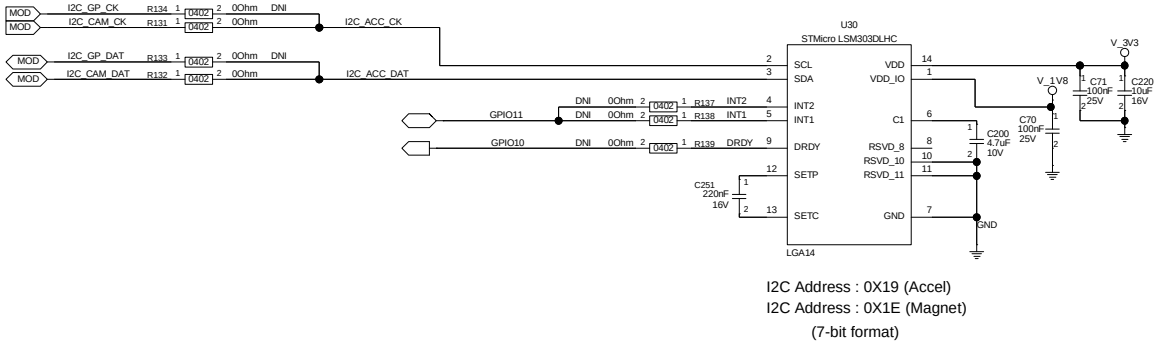
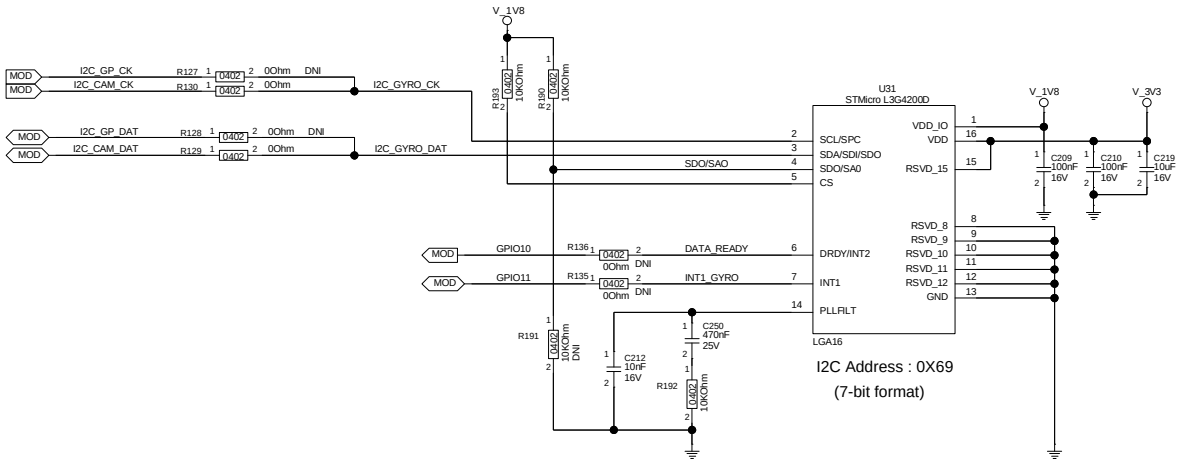


Figure 33 I2C Device: Gyroscope



The table below gives a small sampling of other 1.8V I/O I2C devices that are available. The list is meant to just give the reader an idea of what types of devices are available.

Table 3 I2C Device Examples - 1.8V I/O

Function	Device Description	Vendor	Vendor P/N
ADC	8-channel, 12-bit SAR ADC with temperature sensor	Analog Devices	AD7291
DAC	Quad, 16-bit DAC	Analog Devices	AD5696R
LED driver	7-bit LED driver with intensity control	Texas Instruments	TCA6507
Proximity / Button sensor	Four Channels, Capacitive Proximity/Button Solution	Semtech	SX9500
Temperature Sensor	Temperature Monitor, ±1° C	On Semiconductor	NCT72
UART	128 Word FIFOs	Maxim Integrated	MAX3108

4.3 Touch Screen Controller Interfaces

The two most popular touch technologies used with SMARC systems are summarized in the following table.

Table 4 Popular Touch Technologies

Technology	Notes
Resistive	Low cost; rugged. Display clarity and contrast may be compromised by the resistive touch overlay. Usually used with a stylus but may be used with bare fingers. Multi-touch is possible but not common. More straightforward to implement than capacitive touch.
Projected Capacitive	Higher cost, higher barrier to entry and better quality and user experience than resistive touch. Multi-touch capable. Excellent optics.

There are many other touch technologies, some better suited to certain situations such as user's wearing gloves and so on. An overview may be found on the EloTouch website: **www.elotouch.com** under "Touchscreens".

4.3.1 Interface Types / Driver Considerations

Various host interface types are used by touch screen controllers. A given controller may implement one or more of the following interfaces: USB client, I2C, asynchronous serial port, I2S, SPI, or other interface.

USB interfaces for touch screen controllers are attractive as there is the potential that the software effort is minimal: the touch screen controller may act as a USB HID (Human Interface Device) class device, and the operating system at hand may be able to understand the generic touch HID implementation directly. However, for more advanced touch implementations, such as multi-touch (the ability to track and decipher multiple, simultaneous touch hits on a screen), a more specialized driver is usually necessary. The driver is often touch controller vendor specific. Additionally, a touch controller vendor may offer multiple hardware interfaces, but the driver may be optimized for one particular hardware interface. The conclusion is: check out the software driver situation before going down a particular hardware path.

4.3.2 Touch Controller Modules / ICs / Screens

Table 5 Touch Controller Module / IC / Screen Vendors

Vendor	Notes	Web Link
Microchip (formerly Atmel)	Key vendor of touch screen controller ICs for projected capacitive screens. Microchip is a silicon vendor, and generally will not help directly with touch screen integration issues, unless your company is a Tier 1 company. Microchip has a network of partners that they will steer you to for help with integration issues. Some of the partners from Microchip's list are included in this table.	**www.microchip.com**
Data Modul	Selection of touch screen panels, overlays and controller modules for projective capacitive technology and for resistive touch screens. Company is based in Germany and has a presence in the USA. Products are marketed under the "Easy Touch" trade mark.	**www.data-modul.com**
EloTouch	Elo offers a variety of finished touch panels. They also offer a popular controller chip for resistive touch panels, under the marketing name "AccuTouch COACh V Controller Chip".	**www.elotouch.com**
Pixcir	Vendor of controller ICs for projected capacitive screens. Based in China and in Switzerland.	**www.pixcir.com**
Precision Design Associates	Touch modules and touch overlay screens. Based in Marietta, Georgia, USA.	**www.pdaatl.com**
Touch International	Touch overlays, modules and integration services. One of the larger and better known companies in this field. Based in the state Texas, USA. The Touch International website has an overview of various touch technologies.	**www.touchinternational.com**
MSC Technologies	Vendor of its own product group of Touch Screen Panels, Overlays and Controller Cards for PCAP (Projected Capacitive) Touch Technology; also offers other touch technologies, TFT panels and display systems. MSC has its own sales presence in Central Europe and is marketed by Avnet / Avnet Embedded in all other countries of the world.	**www.msc-technologies.eu**

Also check with your SMARC Module vendor or your SMARC Carrier design partner – some of them have in-house solutions for particular display panels.

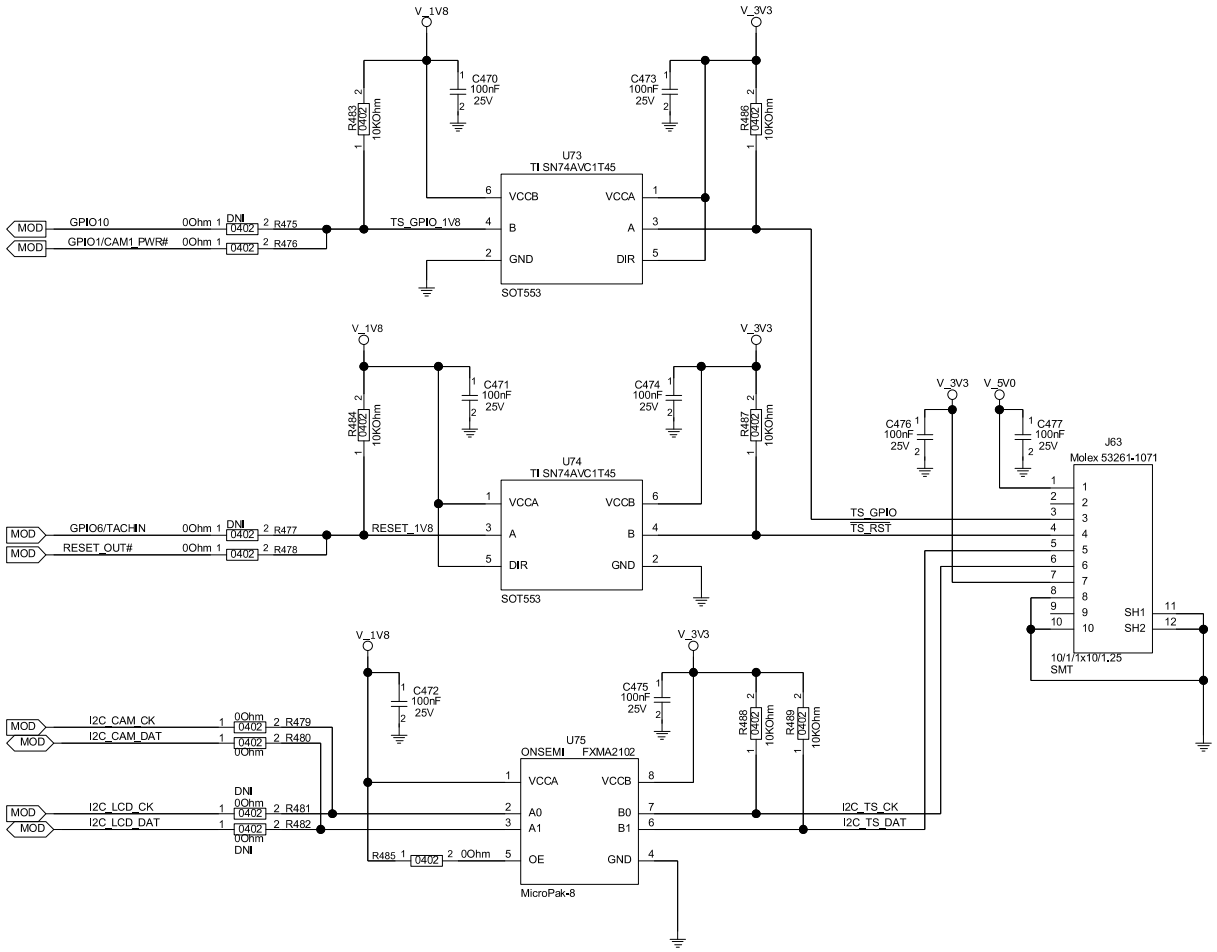
Also remember to consider the availability of software drivers for the choices that you are making.

4.3.3 I2C Interface to Touch Controller

Atmel is a popular choice for projected capacitance touch controllers. Atmel supplies USB and I2C drivers for the mXT1664S touch screen controller. Multi-touch is supported in the I2C driver but not, as of this writing apparently, in the USB driver.

The circuit shown in **Figure 34 Touch Screen Connector – I2C Interface** provides buffering and level translation for a SMARC interface to an I2C interfaced touch controller board. The Atmel mXT1664S can be configured for 1.8V I2C operation, and hence this voltage translation may not be necessary in a custom design. However, off-the-shelf touch controller modules may not be configured for 1.8V I/O (and the particular touch module behind this example was not). In any case, some buffering when cabling to an external board is not a bad thing to have, for robustness.

Figure 34 Touch Screen Connector – I2C Interface



4.4 I2S Interfaces

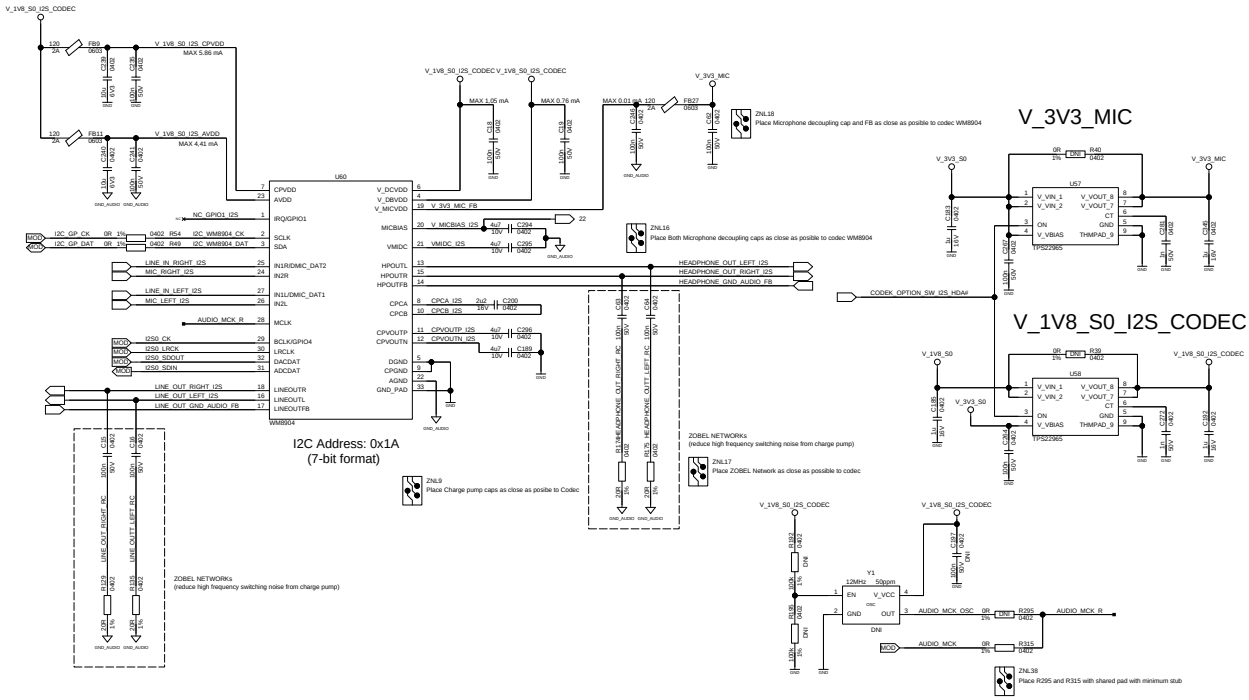
The I2S (Inter IC Sound) bus specification was initially released in 1986 by Philips (NXP) and later revised in 1996. I2S is a synchronous serial bus used for interfacing digital audio devices such as Audio CODECs and DSP chips. Generally, PCM audio data is transmitted over the I2S interface. The I2S bus may have a single bidirectional data line or two separate data lines. The signals constituting the I2S bus are a serial clock/ bit clock (output from the master), a left right clock (output from the master) that indicates the channel being transmitted and a single bidirectional data line or two data lines - one input and one output. A SMARC Module can generally be configured as I2S master or slave. SMARC Modules may support up to two independent I2S interfaces each having separate input and output data lines.

4.4.1 Cirrus Logic I2S Audio Example

An example of an I2S based audio circuit using the Cirrus Logic WM8904 CODEC is given in Figure 35 I2S Audio Codec Cirrus Logic WM8904.

The circuit uses a SMARC I2S interface for the audio PCM data, and a SMARC I2C interface to allow a path for software setup of registers within the CODEC.

Figure 35 I2S Audio Codec Cirrus Logic WM8904



4.4.2 Texas Instruments TLV320AIC3105 I2S Audio Example

An alternative I2S audio CODEC example from TI is shown in Figure 36 I2S Audio CODEC: Texas Instruments below. As in the WM8904 example, the I2S carries the PCM audio from and to the SMARC Module, and the I2C is used for chip setup parameters.

Figure 36 I2S Audio CODEC: Texas Instruments

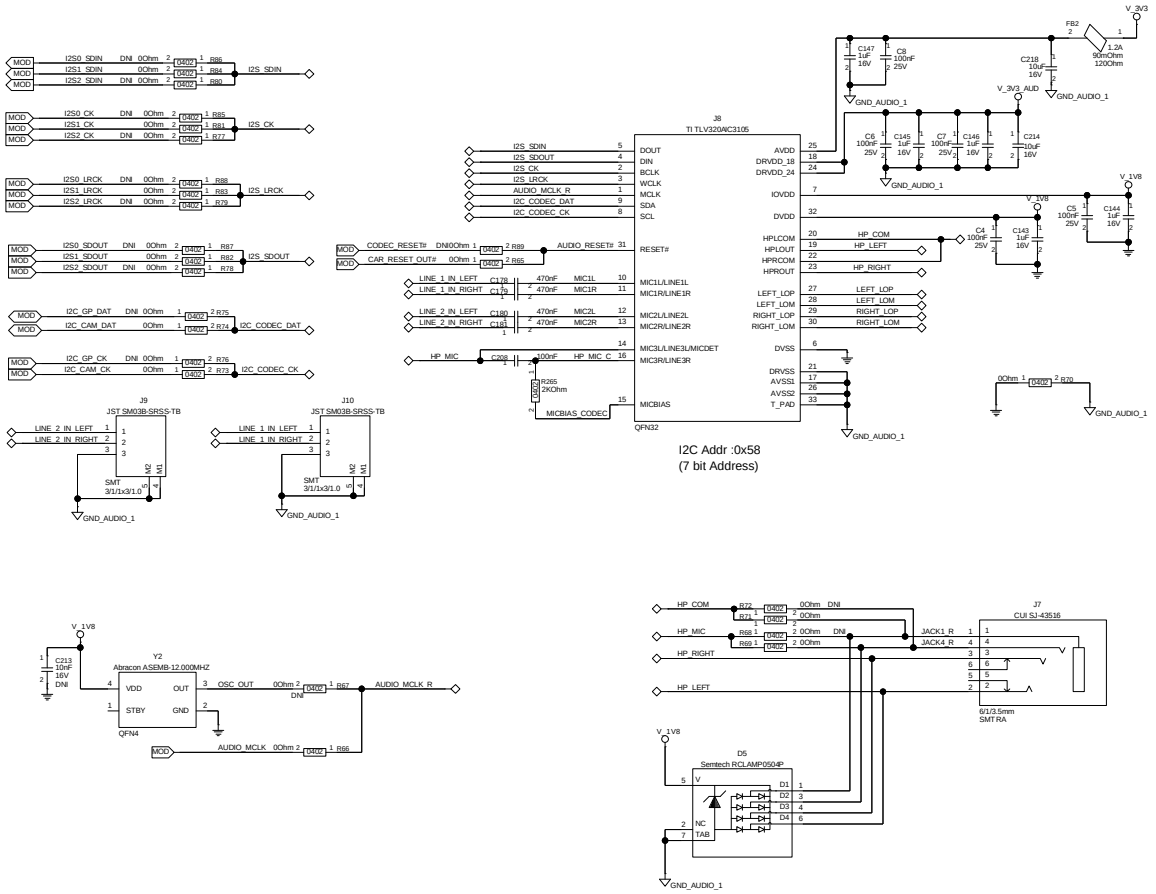
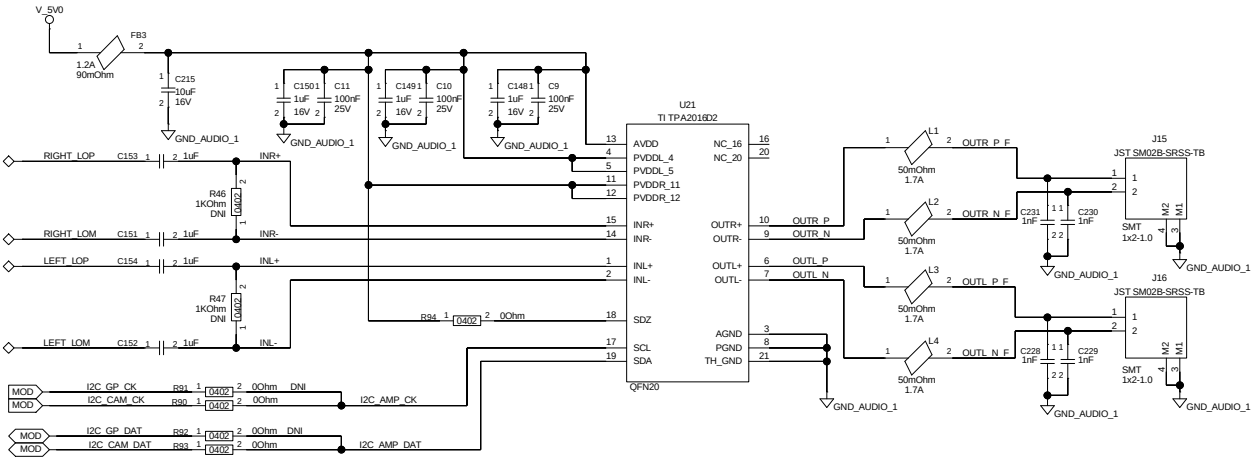


Figure 37 Audio Amplifier: Texas Instruments



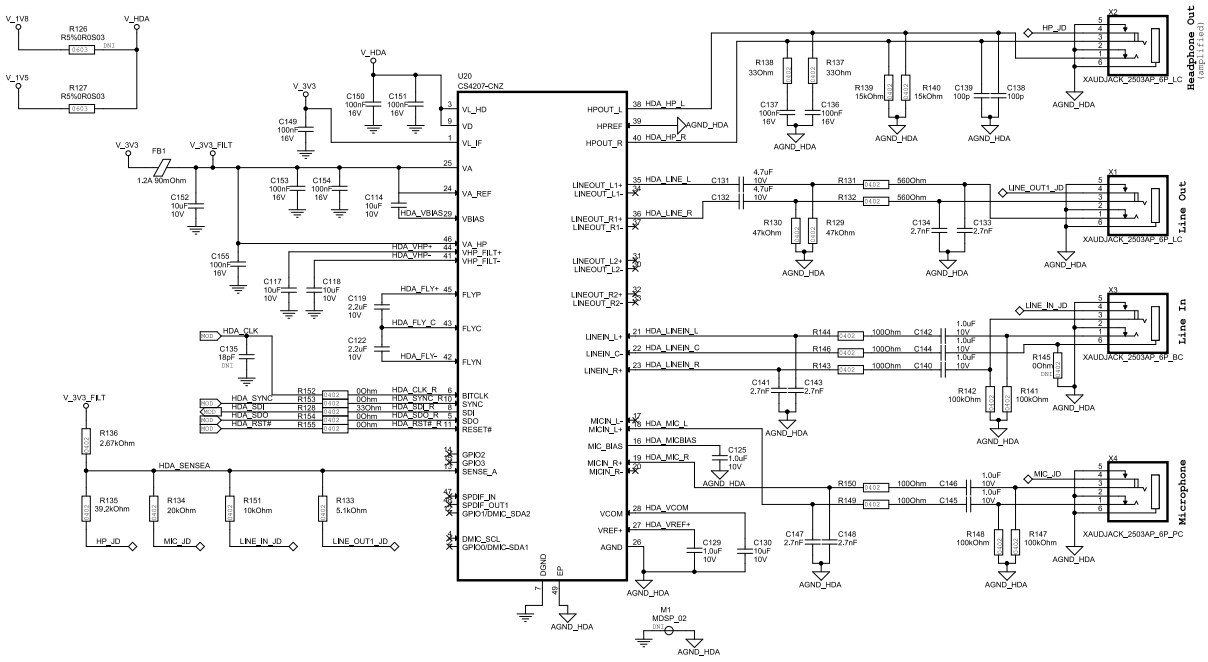
4.4.3 Intel High Definition Audio over I2S2

The HDA interface uses the same pins as I2S2 in SMARC 2.0 specification. At the time of writing HDA is still the preferred Audio Interface for x86 based Modules, even though I2S is getting integrated in the latest x86 SoC generations. There's a minor conflict with regards to voltage levels of the shared HDA and I2S audio interfaces. SMARC defines the I/O levels of HDA to be 1.5V to comply with the HDA specification. Nevertheless, there's a trend to run the HDA interface at 1.8V in order to save cost for additional voltage regulators. Most of chip vendors as well as codec vendors allow either voltage to be used. Please check with your Module vendor if 1.5V or 1.8V are supported and use an audio codec that is capable to support the regarding I/O voltage.

The example schematic shows a simple resistor option (R126 and R127) to support both I/O levels within one design. HDA_SDI signal should have a damping resistor close to the audio codec. It's a good practice to also reserve space for series damping resistors at the other HDA interface lines.

Depending on the Carrier board implementation it might be useful to also apply series resistors there to improve EMI and signal integrity.

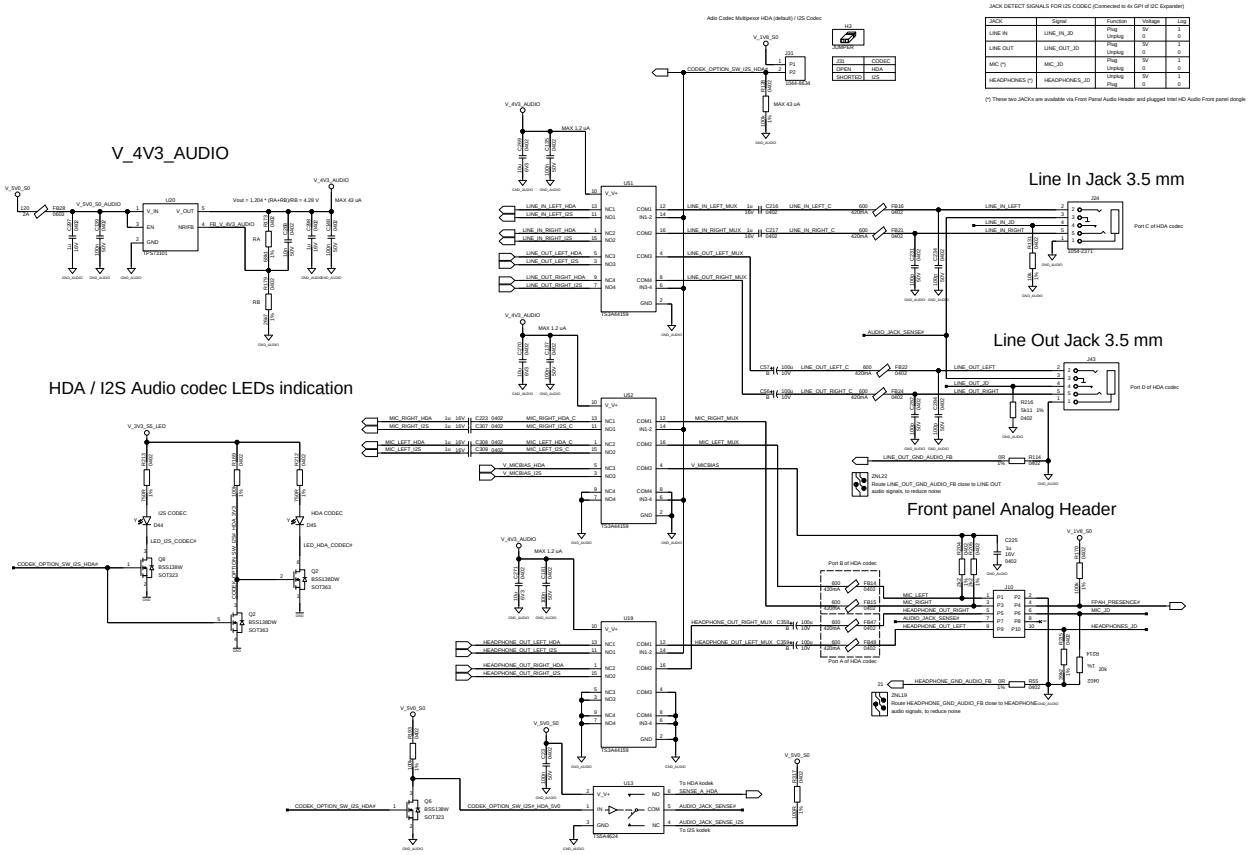
Figure 38 HD Audio



4.4.4 Audio Switch

The following schematic in Figure 39 Audio switch shows an audio switch. This can be used on Carrier boards which have both codecs I2S and HD Audio to switch between the two of them.

Figure 39 Audio switch



4.5 SPI Interfaces

The SPI (Serial Peripheral Interface) is a full duplex synchronous bus supporting a single master and multiple slave devices. The SPI bus consists of a serial clock line (generated by the master); data output line from the master; a data input line to the master and one or more active low chip select signals (output from the master).

Clock frequencies from 1-100MHz may be generated by the master depending on the maximum frequency supported by the components in the system. SMARC Modules running a 1.8V I/O interface are generally limited to about a 50 MHz clock rate on this interface.

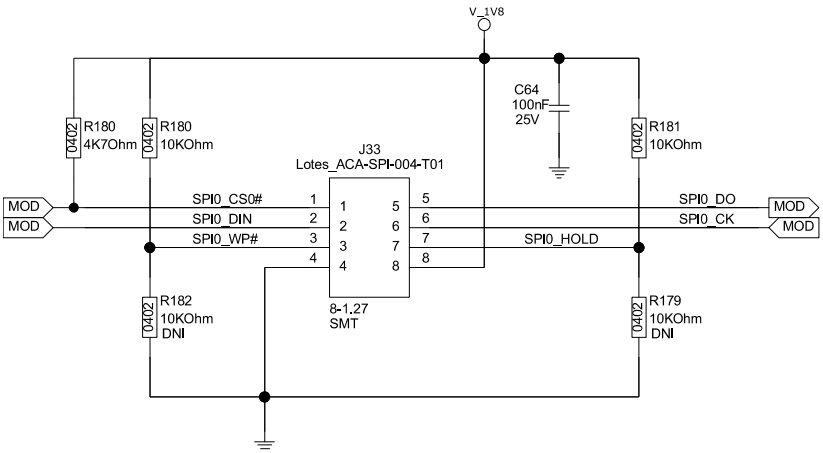
The SMARC Module will always be the SPI master. SMARC Modules may support a Carrier SPI Boot option.

4.5.1 SMARC Implementation

Each SPI device requires a chip select, a clock, a data in line and a data out line. The device I/O level must of course be compatible with the SMARC Module I/O level of 1.8V.

The Winbond W25Q64FW is an example of a 1.8V I/O compatible SPI Flash device. The Figure 40 SPI Flash Socket below illustrates a socket implementation for a SPI Flash memory.

Figure 40 SPI Flash Socket



4.5.2 SPI Device Examples – 1.8V I/O

The Table 6 SPI Device Examples - 1.8V I/O below shows a small sample of the devices available on the market with a 1.8V SPI interface. It is only a sample and is meant to give an idea of the type of devices available. Remember to check the software driver situation before settling on a particular device.

Table 6 SPI Device Examples - 1.8V I/O

Function	Device Description	Vendor	Vendor P/N
ADC	8-channel, 12-bit SAR ADC with temperature sensor	Analog Devices	AD7298
DAC	Quad, 16-bit nano DAC	Analog Devices	AD5686R
Flash Memory	64 Mbit SPI Flash memory	Winbond	W25Q64FW
IO Expander	8-bit GPIO expander with integrated level shifters	MaxLinear (formerly Exar)	XRA1404
Temperature Sensor	Digital thermometer ±2 °C resolution Range - 55°C to +120 °C	Maxim Integrated	DS1722
Touch Screen Controller	4 wire resistive touch screen controller	Texas Instruments	TSC2008-Q1
UART bridge	UART with 128 Word FIFOs and support for 9-bit multi-drop mode data filtering	Maxim Integrated	MAX3108

4.6 CAN Bus

The CAN (“Controller Area Network”) bus is a differential half duplex data bus used in automotive and industrial settings. A CAN bus uses shielded or unshielded twisted differential pair wiring, terminated in the pair differential impedance of 120 ohms at the endpoints of the bus. Nodes on the bus are arranged in daisy-chain fashion, although stubs of up to 0.3 meters are allowed at each node. The standard allows data rates of up to 1 Mbps, with a maximum bus length of 40 meters at that rate. Various slower rates are defined, along with longer and longer bus lengths allowed as the data rates go down. A bus rate of 250 kbps is in common use in automotive situations. With CAN FD also faster baud rates are possible.

The two lines in a CAN twisted pair are referred to as CAN_H and CAN_L (for CAN High and CAN Low). There are two bus states on the CAN physical layer: the Dominant state and the Recessive state. In the Dominant state, CAN_L is pulled to GND through an open drain driver and CAN_H is pulled to the CAN Vcc through an open drain driver. In the Recessive state, CAN_L and CAN_H are not actively driven and they are pulled to a voltage of (Vcc / 2) by passive components. Hence the CAN bus is essentially a differential open-drain bus. On the system logic side of a CAN transceiver, the CAN Dominant state is a logic low and the Recessive state a logic high.

The CAN protocol has features important to a real time environment:

- Nodes are prioritized: CAN nodes are assigned an 11 bit identifier
    - The lower the ID number, the higher priority
- Latency time is guaranteed
- Data packets are limited to 8 bytes maximum
    - Higher level protocols take care of handling large data sets
- The bus has Multi-master capability
- There are error detection and signaling features

The CAN bus base standard is defined by ISO 11898-1:2003, available for a fee from the ISO (**www.iso.org**). There are some very helpful CAN application notes from Texas Instruments (a vendor of CAN MAC and transceiver devices) available for free. These include “***Introduction to the Controller Area Network (CAN)***”, TI document number SLOA101A, and “***Controller Area Network Physical Layer Requirements***”, document number SLLA270. The original CAN bus protocol definition by Bosch is also freely available on the web (***CAN Specification***, Version 2.0 © 1991 Robert Bosch GmbH).

Various connectors are used in CAN bus implementations. The use of DB-9 connectors is fairly common. The TI application note (SLLA270) referenced above has pin-out information for a couple of common CAN connector implementations.

4.6.1 SMARC Implementation

The SMARC specification allows for up to two logic level CAN ports. The ports run at the Module I/O voltage (typically 1.8V) and consist of an asynchronous CAN TX line and an RX line from and to the SMARC Module CAN protocol controller.

A Carrier based CAN transceiver is required to create a SMARC system CAN implementation. CAN PHYs are available from Texas Instruments, On Semiconductor, NXP, Microchip and numerous other vendors. The logic interface for CAN PHYs is typically suited for 3.3V logic I/O, so level translation is required if the SMARC Module is running 1.8V I/O.

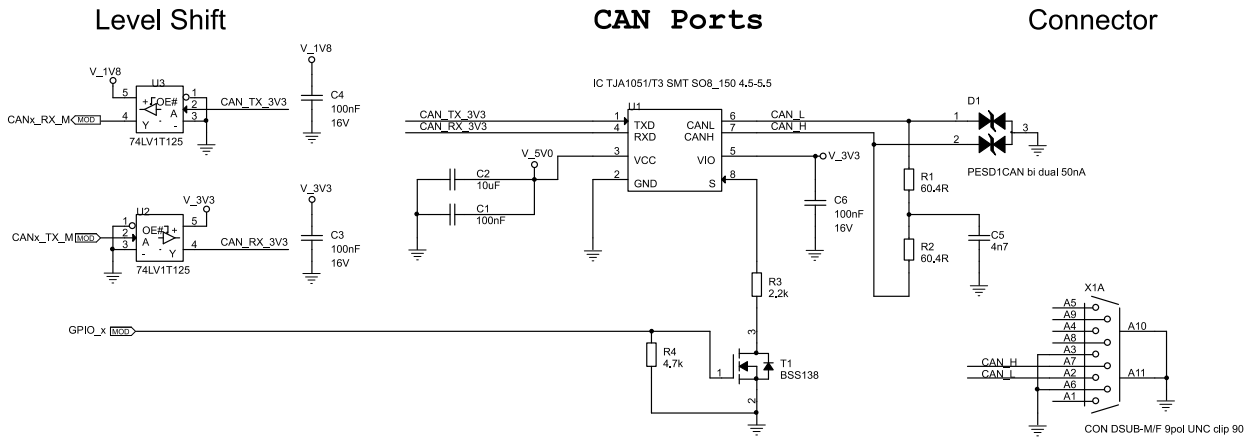
Precautions must be taken to prevent a CAN system from sending out frames or blocking a CAN-Bus unintentionally, for example during reset and power down. During power down, CAN Transceivers are designed to be HIGH-Z. During power up or reset, they must be put into a “listen only mode”. It is the responsibility of the application software to activate the CAN-transceiver after all initialization is done. If no GPIO connection is possible or wanted this signal also could be connected to the RESET_OUT# signal from the SMARC Module. Please check your design carefully if this ensures that no unwanted frames are send in your design.

A SMARC Carrier board CAN transceiver implementation is shown below. This example shows two 60 ohm terminations (or 120 ohms across the CAN pair). This is appropriate only if the node is an end-point, and intermediate nodes should not be terminated.

The example transceiver TJA1051 has a “silent input pin”. If left open, the transceiver enters “listen only mode”. Using a GPIO allows the application software to set the can transceiver into “normal mode = able to send” by pulling “silent” low. A pull down resistor on the gate of T1 is necessary to disable the transceiver in case of a CPU reset or power fail.

It is recommended to use GPIO8 as CAN0_EN and GPIO9 as CAN1_EN.

Figure 41 CAN Bus Implementation



4.6.2 Isolation

Some CAN transceiver application notes show optical isolation between the CAN protocol controller and the CAN transceiver. See, for example, NXP (Philips) application note AN96116 for the PCA82C250 CAN transceiver. They suggest using the 6N137 optical transceivers. Be careful to take into account the I/O levels and current sink / source requirements of the various devices in the chain.

5 HIGH SPEED SERIAL I/O INTERFACES

5.1 USB

The USB (Universal Serial Bus) is a hot-pluggable general purpose high speed I/O standard for computer peripherals. The standard defines connector types, cabling, and communication protocols for interconnecting a wide variety of electronic devices. The USB 2.0 Specification defines data transfer rates as high as 480 Mbps (also known as High Speed USB). A USB host bus connector uses four pins: a power supply pin (5V), a differential pair (D+ and D- pins) and a ground pin. Additionally a fifth pin, USB ID (mostly used in devices supporting USB-OTG), may also be used which indicates whether the device operates in Host mode or a Client/Device mode.

SMARC Modules support up to six independent USB 2.0 busses, designated USB0 to USB5. Of these, SMARC USB0 and USB3 can be configured as a host, client or OTG port. OTG and client operation are optional. SMARC USB1, USB2, USB4 and USB5 are defined as always hosts. A USB host is usually the smarter device – a host computer for example. A USB client is usually a peripheral device, such as a camera, printer or mass storage device. USB clients are often based on microcontrollers that include USB client interface hardware.

USB3.0 Super Speed is supported on USB2 and USB3 and defines data rates up to 5 Gbps (also referred to as USB 3.2 gen1). Therefore these ports have two additional differential signal pairs SSRX and SSTX.

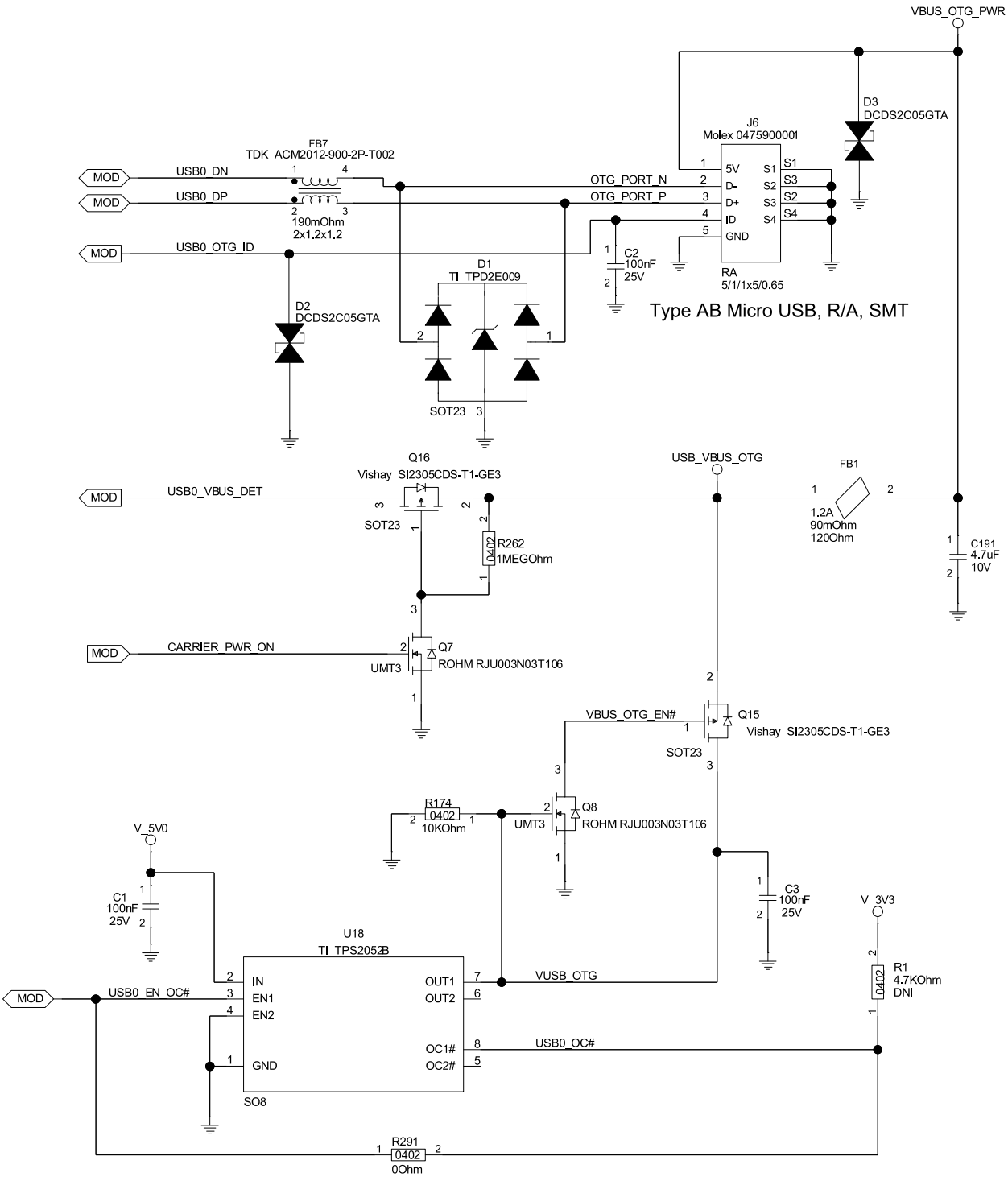
USB3 may also support a USB3.0 OTG port.

5.1.1 USB0 Client / Host Direct From Module

The **Figure 42 USB0 Client / Host Direct From Module** shows a USB-OTG implementation on the USB0 port terminated on a micro USB Type A/B connector

The ESD diodes should be placed close to the connector, and the USB traces routed as differential pairs in “no stub” fashion – the traces should go through the pads of the ESD protection devices, without introducing a stub. If the client device is bus powered, the Carrier can supply 5V, 500mA power to the client device. The Module USB0_EN_OC# signal controls the power switch and current limiter, the Texas Instruments TPS2052, which in turn supplies power to a bus-powered client device. Per the USB specification, bus powered USB 2.0 devices are limited to a maximum of 500 mA. The TPS2052 limits the current and can stand an indefinite short circuit to GND. The current limiting is somewhat imprecise, and kicks in between 500 mA and 1A.

Figure 42 USB0 Client / Host Direct From Module

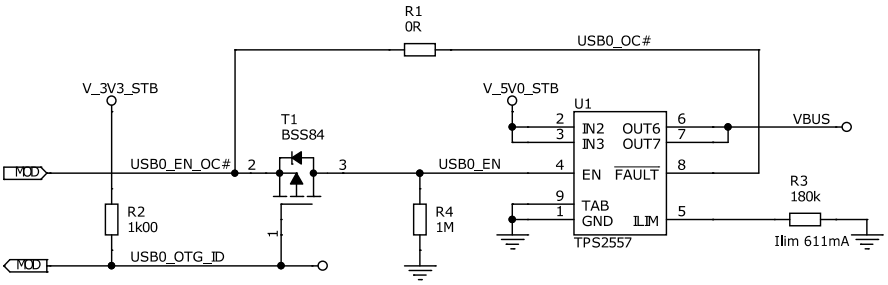


Note: The combined enable and over current signal can result to toggling USB supply voltage. If the Module cannot react fast enough to the over current feedback from the current limiting power switch to inactivate the USB power enable signal the feedback can be disconnected by removing R291. Please be aware that this way the over current situation cannot be detected from the Module any longer.

Note: If the Module doesn´t support USB ID Pin for OTG / Host-Client function the USB VBUS supply control can be manipulated directly (please refer to **Figure 43 USB OTG - Discrete VBus Enable**). A Micro USB type A plug at the Carrier receptacle pulls the ID pin signal to ground so that the Module acts as a Host. With ID signal low the Carrier may drive USB VBUS.

If in doubt, ask your Module vendor for details of OTG and bus power control support.

Figure 43 USB OTG - Discrete VBus Enable Handling



USB0_OTG_ID is pulled low (< 10R to GND) for Host mode within the USB cable if a Micro USB type A plug is used. In case of Device mode is required a USB cable with a Micro USB type B plug is needed. In that case the USB0_OTG_ID signal is floating (> 100k to GND). This results in a “high” signal for the ID pin.

Note: The USB0_EN_OC# pin has a PU resistor (10k to +3.3V) at the Module.

5.1.2 USB1 And USB4 Host Ports Direct From Module

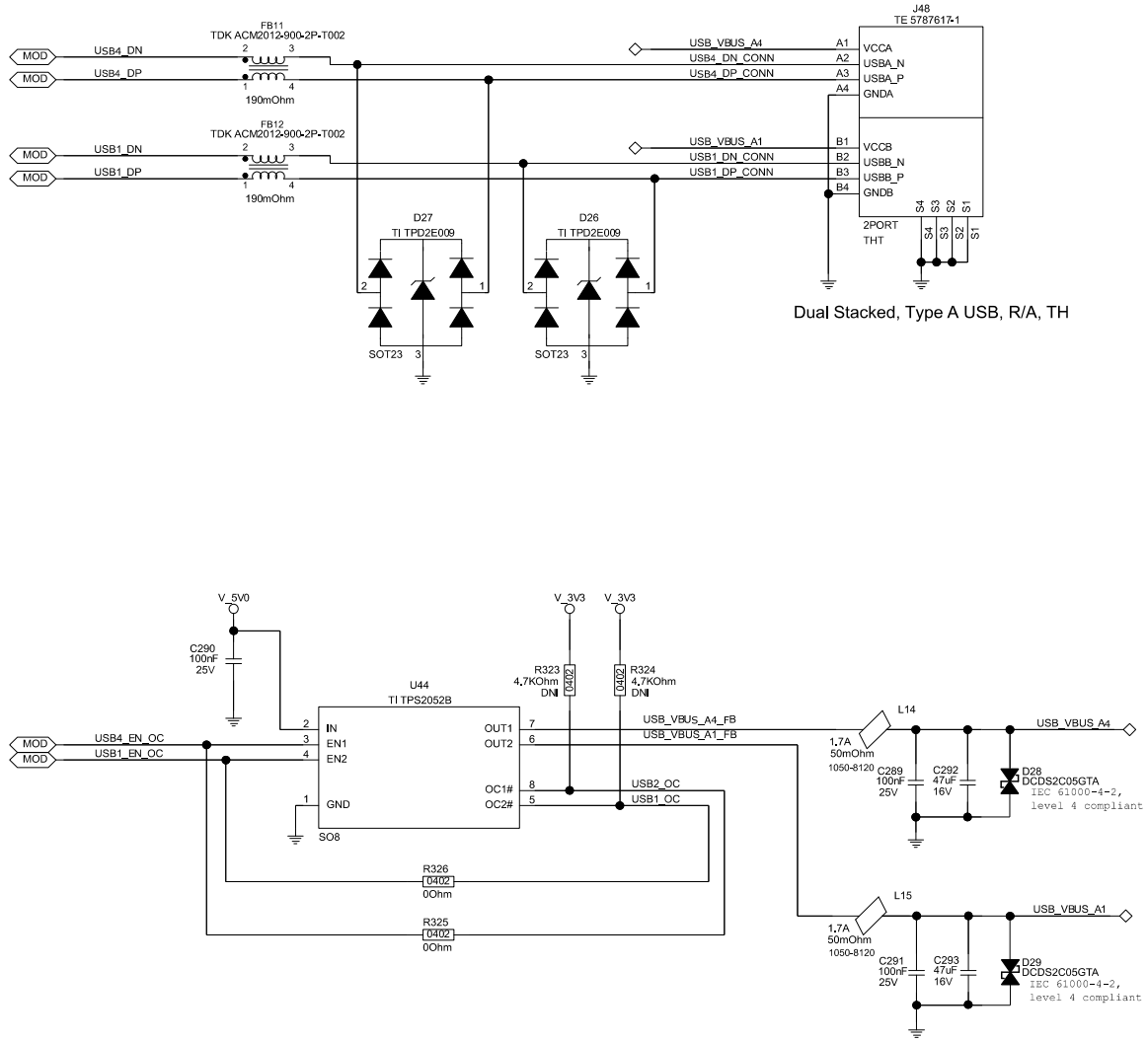
Carrier board implementation of USB host ports from SMARC USB1 and USB4 is straightforward. An implementation of a dual USB Type A host port header is shown in the figure below.

The ESD diodes should be placed close to the connector, and the USB traces routed as differential pairs in “no stub” fashion – the traces should go through the pads of the ESD protection devices, without introducing a stub.

If the target USB devices are “down” on the Carrier, then much or all of this circuit may be omitted. The SMARC USB pairs are routed directly to the target device. The ferrite choke in the USB lines, the ESD diodes, and the TPS2052 power switch and associated passives may be eliminated. However, in some cases, it is desirable to have the capability to “power cycle” a USB peripheral under software control. If this is the case, it might be desirable to retain the TPS2052 power switch, or a similar device for 3.3V power switching, with the power control function performed by the USB1_EN_OC or USB4_EN_OC, as appropriate.

Also the USB5 port can be used in this way.

Figure 44 USB1 And USB4 Host Ports Direct From Module



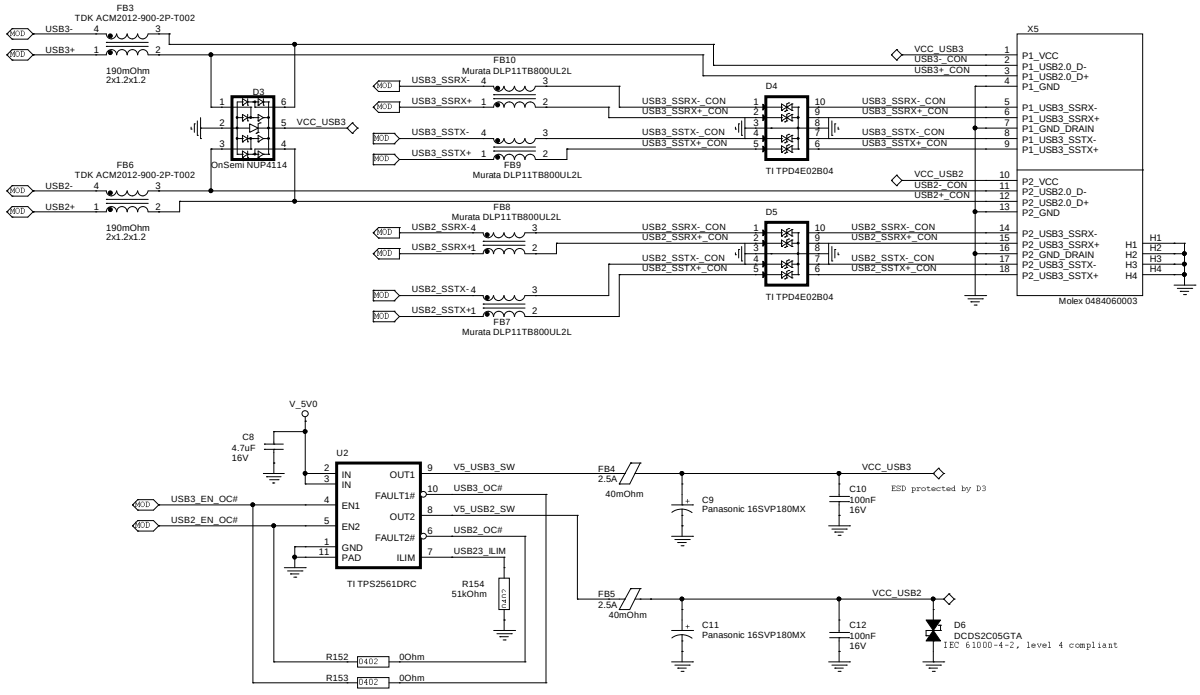
5.1.3 USB2 And USB3 Host Ports Direct From Module

The USB2 and USB3 ports can be USB 3.0 ports and each consists of a USB 2.0 port and a set of unidirectional SuperSpeed differential pair signals. The following example shows an implementation of a stacked dual USB 3.0 connector that is utilizing USB2 and USB3 without using the optional OTG capabilities of USB3.

Place the ESD diodes as close as possible to the connector. For SuperSpeed Signals, ESD diodes with optimized package and low I/O capacitance should be used to create only minimal impact on signal integrity. Also the common mode chokes should be selected carefully. Ensure that their differential mode cutoff frequency is well above the maximum frequency of 2.5 GHz of a USB3.0 signal.

Each USB 3.0 port should be able to supply up to 900mA and should be decoupled with at least 120µF of low ESR capacitance. Not including any USB PD capabilities.

Figure 45 USB2 And USB3 As USB 3.0 Host Dual Port



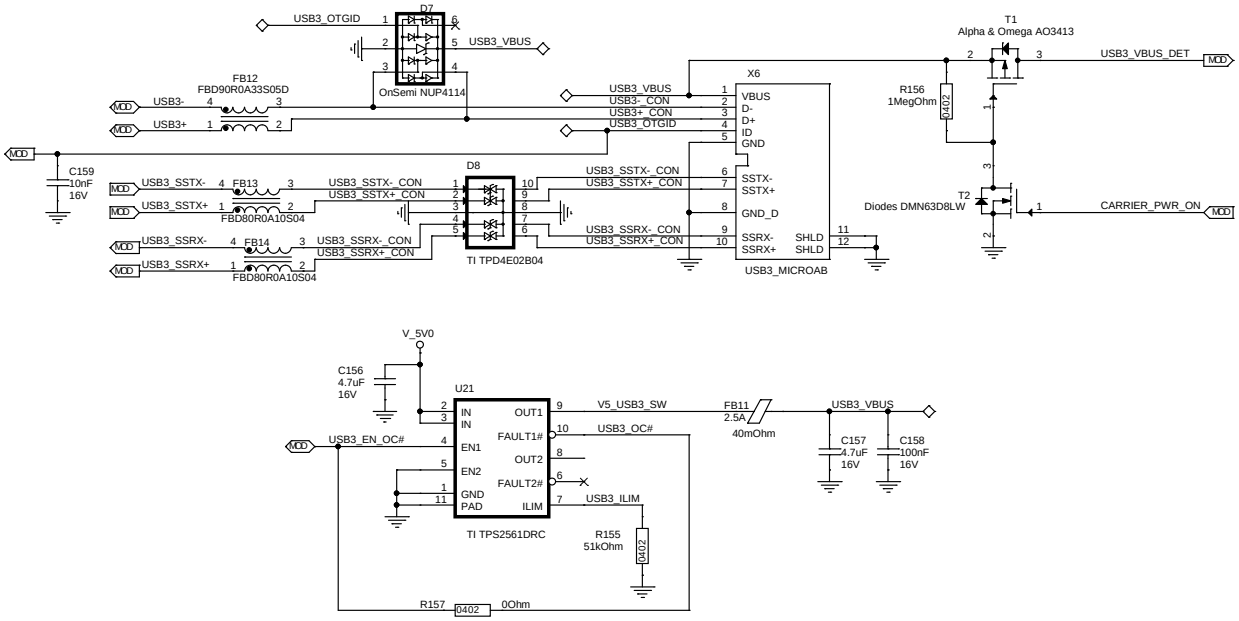
5.1.4 USB3 Client / Host Direct From Module

USB3 may support OTG functionality, depending on Module's capabilities. Check with your Module's vendor manual whether USB3 supports OTG.

Please note that dual role devices should have a VBUS capacitance that is in a range of 1.0µF to 6.5µF.

The ESD diodes should be placed as close as possible to the connector. Take care that VBUS and ID pins are also protected against ESD events as they are directly connected to the SMARC 2.1.1 Module. The Module will control the power switch by driving USB3_EN_OC#. It will be driven low in order to cut-off power to VBUS as it is required for client mode.

Figure 46 USB 3.0 OTG



5.1.5 USB Hub On Carrier

Additional USB ports may be implemented on a SMARC Carrier board using a USB hub to interface with one of the SMARC USB ports (usually USB1 or USB2, saving the SMARC USB0 for possible client or OTG use). The USB 2.0 compliant (and 480 Mbps capable) family of hubs from Microchip (**www.microchip.com**) is recommended. Parts with two, three, four or seven downstream ports are available.

A Carrier hub implementation example using the seven port Microchip USB2517i is shown in the two figures below. There are three configuration straps on this particular hub, designated CFG_SEL[2] through CFG_SEL[0]. The options need to be considered carefully. The example schematic has the 2:0 configuration straps set to binary 110, which, per the Microchip datasheet, sets the hub to the following:

- Microchip hub defaults in effect
- Other strap options disabled
- Hub LED pins configured to indicate USB speed
- Individual port power switching
- Individual port over-current sensing
- External EEPROM not used
- External I2C interface not used

Although the sample schematic shows the external EEPROM and I2C interfaces, they are not used. Note that the “DNI” designation on the schematic stands for “Do Not Install” – i.e. the part is not loaded, in this example.

If implementing such a hub (or any piece of configurable silicon), it is wise to keep your options open and have all strap options accessible for re-configuration by option resistors or other means. It may keep you out of trouble and save an additional board spin.

Since the hub operates at 3.3V, the signals from the SMARC Modules that are at 1.8V (RESET_OUT# and the I2C_GP_ signals, if used) levels need to be level shifted to 3.3V to interface to the hub.

In this example, there are 7 down-stream ports. Two of them are used for Off-Carrier cabled connections. These nets are designated with USB_HUB2_ and USB_HUB3_ prefixes. Since they are used for cabled connections, these are protected by a USB power switch (U19, in the second figure below). Four of the other hub ports are assumed to go to On-Carrier destinations (such as mini-PCIe cards, or a touch controller, or other On-Carrier USB peripheral). One of the 7 down-stream ports is not used.

The behavior of a USB port, at least initially, may differ slightly depending on whether that port is direct from the SMARC Module or whether the port is through a hub. With software adjustments, or “tweaking”, the direct and through – the –hub ports may appear virtually identical to a client device.

Figure 47 USB 2.0 Hub (1 of 2)

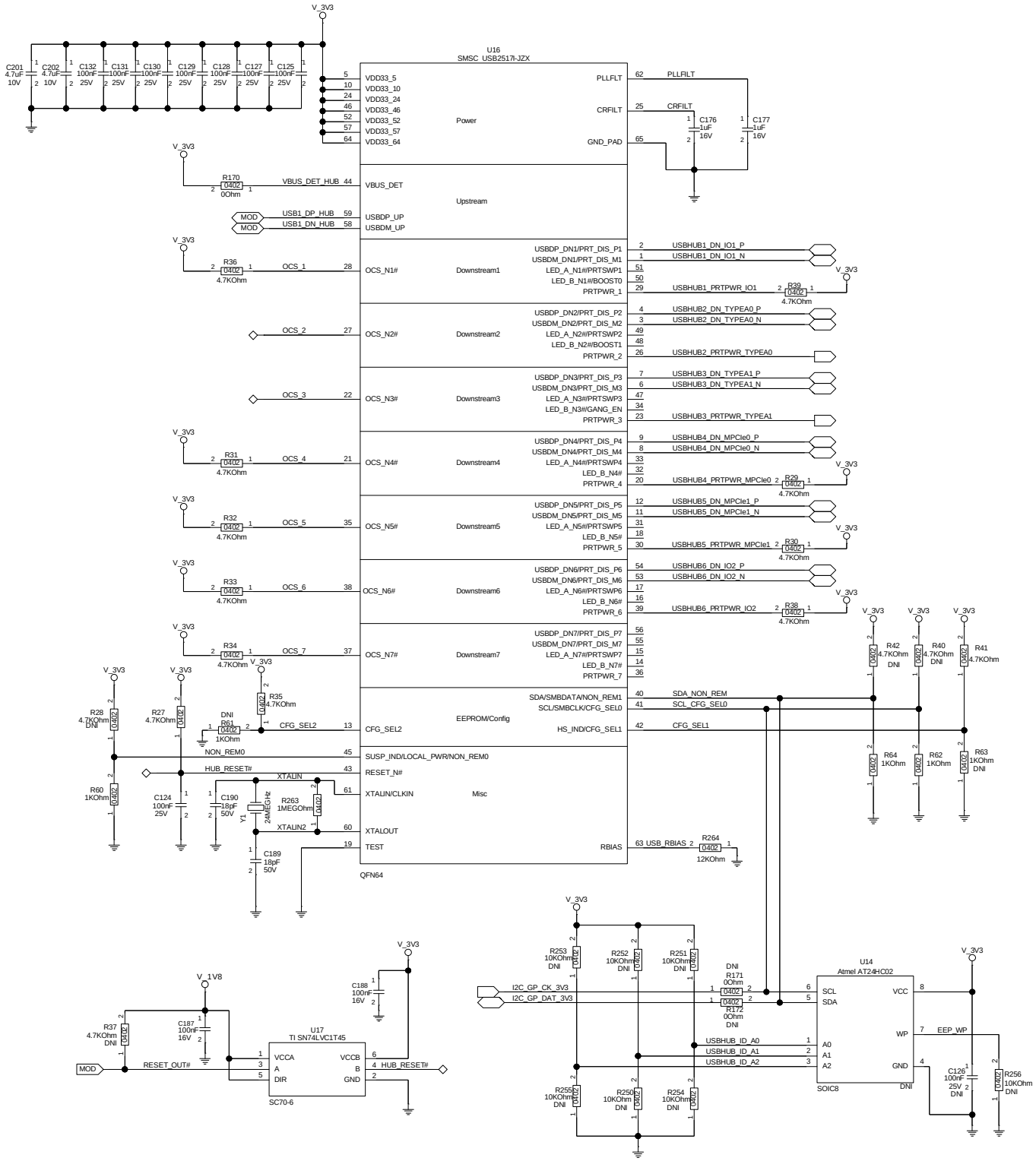
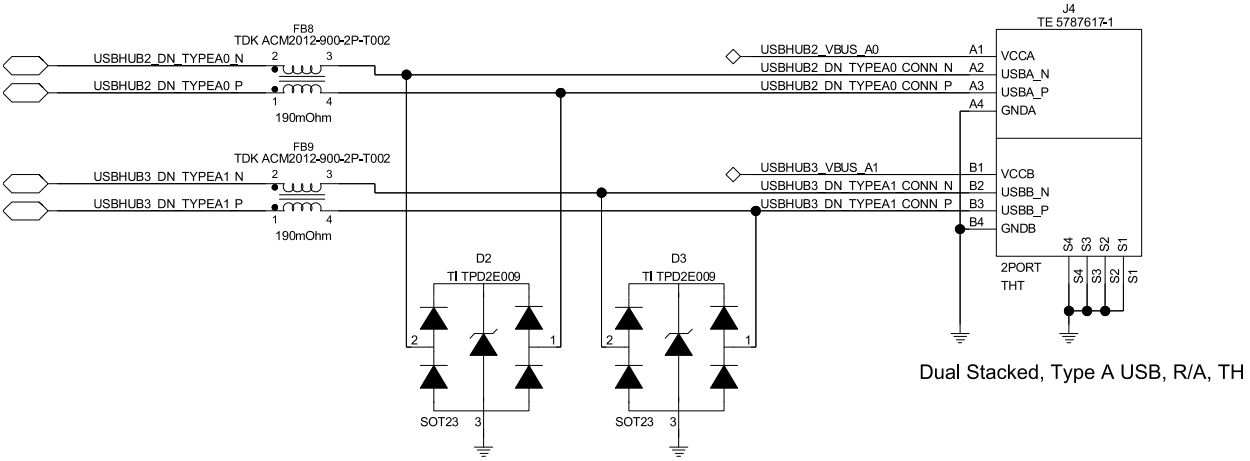
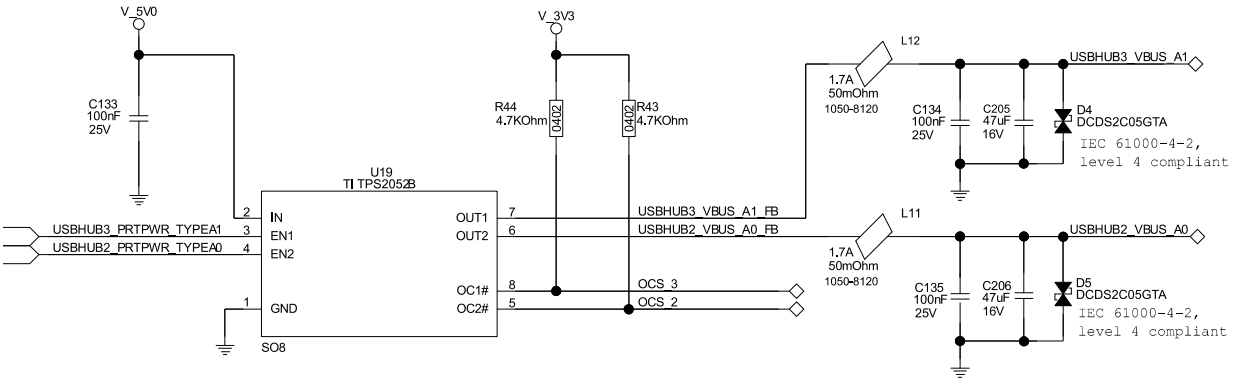


Figure 48 USB 2.0 Hub (2 of 2)





5.1.6 USB type C – Parade PS8750B

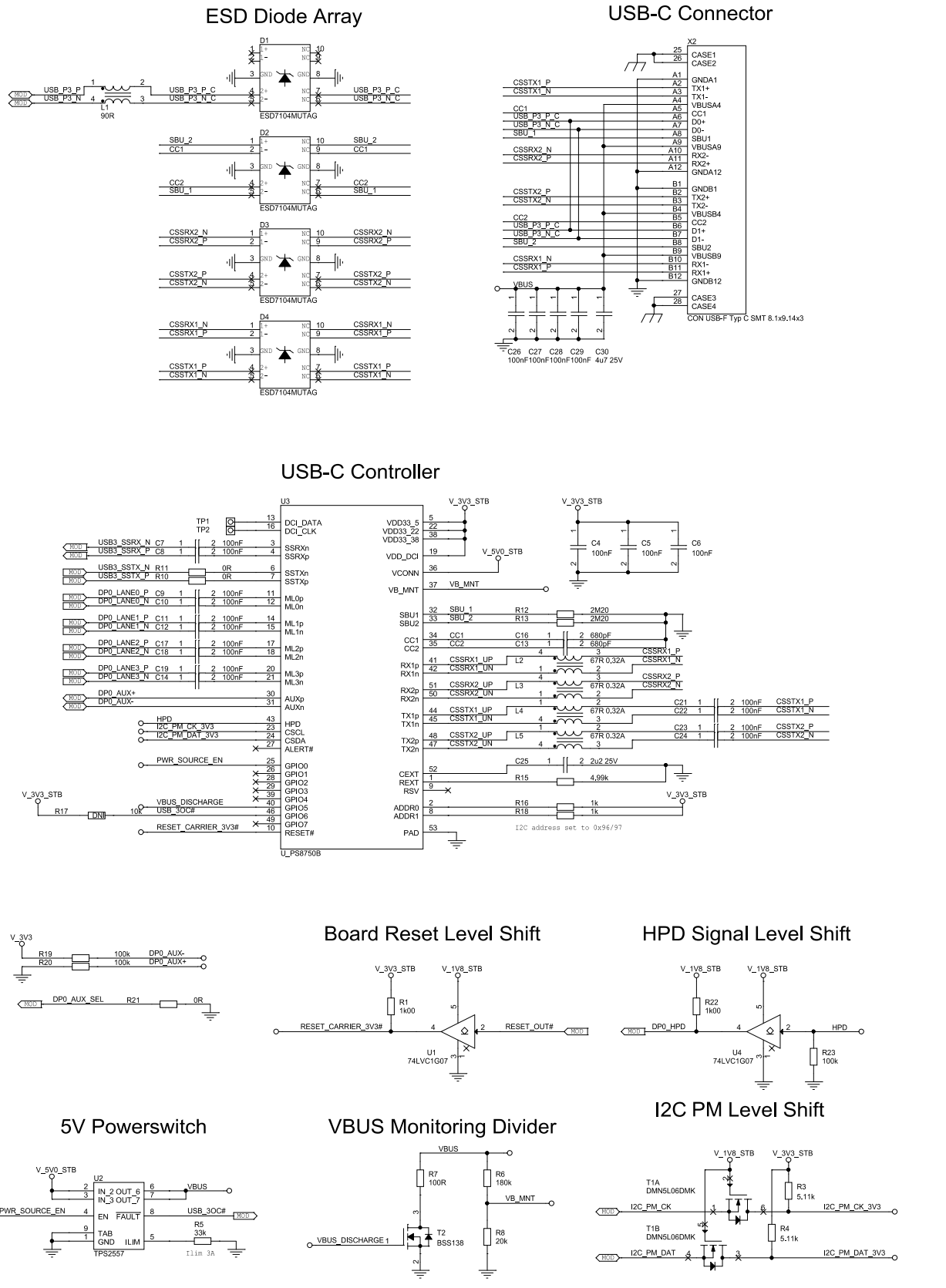
USB type C together with USB PD is a great achievement from the USB consortium to simplify the interfacing between devices and the usage of technology for users. The more complex it is for possible implementations.

To demonstrate that all these features are also available by designing Carriers with SMARC modules a type C connector implementation with USB 3.0 (or 3.2 gen1) with DP alternate function is shown in **Figure 49 USB type C – Parade PS8750B**. It doesn´t include a specific power controller to support enhanced PD functionality but can support up to 3A at 5V to the connector.

Level shifters are implemented to interface the 3.3V signals from the PS8750 to the SMARC required 1.8V signals.

The PS8750 is connected to Stand-By voltages so that Wake-On-USB applications are possible.

Figure 49 USB type C – Parade PS8750B

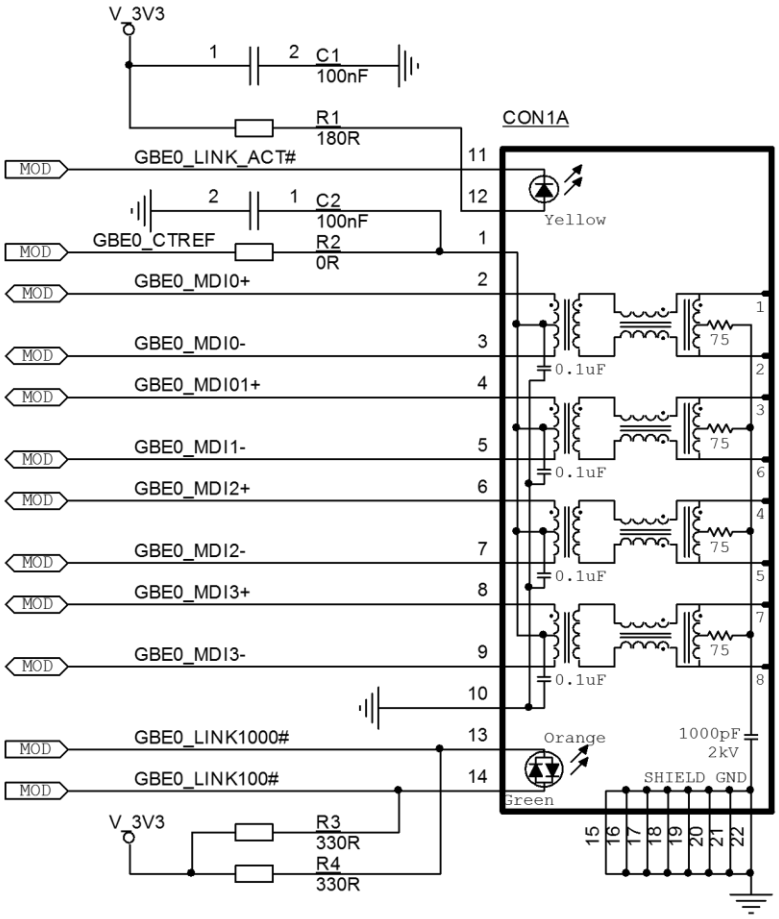


5.2 GBE

5.2.1 GBE Carrier Connector Implementation Example

SMARC Modules include GBE MAC / PHYs but do not include the isolation magnetics. If the SMARC GBE is used, then the Carrier must include GBE compatible magnetics with 1:1 turn ratios. Usually RJ45 jacks with integrated magnetics are used. An example is given in the following figure.

Figure 50 GBE without POE



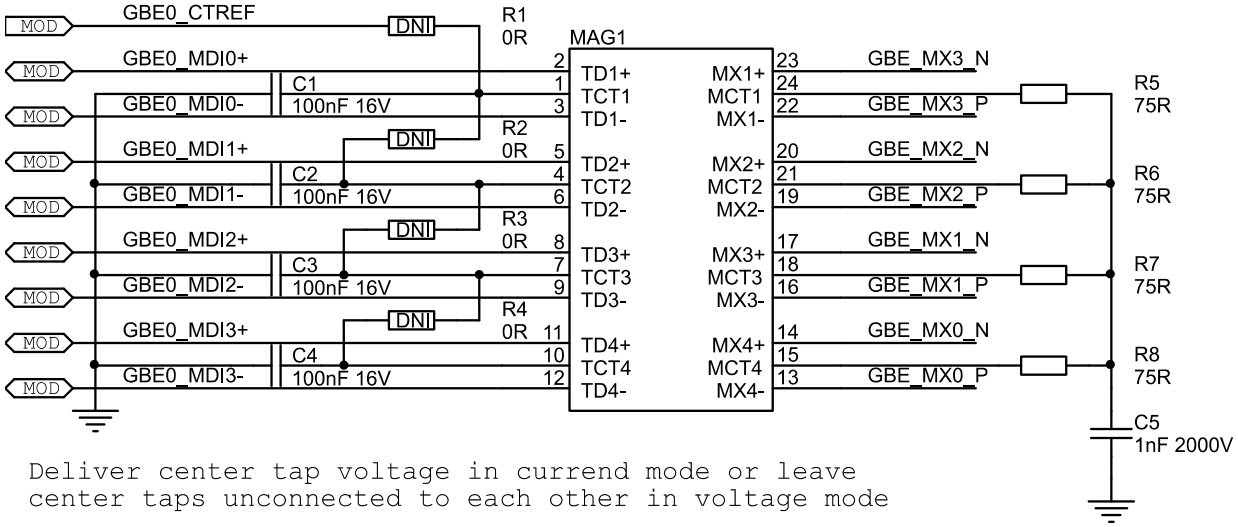
There are two kinds of 1000Base-T Line Driver implementations. The current mode line drivers pull current from one side of the magnetic. To generate the IEEE-specified five level pulse amplitude modulated (PAM) signals two 50 Ohm termination resistors to center tap voltage are required. They are placed in parallel to the output impedance at line driver side. The magnetic center taps are connected to each other and to the center tap reference voltage. This voltage can be provided by the GBE PHY to the magnetic with the GBE_CTREF pins at the SMARC Module.

Voltage mode line driver use series resistors to generate the PAM signal at the magnetic. They are more power efficient, but even more complex. The line driver enables the internal series resistors at the transmit signal pairs.

For most voltage mode PHYs the center taps at the magnetic can be connected to each other and clamped by separate or combined capacitors. They are not connected to any center tap voltage provided by the PHY. There are some voltage mode PHYs available, that do not allow to combine the center taps, due to different voltage levels at RX and TX pairs. These PHYs do not support the usage of RJ45 connectors with integrated magnetics.

See SMARC Module documentation for selected GBE PHY and line driver version.

Figure 51 GBE separate magnetic for current and voltage mode line driver



5.2.2 GBE Mag-Jack Connector Recommendations

SMARC GBE Mag-Jack (magnetics integrated into an RJ45 jack housing) should meet the following general characteristics:

- The turn ratios should be 1:1
- An integrated common mode choke should be included
- Termination resistors on the primary side (i.e. the Ethernet cable side) should be included
- The secondary side transformer center-taps may be tied together or may be brought out separately. If they are brought out separately, they are tied together on the Carrier PCB.
- The secondary side center-taps need to be tied to the SMARC GBE_CTREF voltage, with bypass capacitors connected to GND.

Mag-Jacks (and RJ45 jacks in general) are available in ***tab-up*** and ***tab-down*** configurations. The pin order on the Mag-Jack reverses between the tab-up and tab-down configurations. One of them may work better for your layout than the other (although since only four pairs are involved, this may not be a major concern). Tab-up is generally more common; tab-down parts do exist; most tab-down parts target low-profile needs in which part of the Mag-Jack connector height is hidden by a Carrier PCB cutout.

Table 7 Recommended Gigabit Ethernet Connectors with Magnetics

Manufacturer	Manufacturer P/N	Description
Bel Fuse	L829-1J1T-43	Tab Up, 1:1 turns ratio, 3 LEDs, 0.950” depth
Pulse	JK0-0136NL	Tab Up, 1:1 turns ratio, 3 LEDs, 1.30” depth
Tyco	1840437-1	Tab Down, 1:1 turns ratio, 3 LEDs, special low profile feature
Wurth	7499111447	Tab Up, 1:1 turns ratio, 4 LED

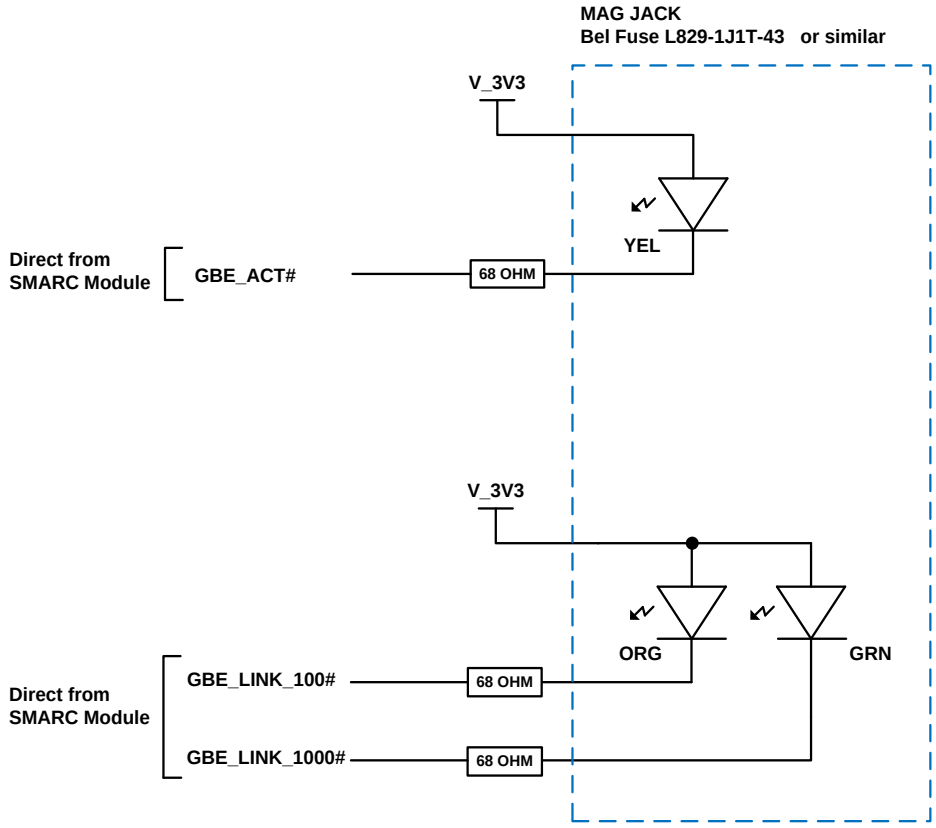
Note that POE (Power Over Ethernet) capable jacks are slightly different – they have extra pins to bring the POE power into the system. A GBE POE jack may be used in a non-POE system, but not the other way around. A GBE POE example is given in chapter **9.11 Power Over Ethernet** later in this Design Guide.

5.2.3 GBE LEDs

Mag-Jack LED implementations vary widely. There does not seem to be any common standard, so be aware.

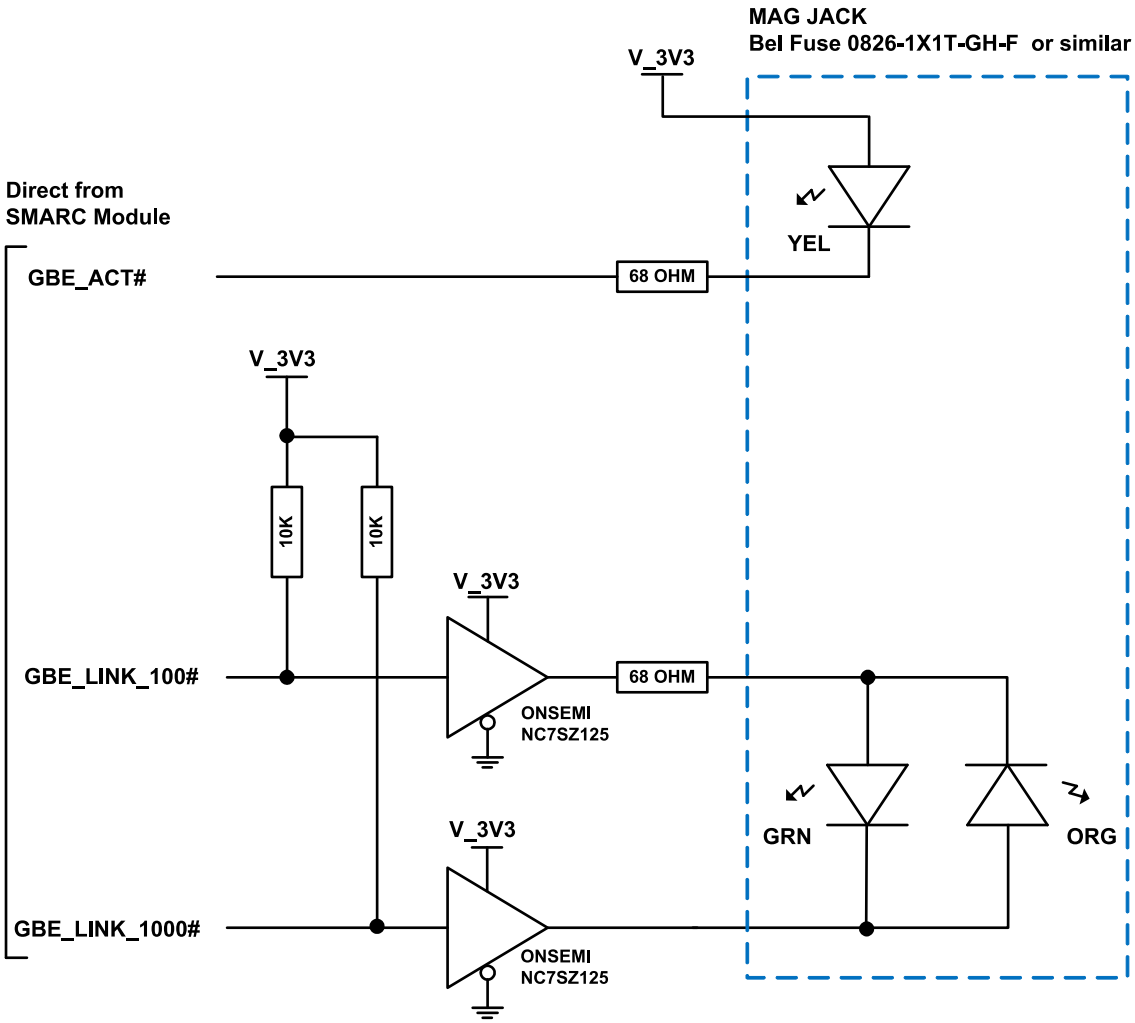
The SMARC GBE status LED outputs are open drain outputs that are capable of sinking up to 24 mA. They may be connected directly to the cathode of GBE status LEDs as shown in the following figure. Make sure the resistors can handle the expected power dissipation.

Figure 52 GBE LED Current Sink



Some integrated GBE Mag Jacks have a pair of opposing (cathode to anode) diodes, as shown in the **Figure 53 GBE LED Current Sink / Source**. In this case, Carrier board buffers are recommended, as the SMARC Module status LED lines can sink current but cannot source it.

Figure 53 GBE LED Current Sink / Source



5.2.4 GBE software-defined Pins

The Precision Time Protocol (PTP) (according to IEEE 1588) is used to synchronize clocks throughout a computer network. If it is implemented in the hardware of the Ethernet controller clock accuracy in the sub-microsecond range can be achieved.

The Ethernet controller usually has several GPIO pins whereof one can be connected to the GBE_SDP pin. This pin can be used as output and distribute synchronized clocks or trigger impulses. When used as input it can synchronize the internal clock of the controller to external clocks for example from GPS receivers. Such a system could serve as a master clock.

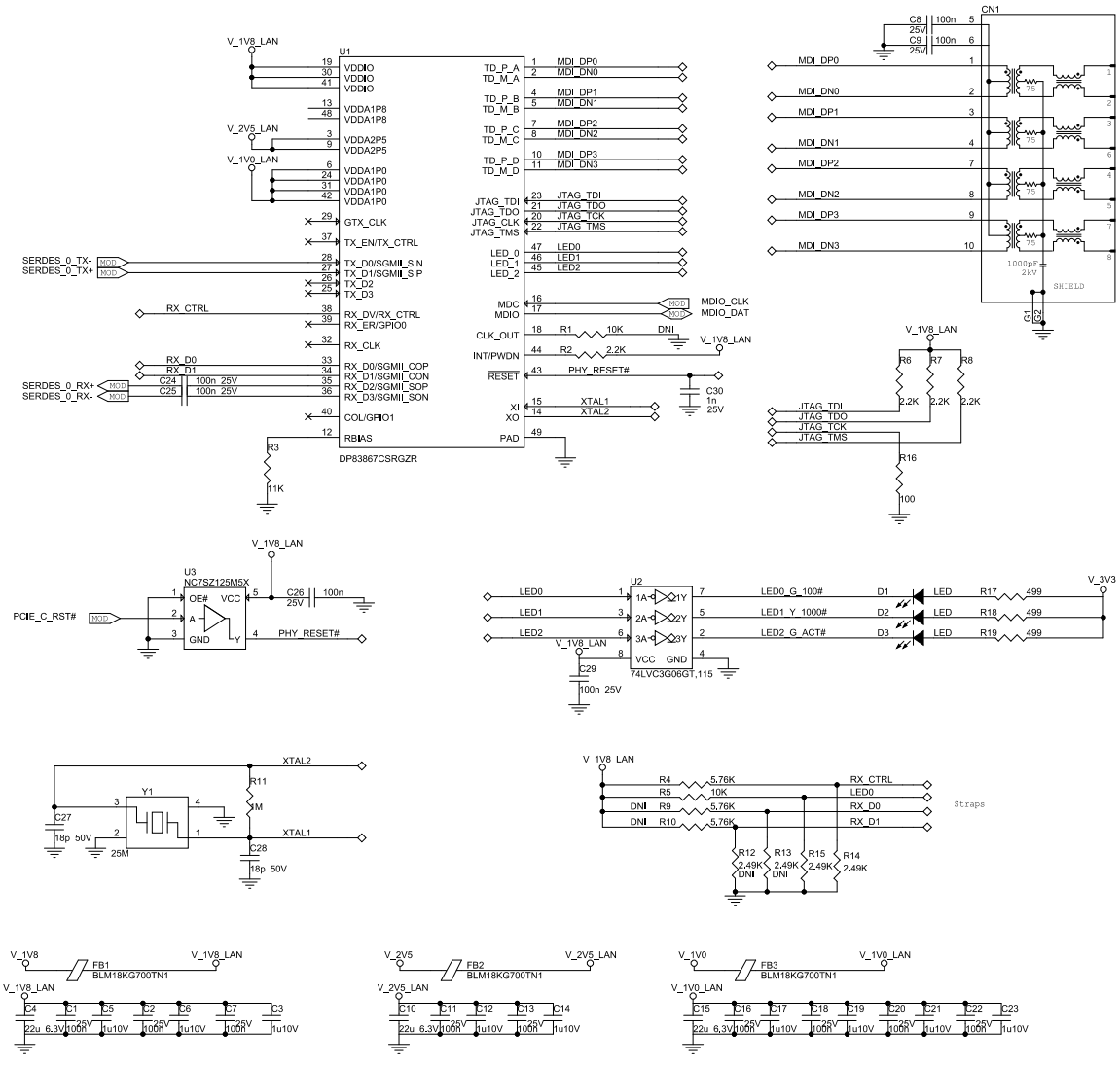
These functions depend highly on the used Ethernet controller and wiring – check with your Module vendor.

5.3 SERDES

The SERDES0 and SERDES1 interfaces can be utilized to connect an SGMII PHY to the interface. In this example a single GBE interface is created on the Carrier connected to the SERDES0 interface. There are also quad PHYs available in the market to allow enhanced functionality. For easier understanding a single PHY was selected for the Design Guide.

Figure 54 GBE implementation using SERDES0 interface

SERDES0 INTERFACE
DP83867: gigabit Ethernet PHY transceiver with SGMII



DESIGN NOTES

RUNTIME POWER DOMAIN AS 2.1.1 SMARC SPEC
PHY RESET CONNECTED TO PCIE_C_RST# (3.3V O CMOS)

Within this example VDDIO of U1 has been set to 1.8V. This way, the MDIO signals can be directly connected to the SMARC module without the need of additional level shifters. In case level shifters are needed please refer to chapter **4.2.1 I2C Level Translation, Isolation and Buffering**.

PHY_RESET# has been translated from 3.3V to 1.8V by using the PCIE_C_RST# signal from the SMARC module. The chosen buffer NC7SZ125 is already in use within the DG. It can work with a signal voltage of up to 6V regardless of VCC.

U2 power supply is set to 1.8V to be compliant with the LED0...LED2 input signals. As output, it is 5V tolerant, so it can directly drive LEDs powered at 3.3V.

Note: This example is utilizing the SERDES0 interface. In order to use it for the SERDES1 interface please change the RX_D straps and SERDES_TX+/- / SERDES_RX+/- signals accordingly. The PHY RESET signal will stay the same of the SERDES0 implementation.

5.4 PCIe

PCI Express (or PCIe) is a scalable, point-to-point serial bus interface commonly used for high speed data exchange between a PCIe host, or root, and a target device. It is scalable in the sense that there may be link widths, per the PCIe specification, that are x1, x2, x4, x8, x16 or x32. SMARC currently calls out x1, x2 and x4 operation. Up to four PCIe x1 links may be implemented on a SMARC Module. There are four generations of PCIe defined, with each successive generation offering a speed increase, per the table below. The PCIe generation that may be supported on a particular SMARC Module is design and SOC dependent.

Table 8 PCIe Data Transfer Rates

PCIe Generation	Link Speed (x1 link)	Encoding / Overhead	Net Data Transfer Rate (per lane)
1	2.5 GT/s	8b/10b 20%	250 MB/s
2	5.0 GT/s	8b/10b 20%	500 MB/s
3	8.0 GT/s	128b / 130b 1.54%	985 MB/s
4	16.0 GT/s	128b / 130b 1.54%	1,969 MB/s

PCI Express is defined in a series of documents maintained by the PCI Special Interest Group (**www.pci-sig.org**). The three most important documents to obtain are the Base Specification, the Card Electromechanical (CEM) Specification (which describes slot cards) and the Mini Card Electromechanical Specification (which describes the small format cards commonly referred to as Mini-PCIe cards).

The four possible PCIe links on a SMARC Module are designated with net name prefixes PCIE_A_, PCIE_B_, PCIE_C_ and PCIE_D_. Each of the four has the following signal set (x in the **Table 9 SMARC PCIe A, B, C Signal Summary** below designates A, B or C) with the exception of PCIE_D which is visible in **Table 10 SMARC PCIe D Signal Summary** that doesn´t carry an own REFCLK.

Table 9 SMARC PCIe A, B, C Signal Summary

Signal	Description	Signal Type	Notes
PCIE_x_TX+ PCIE_x_TX-	Data out of Module	Differential pair	Capacitive coupled – on Module
PCIE_x_RX+ PCIE_x_RX-	Data into Module	Differential pair	Capacitive coupled – on Carrier
PCIE_x_REFCK+ PCIE_x_REFCK-	Reference clock out of Module	Differential pair	No caps needed
PCIE_x_RST#	Active low output to reset the PCIE_x device	Single ended	

Table 10 SMARC PCIe D Signal Summary

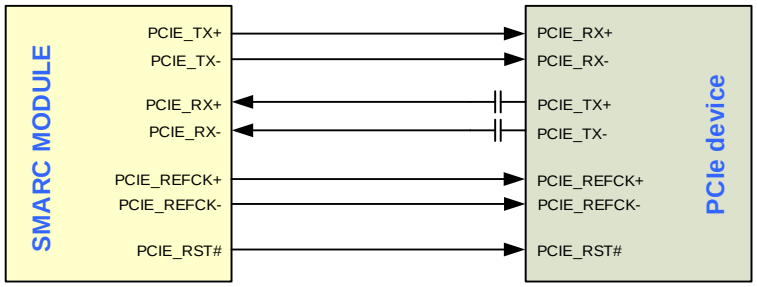
Signal	Description	Signal Type	Notes
PCIE_D_TX+ PCIE_D_TX-	Data out of Module	Differential pair	Capacitive coupled – on Module
PCIE_D_RX+ PCIE_D_RX-	Data into Module	Differential pair	Capacitive coupled – on Carrier
PCIE_D_RST#	Active low output to reset the PCIE_x device	Single ended	

Note: If PCIE_D shall be used as x1 link a clock buffer is needed as shown in **Figure 57 PCIe Clock buffer**.

5.4.1 PCIe x1 Device Down on Carrier

An example of a PCIe x1 “device down” on the Carrier is shown below. Coupling caps on the SMARC PCIe TX and PCIe reference clock pairs are not needed on the Carrier. Coupling caps on the SMARC PCIe RX pair (TX pair from the Carrier PCIe device) are needed. They should be placed close to the Carrier device PCIe TX pins. Use 0402 package 0.2 uF X7R or X5R dielectric discrete ceramic capacitors. Do not use a capacitor array. Place the parts in a way to preserve the symmetry of the differential pair. Usually they are placed close to the Carrier device TX pins to avoid a via transition.

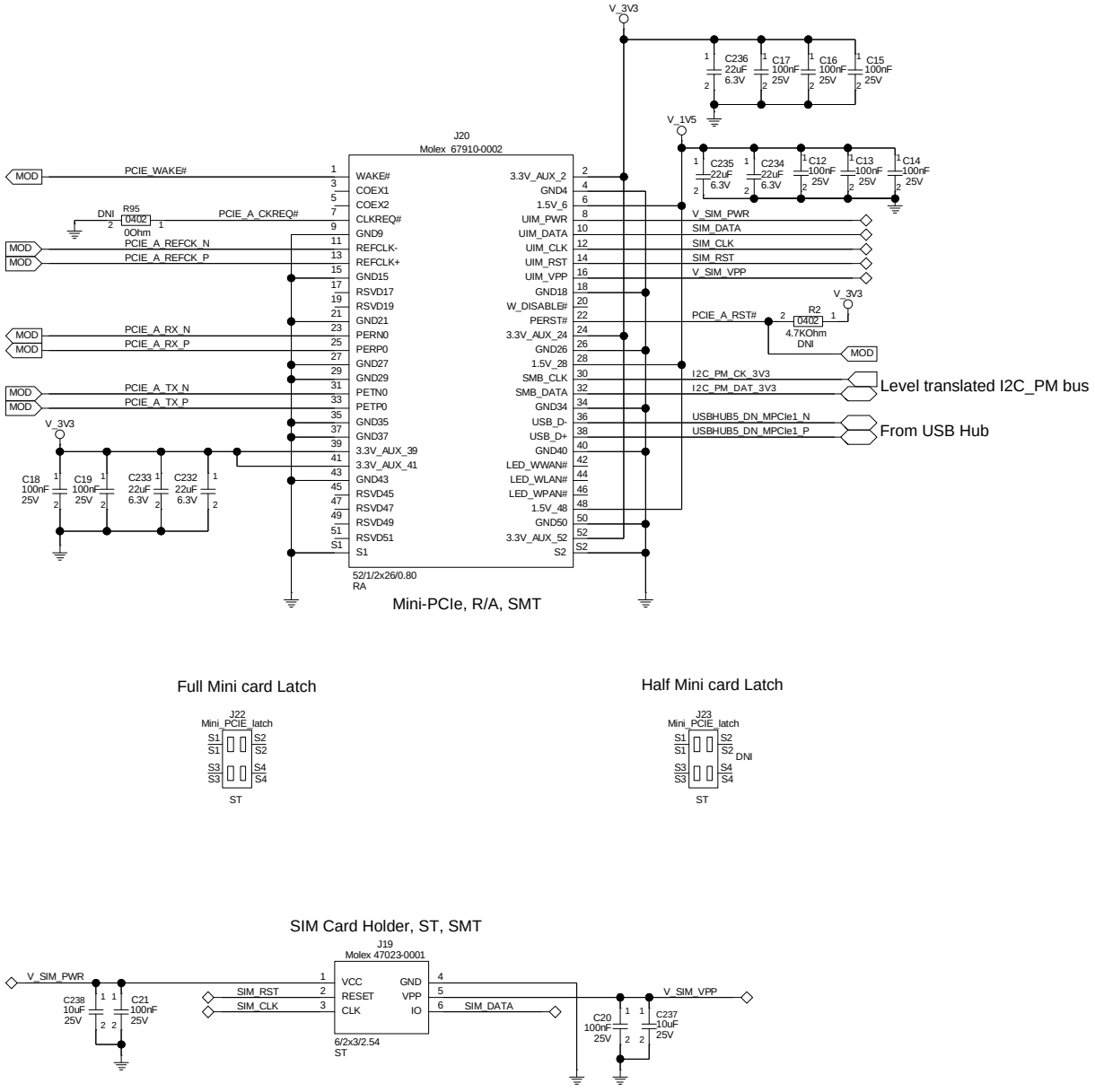
Figure 55 Interfacing a PCIe x1 Carrier Board Device



5.4.2 Mini-PCIe

A SMARC Mini-PCIe implementation example is shown **Figure 56 Mini-PCIe Slot**. Mini-PCIe cards are defined to have pins for PCIe x1 and also a USB interface. A given card generally uses only one or the other. If you know exactly what Mini-PCIe card you plan to use, it is possible to omit either USB or PCIe. Generally, Mini-PCIe 802.11 WiFi cards use the PCIe interface and cellular modem cards use the USB interface.

Figure 56 Mini-PCIe Slot



Full Mini card Latch

Half Mini card Latch

SIM Card Holder, ST, SMT

5.4.3 PCIe Reference Clock buffer

The SMARC 2.1.1 Specification calls for three copies of the PCIe reference clock pairs to be brought out of the Module. This clock is a 100MHz differential pair and is sometimes known as a "hint" clock. The clock allows the PLL in the target PCIe device to lock faster onto the embedded clock in the PCIe bit stream.

If the Carrier board implements only three PCIe devices or slots, then the PCIe reference clock pairs from the Module may be routed directly to that devices or slots. However, if there are four PCIe devices or slots on the Carrier Board, then one of the Module's PCIe reference clocks should be buffered.

Note: A device which meets the jitter requirements for the intended PCI Express generation must be used.

The IDT9DB233, IDT9DB433, IDT9DB844 have two, four and eight differential output replicas of the input clock, respectively. Each target device (PCIe "device down" chip, slot, Express Card slot, Mini-PCIe device, M.2 device, PEG slot) should get an individual copy of the reference clock. Similar parts may be available from other vendors.

The PCIe Clock buffers have both PLL and bypass modes. In some situations it is preferable to operate the clock buffer in bypass mode.

The reference clock pairs should be routed as directly as possible from source to destination.

The following notes apply to **Figure 57 PCIe Clock buffer**.

Each clock pair is routed point to point to each connector or end device using differential signal routing rules.

Each clock output pair in the example shown is terminated close to the IDT9DB433 buffer pins with a series resistor (shown as 33 ohms) and a termination to GND (shown as 49.9 ohms), per the vendor's recommendations. Other vendors may have different recommendations, particularly in regard to the source termination to GND.

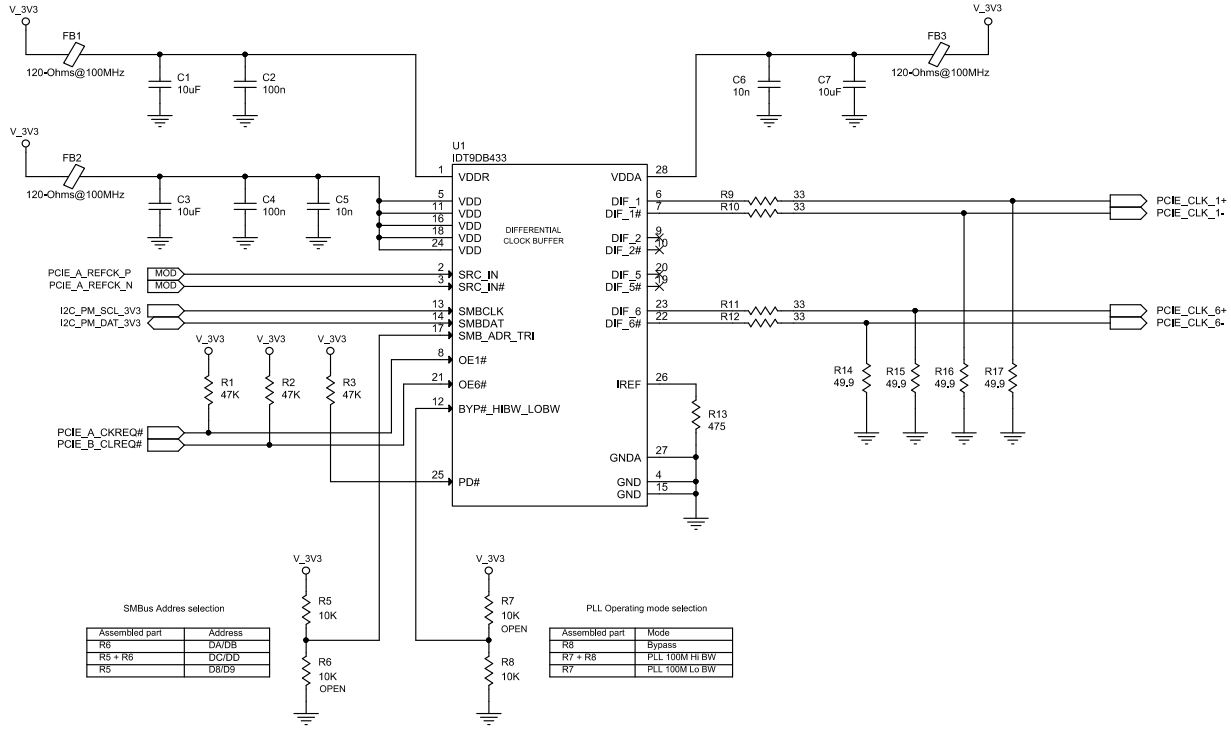
SMBUS software can enable or disable clock-buffer outputs. So the SMBUS pins of the clock buffer should be connected to the I2C_PM pins of the SMARC Module. Configuration resistors or alternatively the SMBUS also allow software to put the clock buffer into "Bypass Mode", which experience has shown is needed in some Carrier situations.

Disable unused outputs to reduce emissions.

The PCIE_A_CKREQ# and PCIE_B_CKREQ# should be pulled low to enable the corresponding clock buffer outputs. For applications in which power management is not a concern, these inputs may be tied low to permanently enable the outputs.

SMBCLK and SMBDAT need to be connected to a 3.3V I2C bus as described in **4.2.1 I2C Level Translation, Isolation and Buffering**.

Figure 57 PCIe Clock buffer



Note: The example in **Figure 57 PCIe Clock buffer** is supporting PCIe gen 3.

5.5 SATA

Serial ATA (or SATA) is a high speed point to point serial interface that connects a host system to a mass storage device such as rotating hard drive, solid state drive or an optical drive. Data and clock are serialized onto a single outbound differential pair and a single inbound pair. Data link rates of 1.5, 3.0 and 6.0 Gbps are defined by the SATA specification. A SATA link is AC coupled, but the coupling capacitors are defined in the SMARC specification to be on the Module, for both SATA transmit and receive pairs.

Table 11 SATA SSD Form Factors

Format	Notes
IC (chip level)	Smallest form factor. Densities of 512GB and more possible.
mSATA MO-300	Small form factor SATA module, defined in the SATA specification (search for “mSATA” in the specification). The mSATA form factor is roughly 30mm x 51mm x 3.5mm (see the specification for exact dimensions).
Slim SATA MO-297	Small form factor solid-state SATA modules that use a standard SATA connector (7 pin data / GND section and 15 pin power section). The connector is compatible with the connector used on larger format (2.5”) hard drives used in PC systems. Available in SLC and MLC versions. Form factor is defined by JEDEC MO-297.
CFast	Removable card format with SSD interface; similar to popular Compact Flash (parallel interface) cards. Form factor is roughly 36mmx 43mm x 3.6mm.
SSD 1.8”	Solid State Disk in traditional 1.8” format that was originally used for rotating drives
SSD 2.5”	Solid State Disk in traditional 2.5” format that was originally used for rotating drives

Table 12 SATA SSD Vendors

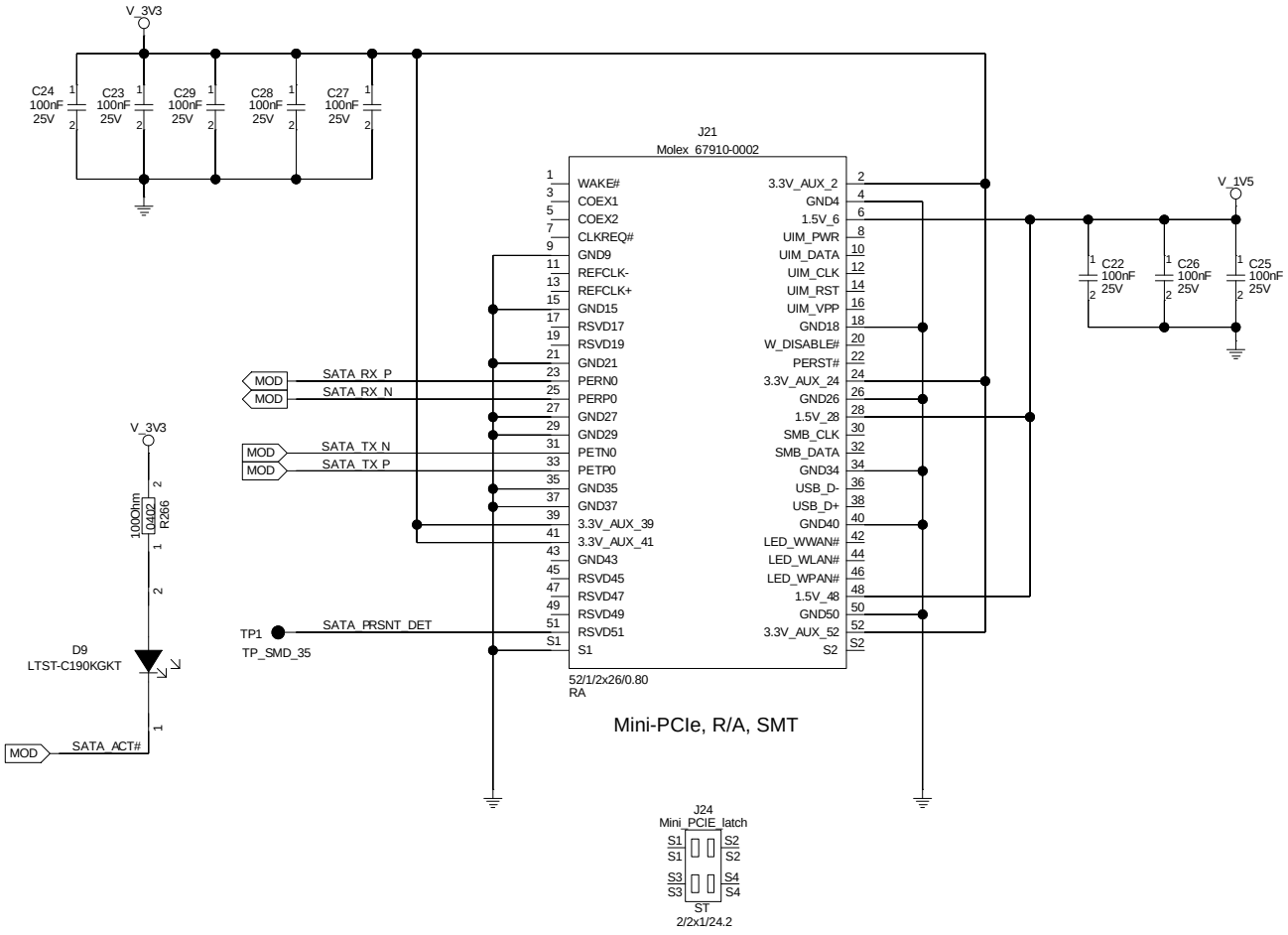
Vendor	Link	SATA Products
Greenliant	**www.greenliant.com**	Chip-level SLC and MLC NAND flash with SATA interface.
Innodisk	**www.innodisk.com**	mSATA / MO-300 Slim SATA / MO-297 CFast SSD 2.5”
Intel	**www.intel.com**	mSATA / MO-300 SSD 1.8” SSD 2.5”
SMART Modular	**www.smartm.com**	mSATA / MO-300 Slim SATA / MO-297 SSD 1.8” SSD 2.5”
Swissbit	**www.swissbit.com**	mSATA / MO-300 Slim SATA / MO-297

		CFast SSD 1.8” SSD 2.5”
Transcend	**www.transcend-info.com**	mSATA / MO-300 Slim SATA / MO-297 SSD 1.8” SSD 2.5”
Virtium	**www.virtium.com**	mSATA / MO-300 Slim SATA / MO-297 SSD 1.8” SSD 2.5”

5.5.1 mSATA / MO-300

A popular SATA form factor for SMARC systems is the mSATA / JEDEC MO-300. This is physically the same as a mini-PCIe card, and uses the same Carrier socket, but the mini-PCIe pinout is re-purposed for SATA use. A schematic example is shown below. The pin names within the J21 connector box outline below are the mini-PCIe pin names. The net connections outside the box show the appropriate connections for mSATA / MO-300 SATA use. Coupling capacitors are not needed on the Carrier SATA TX and RX pairs. mSATA / MO-300 SATA is described in the ***Serial ATA Revision 3.1*** specification document – search for “mSATA”.

Figure 58 mSATA / MO-300



According to the mSATA specification SATA_RX_P (positive signal) has to be connected to Pin 23 of the Mini-PCIe socket although this is used as a negative signal with PCIe. The same applies to SATA_RX_N and Pin 25 vice versa. Nevertheless SATA_TX_N and SATA_TX_P use the right polarity of the socket (Pin 31 and 33).

5.6 M.2

The M.2 form factor is a specification for mobile expansion cards and is supposed to replace the Mini PCIe cards and mSATA cards. The M.2 is a smaller form factor in both size and volume. It is a family of form factors that will enable expansion, contraction, and higher integration of functions onto a single form factor module solution.

PCIe, SATA, USB 3.0 and SDIO are provided through the M.2 connector. It is up to the manufacturer of the M.2 host or device to select which interfaces are to be supported. The M.2 connector has different keying notches that denote various purposes and capabilities of M.2 hosts and modules, preventing plugging of M.2 modules into feature-incompatible host connectors.

M.2 cards are available in various physical sizes, starting from 1630 wireless cards, up to 22110 or 25110 SSDs.

Carrier Board designers must provide a stand-off for each physical card size they would like to support.

The module stand-off should be directly connected to Carrier board's GND, as it is part of the M.2 Electrical and Thermal Ground Path.

The M.2 standard defines different pinouts that are separated by keys to avoid miss-plugging of cards. Some of the most widely used keys are:

5.6.1 B keying

M.2 Key B sockets support a wide range of add on cards, like SSDs, GPS and WiFi devices.

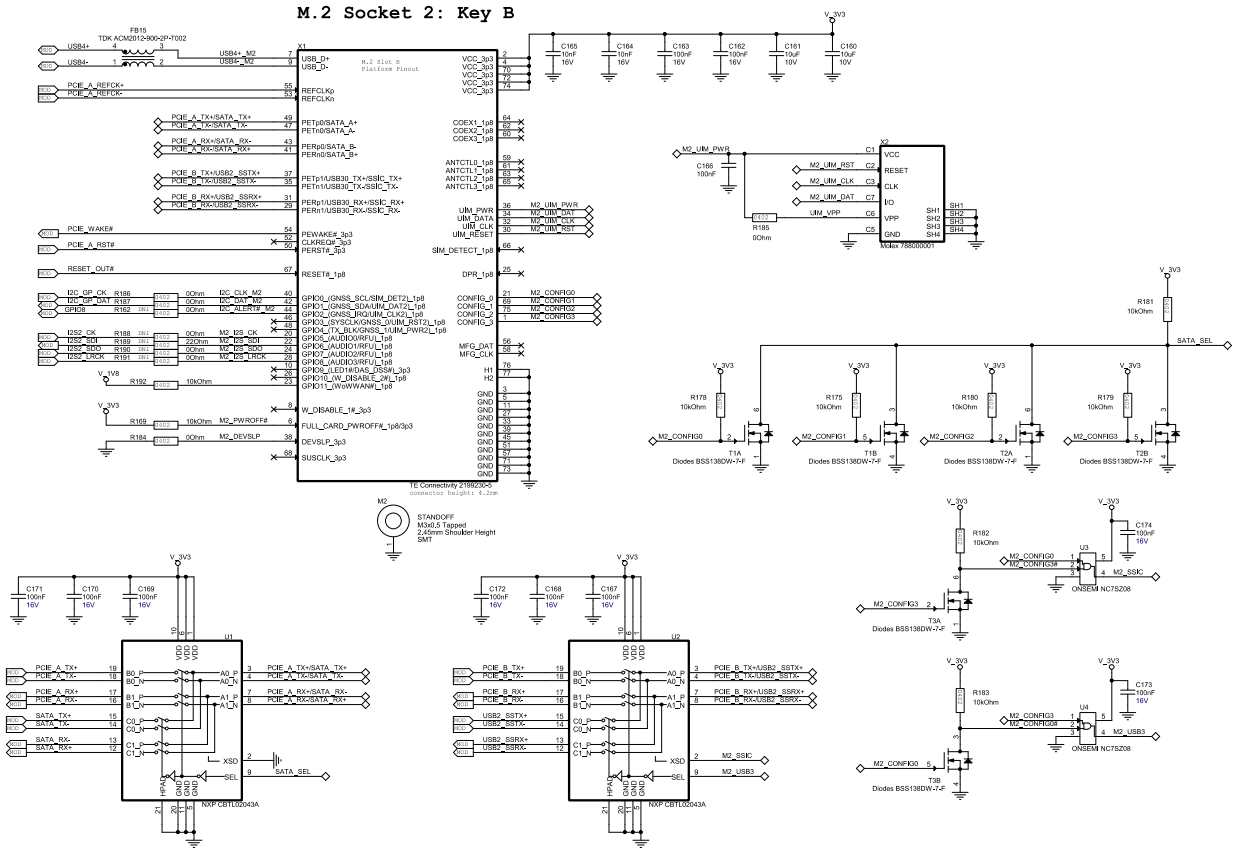
Some high-speed interfaces like SATA and PCIe share the same pins at the M.2 Key B connector.

The desired interface configuration can be decoded by CONFIG_[0-3] which are either tied to GND or left floating by the M.2 card.

At the time of writing, a majority of medium-speed (SATA) SSDs implement dual-keying which allows to plug them into Key B and Key M sockets.

High-End SSDs often come in a Key-M only format, as they rely on a PCIe x4 link.

Figure 59 M.2 Key B



5.6.2 M keying

M.2 Key M is intended for use with SSD Cards. The connection can either be done by PCIe x4 or a single SATA lane.

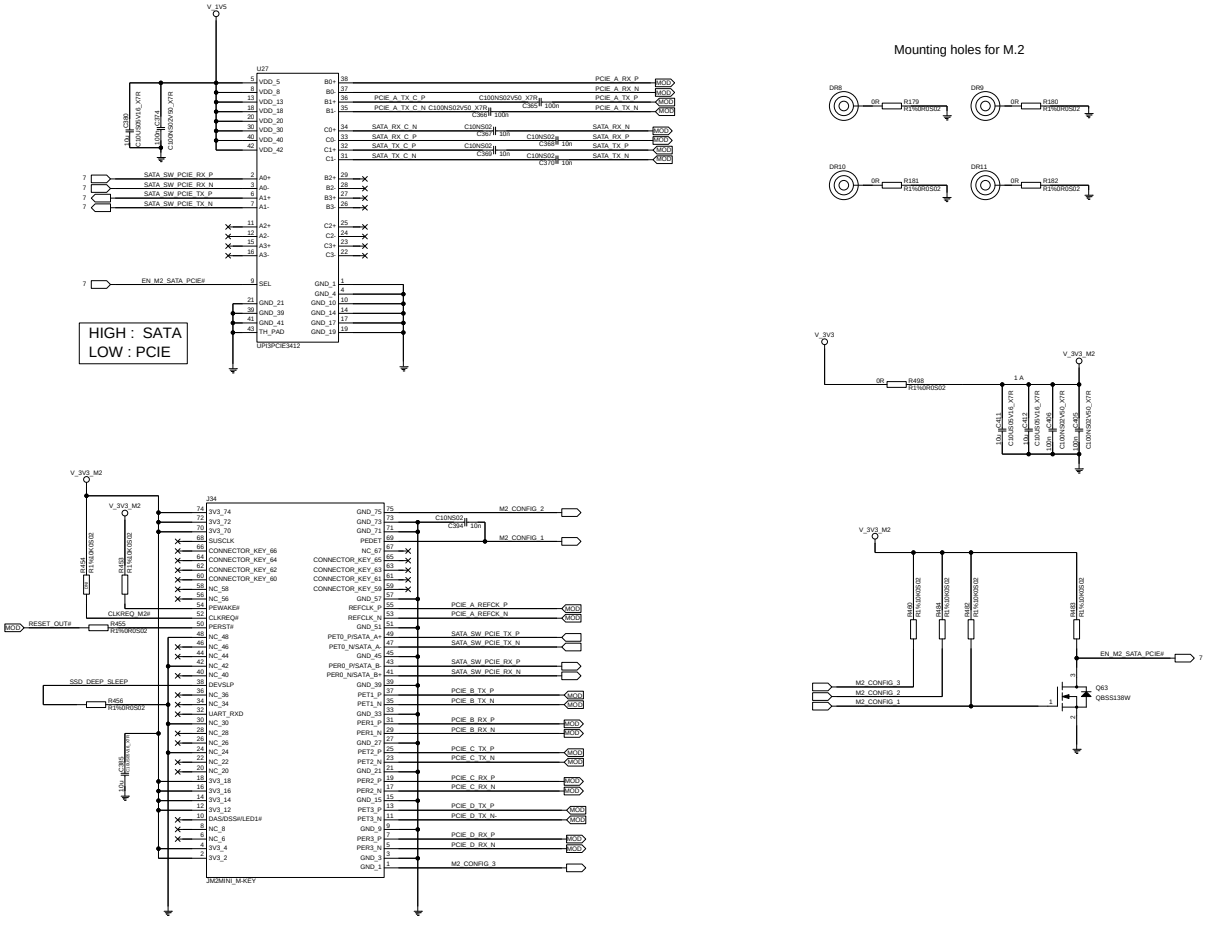
In this example schematic both PCIe and SATA is connected to the M.2 socket according to the M.2 specification.

The M.2 SSD decides with configuration pins, which interface should be used for the inserted SSD.

It is recommended to check with your SMARC Module vendor if PCIe x4 is supported by the used SMARC Module, if PCIe x4 SSD will be connected. This usage would consume all available PCIe lanes from the Module. Other PCIe devices could only be used if a PCIe bridge is implemented on the Carrier board. Both used interfaces by the M.2 SSD and the SMARC Module must match.

Note: In order to support x4 configuration a modified BIOS for x86 or Device Tree File for ARM designs from the Module vendor is required.

Figure 60 M.2 Key M

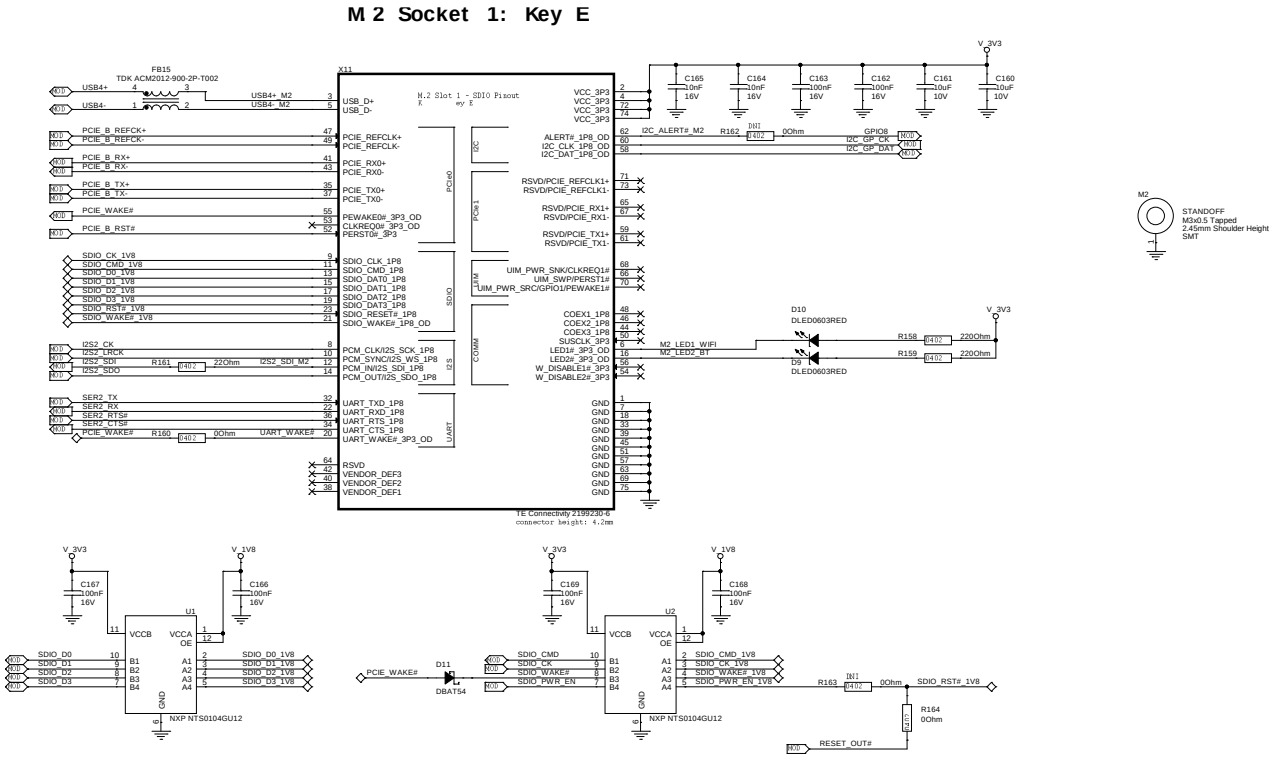


5.6.3 E keying

M.2 Key E is intended for use with Wireless Connectivity cards, which are WiFi / Bluetooth cards in most of the cases. WiFi is utilizing either PCIe or SDIO connection to the host system. It is recommended to check with your SMARC Module vendor if SDIO could be used for WiFi devices as well.

USB or UART+I2S are used to connect the Bluetooth Interface IC to the Host system. NFC capable add-in cards may also require an I2C connection. Please be aware that the I/O voltage of I2C was changed from 3.3V to 1.8V per ECN after the official M.2 specification release.

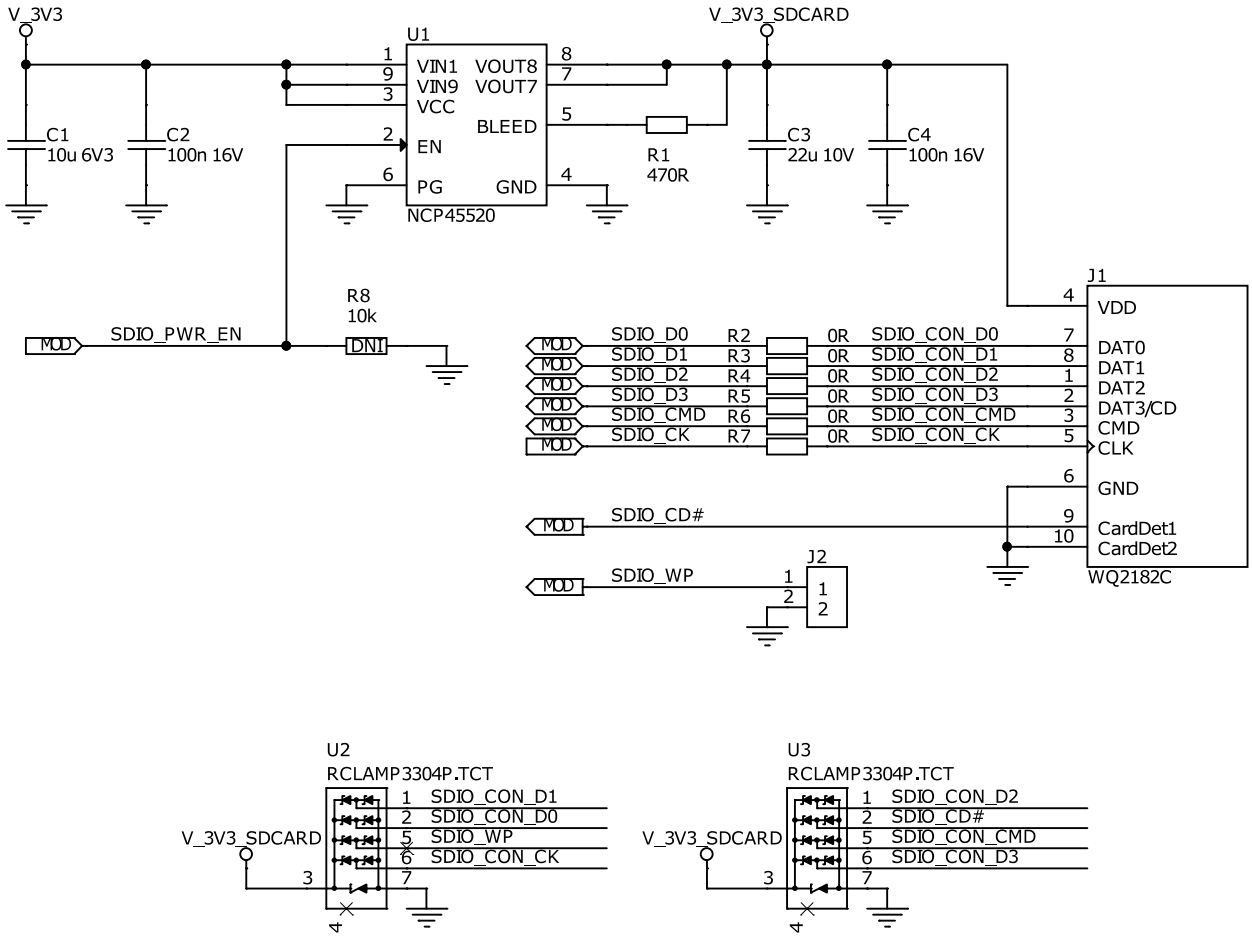
Figure 61 M.2 Key E



6 SDIO INTERFACE (FOR SD CARD)

The SD (Secure Digital) Card is a non-volatile memory card format used as mass storage memory in portable devices. The SD standard is maintained by the SD Card Association. SMARC Modules support SD cards over the SMARC SDIO interface. The interface may be used in a 4 bit or 1 bit mode. If used in 1 bit mode, the least significant bit (SDIO0) should be used. Most SMARC Modules offer a SDIO BCT boot and an SDIO OS boot. Since SD cards can (usually) be inserted and removed by the user, it is important to implement ESD protection on all the SD lines.

Figure 62 Micro SD Card Implementation



Note: The SDIO_WP is used on the Module with a PU. If **not considered** at the Carrier the uSD/ SD card will be **automatically write protected**. To enable to write to the card it is suggested to use a PD resistor with a value of 1k or below on the Carrier.

Note: Some SD card connectors do not offer a card detect switch. If the signal SDIO_CD is interpreted by the Module software it is necessary to pull this signal to Ground at the Carrier with a PD resistor of 1kOhm or lower.

Note: In order to switch the speed mode to SDR and DDR speed grades (with 1.8V signal voltages) a power cycle of the SD card is required. To achieve this the V_3V3_SDCARD voltage need to be dis-charged below 0.4V. This can be achieved by a power supply with bleed out feature as shown in tbd above.

7 CAMERA INTERFACES

The SMARC Module specification allows for up to four serial (MIPI CSI) cameras to be interfaced to the module. The defined CSI0 interfaces supports up to two differential data lanes (CSI0_D[0:1]+/- signals). CSI1, CSI2 and CSI3 may be implemented with up to four differential data lanes (CSIx_D[0:3]+/- signals) to support higher resolution cameras. The Module camera interface is at CSI voltage levels.

Note: As fill order the CSI1 interface has priority before CSI0.

CSI0 and CSI1 are available on the Carrier via the SMARC connector pins. CSI2 and CSI3 are available via extra feature connectors on the Module. Flat foil cables can be used to interface to the cameras. The preferred connector areas are defined as marked in **Figure 63 MIPI CSI feature connector placement (82x50mm² Module)** and **Figure 64 MIPI CSI feature connector placement (82x80mm² Module)**:

Figure 63 MIPI CSI feature connector placement (82x50mm² Module)

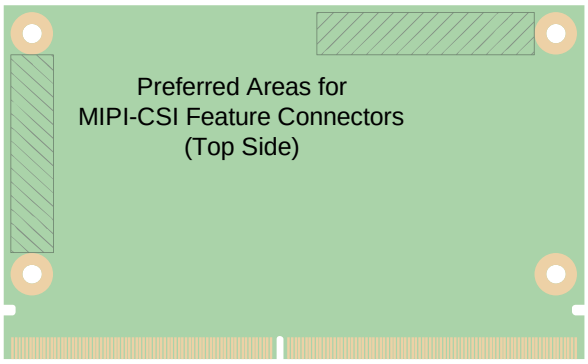
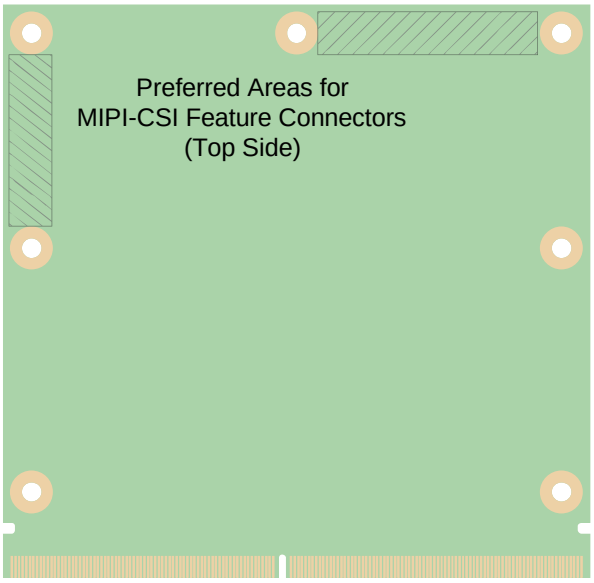


Figure 64 MIPI CSI feature connector placement (82x80mm² Module)



7.1 Camera Data Interface Formats

There are a wide variety of data formats that are used to convey camera data to a host system. A complete description of these formats is very much beyond the scope of this Design Guide. Briefly stated, camera data formats may be divided into two groups: “raw” and “processed”. The raw camera data formats need to be adjusted for camera and sensor specific characteristics (non-linearities, sensor pixel quirks, color corrections and so on). Using the raw format requires an additional level of software complexity that is beyond many users. Unless you have a specific need for a particular camera that outputs “raw” sensor data, it is best to stick with cameras that include an image processor on the camera module that convert the camera sensor data to a standard format such as RGB or YUV, JPEG or others. The “Bayer” format is one of the numerous raw formats that you may wish to avoid. A variation on the above is that some cameras offer “raw” RGB, meaning that the pixel data is sorted into RGB elements but sensor nonlinearities are not processed in the camera IC.

7.2 Camera Sensors and Camera Module Vendors

Table 13 Camera Sensors

Vendor	Link
ON Semiconductor	**www.onsemi.com**
OmniVision	**www.ovt.com**
Sony (Brand: Exmor)	**www.sony.com**

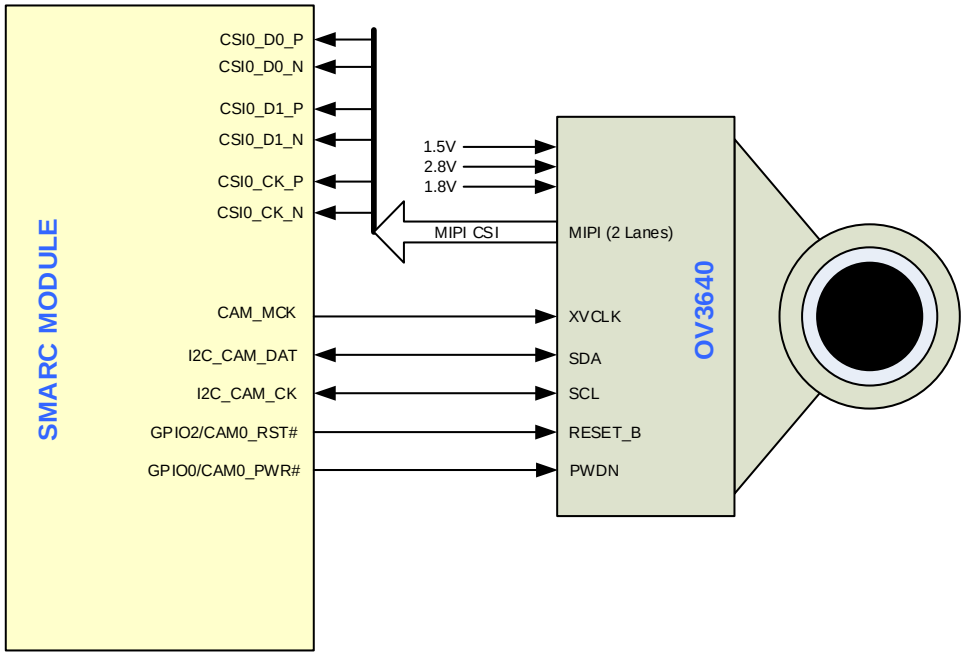
Table 14 Camera Module Vendors

Vendor	Link
Leopard Imaging	**www.leopardimaging.com**
KaiLap	**www.kailaptech.com**
Chicony	**www.chicony.com.tw**
Truly Opto	**www.trulyopto.com**
Sunny Optical Technology	**www.sunnyoptical.com/en/**
Sharp	**www.sharp-world.com**
e-con Systems	**www.e-consystems.com/**

7.3 Serial Camera Interface Example

The **Figure 65 Serial Camera Implementation** below illustrates a CSI implementation on a SMARC Carrier. The OV3640 is a 3.1 Mega-pixel CMOS sensor from OmniVision which supports both serial and parallel camera interfaces. Here, the output of the sensor is connected to CSI0 interface of the SMARC Module. I2C_CAM is the control interface used for configuring the sensor. CAM_MCK is the master clock output from the SMARC Module.

Figure 65 Serial Camera Implementation



7.4 Other Camera Options

SMARC systems have the option of using the dedicated SMARC camera interface pin set. For a dedicated system produced in high volume, this is likely to be the most cost-effective option. However, other options exist. USB cameras are becoming very popular. They enjoy good software support and are becoming more and more cost effective as time passes.

Cameras with GBE interface could also be considered so that there are multiple camera options available for different applications.

8 GPIO

It is possible to use up to 14 GPIOs coming from the SMARC Module directly. If these are not sufficient additional IO expander can be used to generate additional GPIOs.

8.1 SMARC Module Native GPIO

SMARC Modules support up to fourteen general purpose I/O pins: GPIO0 to GPIO13. Each of these can be configured as an input or output pin. The SMARC specification recommends the use of GPIO0 to GPIO5 as outputs and the use of GPIO6 to GPIO13, as inputs. SMARC Modules support up to seven dedicated GPIOs (GPIO7 to GPIO13). The other seven GPIOs are multiplexed pins supporting functions like Camera Power Enable, Camera Reset, Tachometer input, PWM output etc. SMARC Modules generally allow the GPIO to be configured to generate an interrupt.

GPIO0 to GPIO11 shall always be present.

GPIO12 and GPIO13 are optional. Please check the Module documentation for support or contact your SMARC Module vendor.

SMARC Modules use a GPIO voltage level of 1.8V.

8.2 GPIO Expansion

For a low cost, easy way to implement additional GPIO ports, see section **4.2.4 I2C Based I/O Expanders**.

9 CARRIER POWER CIRCUITS

9.1 Power Budgeting

One of the early steps in a SMARC Carrier design is to develop a power budget and a strategy for meeting that budget. All the power rails need to be identified and worst-case current consumptions listed. A spread-sheet is usually developed. The power circuits should be designed to meet the worst case numbers, but the actual system power consumption will usually turn out to be quite a bit less than the total indicated by the total worst case numbers for each individual rail. Once there is an understanding of the amount of power required, a plan can be developed for meeting the requirements. A sample power budget sheet is shown in the table below. This example is hypothetical and serves to illustrate the process. It assumes that the SMARC Module is to be supplied by a fixed 5V DC source. A variable battery power source would result in a different sheet.

Table 15 Hypothetical Power Budget Example – Part 1

	12V Current	5V Current	3.3V Current	1.8V Current	1.5V Current	Power	Notes
Display Backlight	0.6A					7.2W	
USB		2.0A				10.0W	4 devices
USB 3.0		1.8A				9.0W	1 device
SMARC Module		3.0A				15.0W	
Mini PCIe Module			1.0A		1.0A	4.8W	
Audio Circuits		0.5A		0.1A		2.7W	
Misc. Carrier Circuits			0.5A	0.2A		2.0W	
Current Subtotals	0.6A	7.3A	1.5A	0.3A	1.0A		
Power Totals	7.2W	36.5W	5.0W	0.5W	1.5W	50.7W	

The total shown is a worst case value, and power circuits should be designed to handle the worst case. However, experience shows that typical average system power consumptions are significantly less, on the order of 50% of worst case. The total above does not account for power conversion losses. These are added in a later section, when this hypothetical example is continued.

Many SMARC Module vendors offer evaluation platforms, and it is worth the time and effort to roughly prototype the target system with available hardware and software. This can validate power estimates and have other benefits, such as allowing performance benchmarks to be carried out before committing to the full system design.

9.2 Input Power Sources

Table 16 Input Power Source Possibilities

Power Source	Voltage	Notes
3.3V Fixed	3.3V +/- 5%	Possible, but not a common choice, as often there are significant power requirements for USB (5V at up to 500 mA for each external USB 2.0 port) and the display backlight supply (12V at up to 600 mA is common), requiring up (boost) conversion. Some SMARC Modules may not support 3.3V power input.
5V Fixed	5.0V +/- 5%	Common choice – allows some of the higher power consuming devices (USB, SMARC Module) to be fed directly without conversion. Other, lower current devices require power conversion.
12V Fixed	12V +/- 5%	Allows display backlight to be powered directly, without conversion (if the display backlight accepts 12V). Requires buck conversion of 12V to 5V for Module and for Carrier USB and other functions.
Power “Brick”	Various ranges available 6V, 9V, 12V, 14V	Various output levels are available. The voltage regulation from a power brick is often not good, and it is best not to rely on the brick output to feed any circuit that needs to be supplied with a voltage regulated over a relatively tight range. Usually the brick output voltage is down converted and regulated on a Carrier board design.
Battery - Single Level Lithium Ion Cell	3.6V nominal	4.2V fully charged; 3.0V discharged. Most SMARC Modules operate directly from this range (check with your vendor) if the current demand can be served by the battery.
Battery - Two Level Lithium Ion Cells	7.2V nominal	8.4V fully charged; 6.0V discharged
Battery - Three Level Lithium Ion Cells	10.8V nominal	12.6V fully charged; 9.0V discharged
Wide Range DC	10V – 30V (Typical)	Wide range input power supply is possible. Note that to handle higher voltages, parts rated for use at the higher voltages must be used.
Power Over Ethernet	48V	IEEE802.3af POE standard allows 12.5W load power IEEE802.3at POE standard allows 25.5W load power IEEE802.3bt POE standard allows up to 71W load power The POE supply output is transformer isolated from the GBE lines, with 1500V DC isolation. POE supply output voltages are design specific – 24V, 12V and 5V outputs are common.
Automotive	12V nominal	When the engine is off, the supply battery voltage is 12V nominal. During engine cranking, the supply can dip to 6V. When the engine is running, the DC level can be up to about 16V, with a 14.4V level being typical. Transients in

		excess of +/- 100V are common. A user may disconnect the battery and reconnect it with the polarity reversed. All in all, it's a harsh environment that needs careful attention. A basic strategy is to have an input network with good transient and reverse polarity protection, and then use a rugged switching supply that can handle an input range from 6V to 24V, and deliver a 5V output to the SMARC Carrier.

9.3 Power Budgeting, Continued – Fixed 5V Power Source

Once a power budget is in hand, a power architecture can be developed. Let's assume that the input power source is to be 5V fixed, and the power budget per voltage rail is as per the hypothetical example given in **Table 15 Hypothetical Power Budget Example** above. Next, one has to decide how to realize the various power rails. Here we assume that switch mode power converters are used to create all rails from the 5V source. The efficiency (or inefficiency) of the power converters must be accounted for, as shown in the following table.

Table 17 Hypothetical Power Budget Example – Part 2

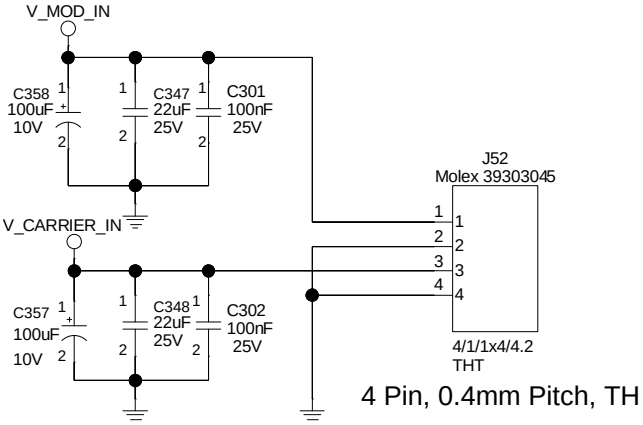
Voltage Rail	Current	Power	Derived From	Efficiency Assumption	Power From 5V Input	Current From 5V input rail
12V	0.6A	7.2W	5V (Boost)	90%	8W	
5V	7.3A	36.5W		100%	36.5W	
3.3V	1.5A	5.0W	5V (Buck)	90%	5.6W	
1.8V	0.3A	0.5W	5V (Buck)	90%	0.6W	
1.5V	1A	1.5W	5V (Buck)	90%	1.7W	
				Total	52.4W	10.5A

Other factors can make the process a bit more complex than this example. If some power rails are to be created with linear supplies from a higher voltage rail, for example, then the entire current used by the lower rail needs to be added to the current budget of the higher voltage source rail. If the primary source rail varies (such as from a battery) the extremes of the source rail must be taken into account.

9.4 Fixed 5V DC Power Input Circuit Example

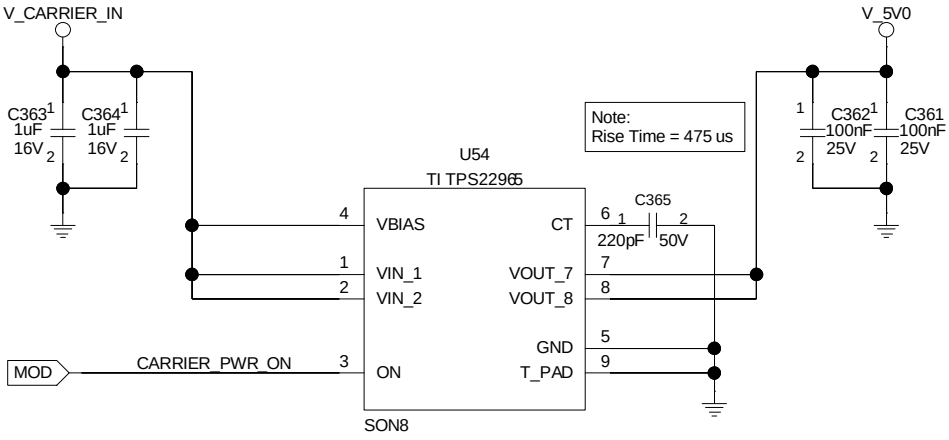
The power entry connector for this fixed 5V power source example is shown in the figure immediately below. There are two paths, given net names V_MOD_IN and V_CARRIER_IN. Both carry 5V in from a single bench supply. The nets are separated to allow separate current (and power) measurements of the SMARC Module and the Carrier board. If this separate measurement capability is not needed, then the separate entries could be combined into a single net.

Figure 66 5V Input Connector



The **Figure 67 5V, 6A Carrier Power Switch** illustrates a power switch used to hold off most Carrier board circuits from being powered until the Module asserts the “CARRIER_PWR_ON” signal. Some Carrier circuits, such as those involved in power management and those that are in the “Module Power Domain” as defined by the SMARC specification, may be powered whenever the Module has power, before (and after) the assertions of CARRIER_PWR_ON.

Figure 67 5V, 6A Carrier Power Switch



The following three figures illustrate buck (or step-down) switching converters that create 3.3V, 1.8V and 1.5V from the V_CARRIER_IN 5V power source. Since the power needs on these rails are modest, integrated switchers with internal power FETs are well suited to the job. They are physically small and robust. The parts shown are from Texas Instruments, although similar parts exist from other vendors.

The figures show three separate enables for the three supplies, with net name designations V_3V3_EN, V_1V8_EN and V_1V5_EN. Sources for these nets are not shown. These enable pins should be driven to the “enabled” state when signal CARRIER_PWR_ON is high. They could be driven by CARRIER_PWR_ON, or by V_5V0, or by other Carrier circuitry. If the situation demands aggressive power management, it may be desirable to have Carrier I/O circuits that allow the various enables to be brought low if the power rail is not needed. If this is done, the designer should arrange that the enables do not go high before CARRIER_PWR_ON is high.

The LEDs and signal FETs on the right side of the three figures are optional. The LED lights up as a status indicator when the power rail (V_3V3, V_1V8 or V_1V5) is up. The FET prevents leakage from the main power rails (V_MOD_IN and V_CARRIER_IN) when the switchers are powered down. Rail V_MOD_IN_LED ties to V_MOD_IN through a removable jumper. Removing the jumper prevents the LEDs from burning power in standby states (and in all states).

Figure 68 3.3V, 2A Buck Converter

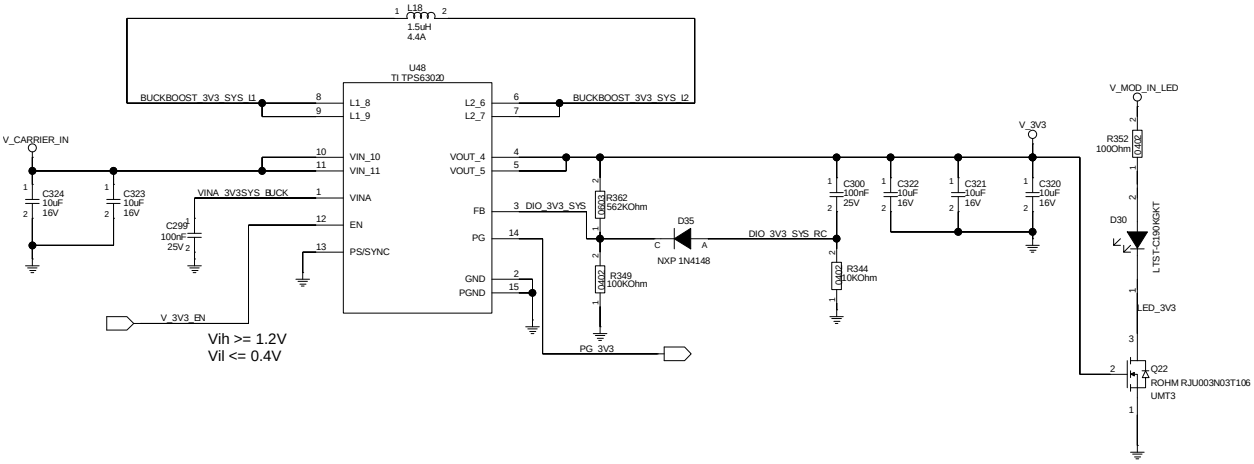


Figure 69 1.8V, 0.6A Buck Converter

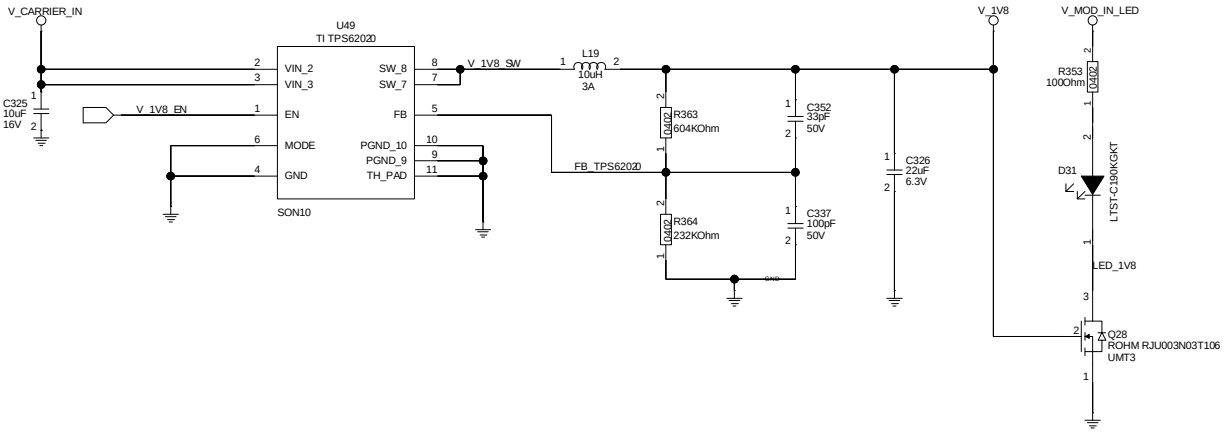
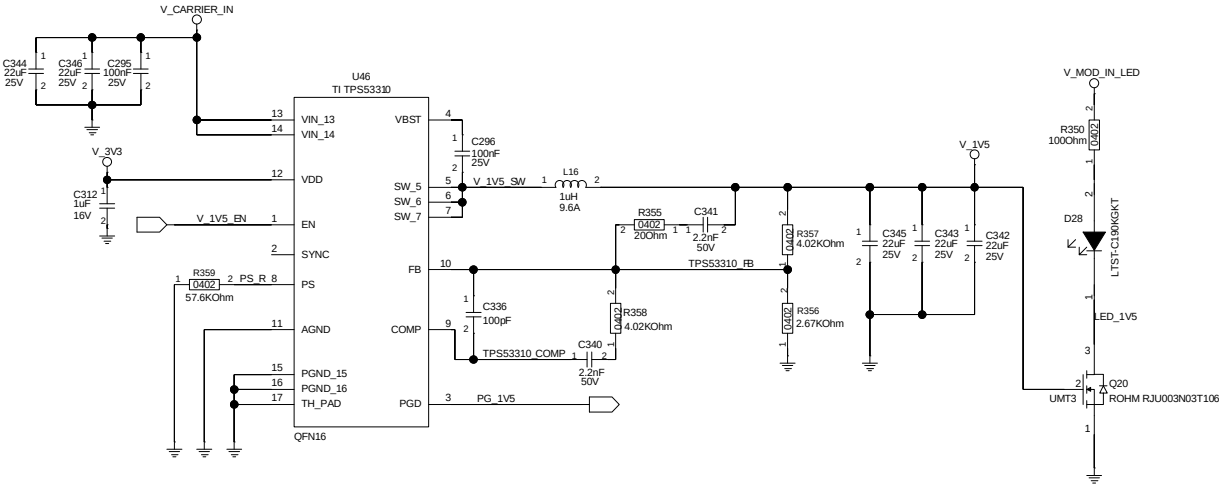
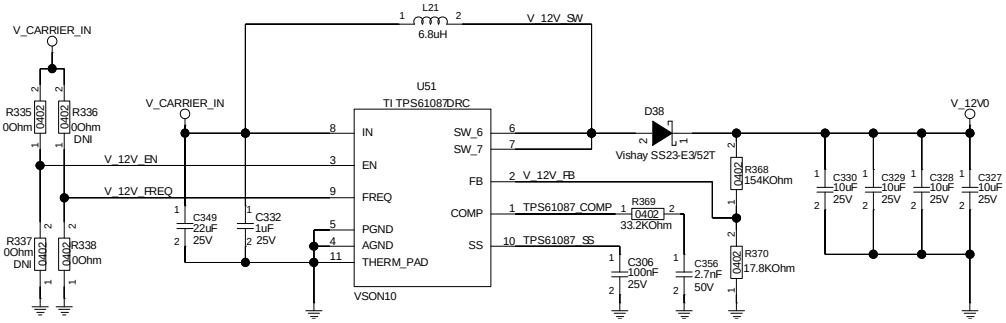


Figure 70 1.5V, 3A Buck Converter



Many LCD backlights require a 12V power source. If the system power source is a fixed 5V supply, or a battery supply well under 12V, then a boost converter circuit is needed. An example is shown here:

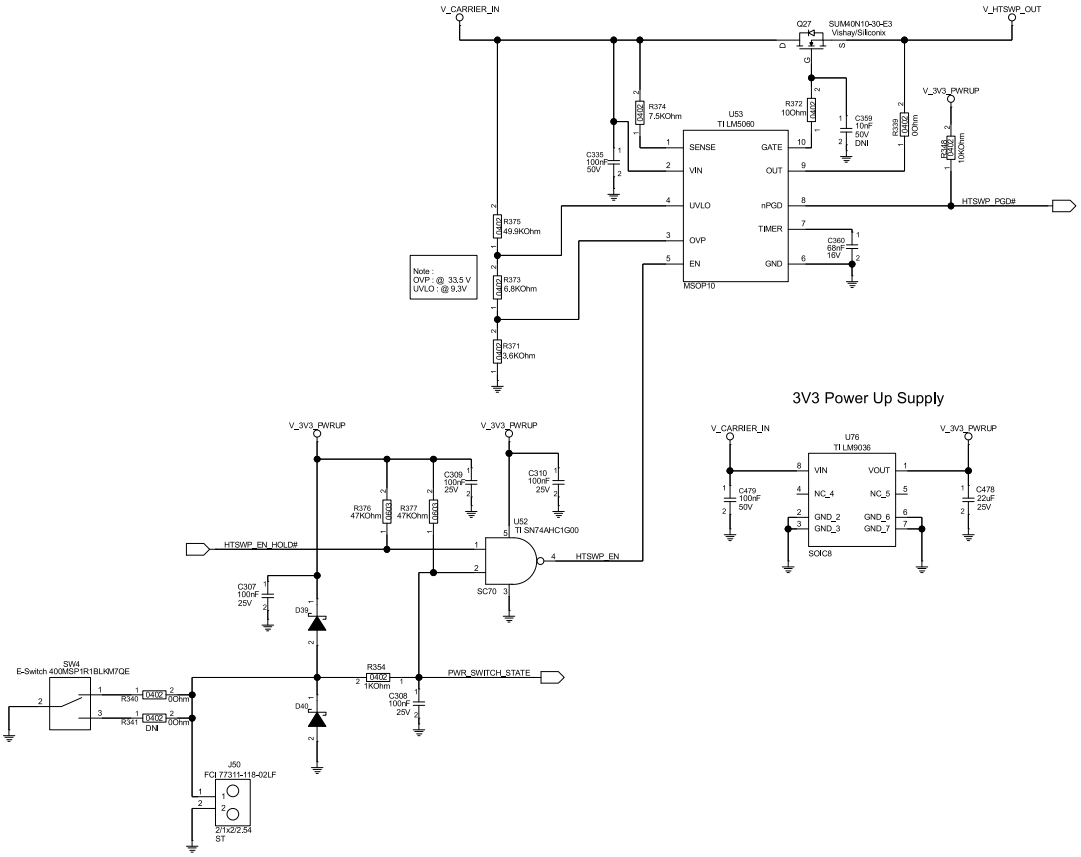
Figure 71 12V, 3.2A Boost Converter for Backlight Power



9.5 Power Hot Swap Controller

Hot swap controller circuits can be used to control the system power supply rise time. This may be desirable when plugging circuits in live to low impedance sources, such as a battery. The figure below illustrates a high-side protection controller circuit using TI LM5060. The N-Channel MOSFET isolates the input supply (V_CARRIER_IN) from rest of the board (V_HTSWP_OUT). The circuit limits the in-rush current and provides a power good signal once the output voltage reaches the input voltage. An option is provided to enable LM5060 (HTSWAP_EN) from a CPLD or other source as well as using a switch / jumper.

Figure 72 Hot Swap Controller

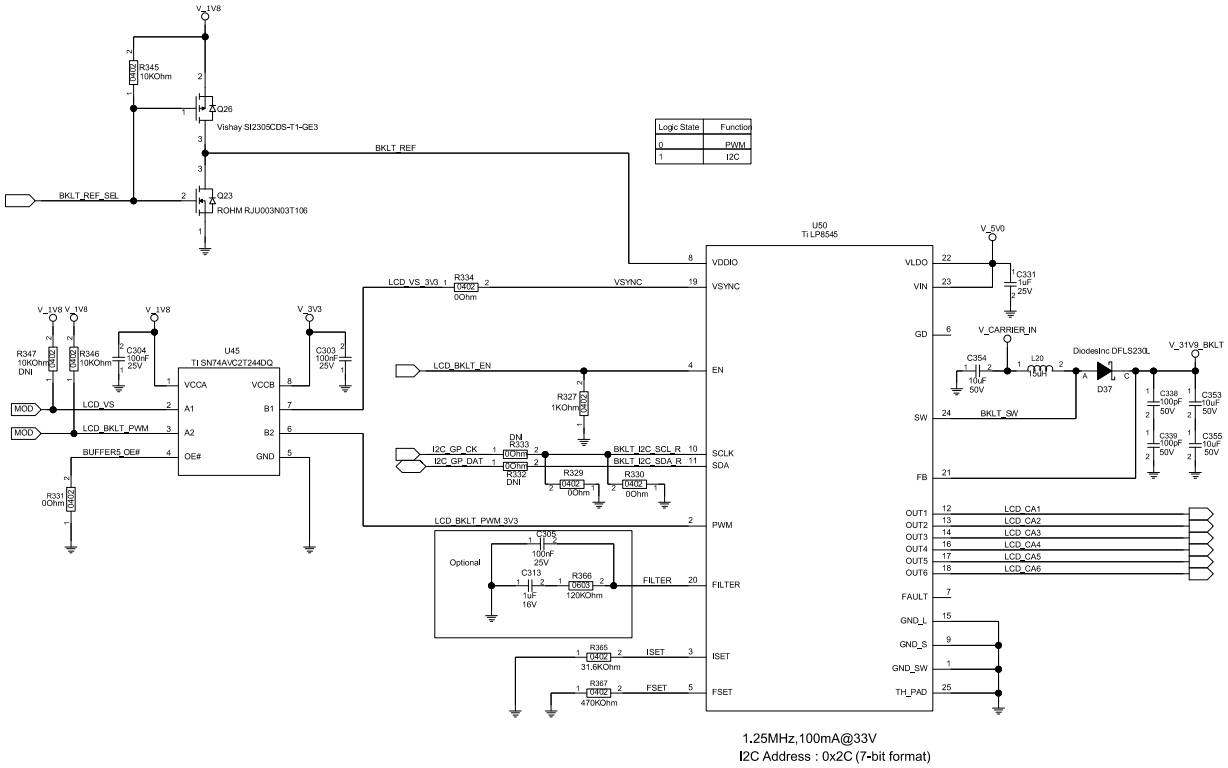


9.6 High Voltage LED Supply

Some LCD panels have multiple sets of series LED strings that are to be driven by a high voltage LED supply. Vendors such as TI and Analog Devices provide the ICs for these supplies. A schematic example using a TI high voltage LED supply is given below.

The LED brightness can be controlled either using PWM control (if the IC VDDIO pin is set LOW) or by I2C (if VDDIO is HIGH). A level translator needs to be used for signals VSYNC and PWM.

Figure 73 LP8545 LED Backlight Power



Note: The output voltage and current need to be defined for the related backlight. In this example 33V and 100mA is selected.

9.7 3.0V to 5.25V Power Input Example

The circuits shown in **Figure 74 5V, 2A Buck-Boost Converter** and **Figure 75 3.3V, 2A Buck-Boost Converter** illustrate buck-boost switching converters that generate 5V and 3.3V from the V_CARRIER_IN power source (3.0V to 5.25V). Since the power needs on these rails are modest, integrated switchers with internal power FETs are well suited to the job. They are physically small and robust. The parts shown are from Texas Instruments, although similar parts exist from other vendors.

The figures show separate enables for the 5V and the 3.3V supplies, with net name designations V_5V0_EN and V_3V3_EN. Sources for these nets are not shown. These enable pins should be driven to the "enabled" state when signal CARRIER_PWR_ON is high. They could be driven by CARRIER_PWR_ON, or by V_CARRIER_IN, or by other Carrier circuitry. If the situation demands aggressive power management, it may be desirable to have Carrier I/O circuits that allow the various enables to be brought low if the power rail is not needed with CARRIER_STBY# for example. In this case the signal would need to be inverted and a level shifter is needed. If this is done, the designer should ensure that the enables do not go high before CARRIER_PWR_ON is high.

Figure 74 5V, 2A Buck-Boost Converter

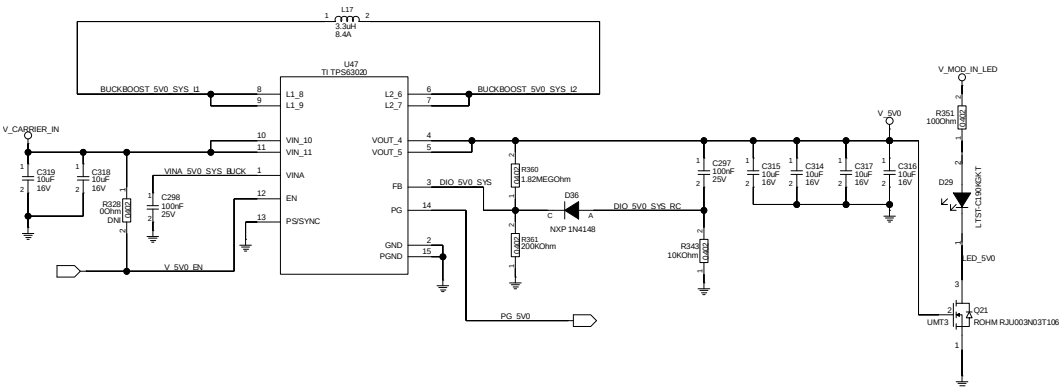
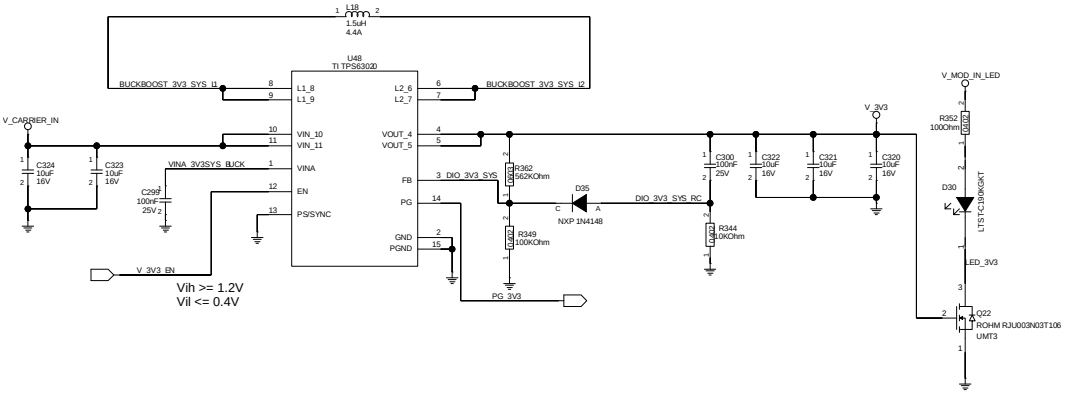


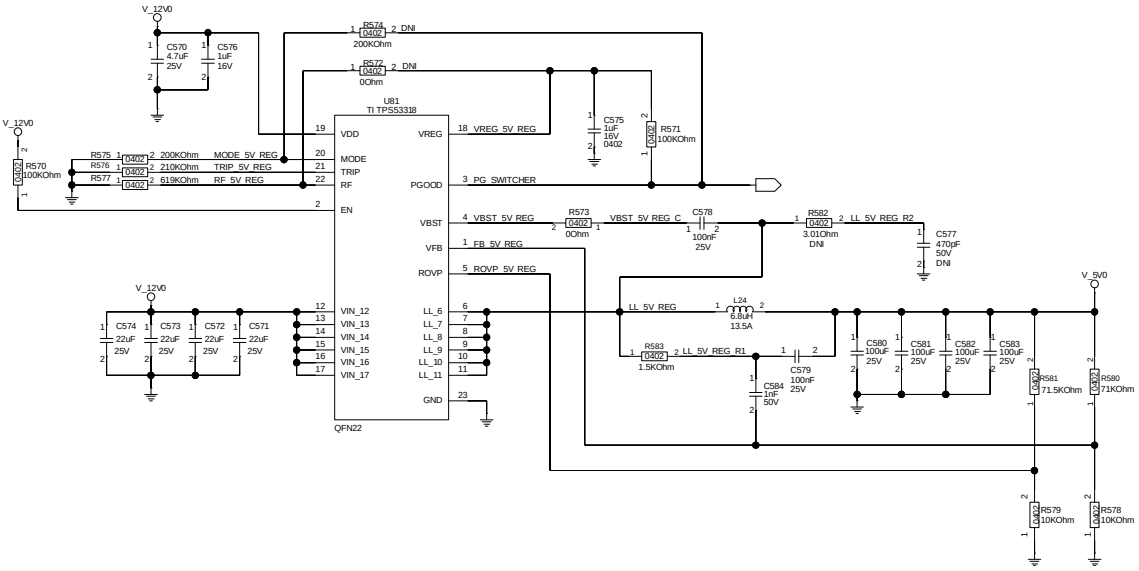
Figure 75 3.3V, 2A Buck-Boost Converter



9.8 12V Input

There are many choices for switching power supply circuits to step a 12V input down to lower voltages for SMARC Module and Carrier use. An integrated switcher possibility from TI is shown in the following figure.

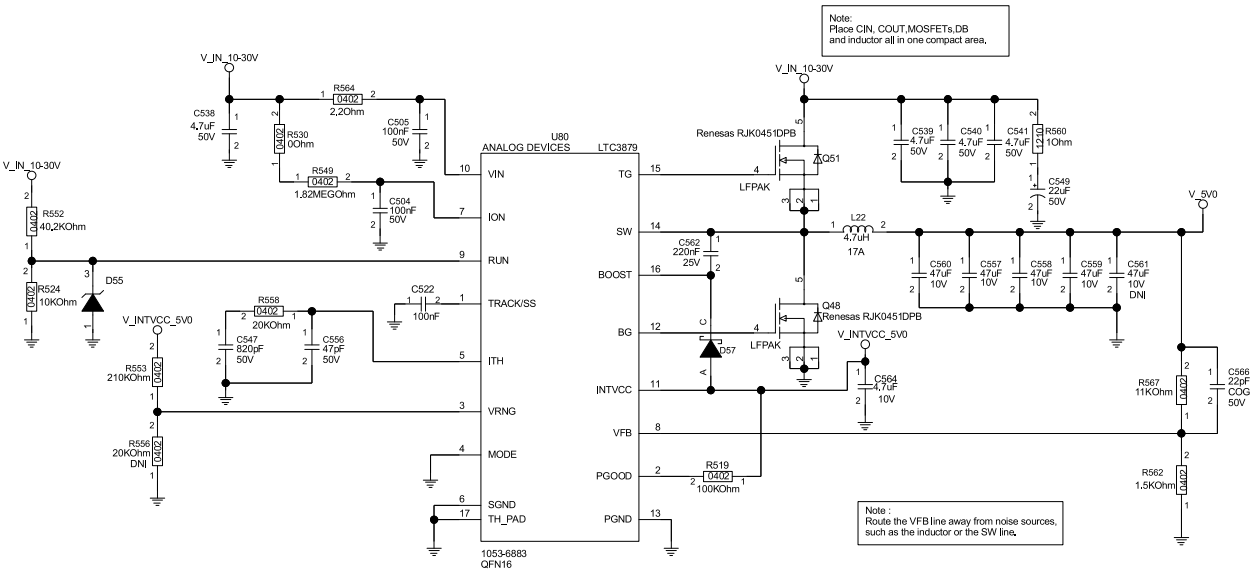
Figure 76 12V, 8A Step Down Switcher



9.9 Wide Range Power Input

In some applications it is desirable to allow for a wide range power input. This is the case in certain industrial and automotive settings. Since SMARC systems operate at low voltages (5V and under, apart from LCD backlight considerations), it is straightforward to implement a wide range buck converter. The figure below shows an example implemented with the Linear Technologies LTC3879 with an input range from 10V to 30V. Similar parts are available from other vendors. The Texas Instruments TPS40170 is another part to consider for this application. The TPS40170 allowable input range spans 4.5V to 60V. If you are targeting the higher input ranges, be sure that components exposed to the input voltage are adequately rated for that high voltage.

Figure 77 Wide Range 10-30V, 12A Power Input Switcher



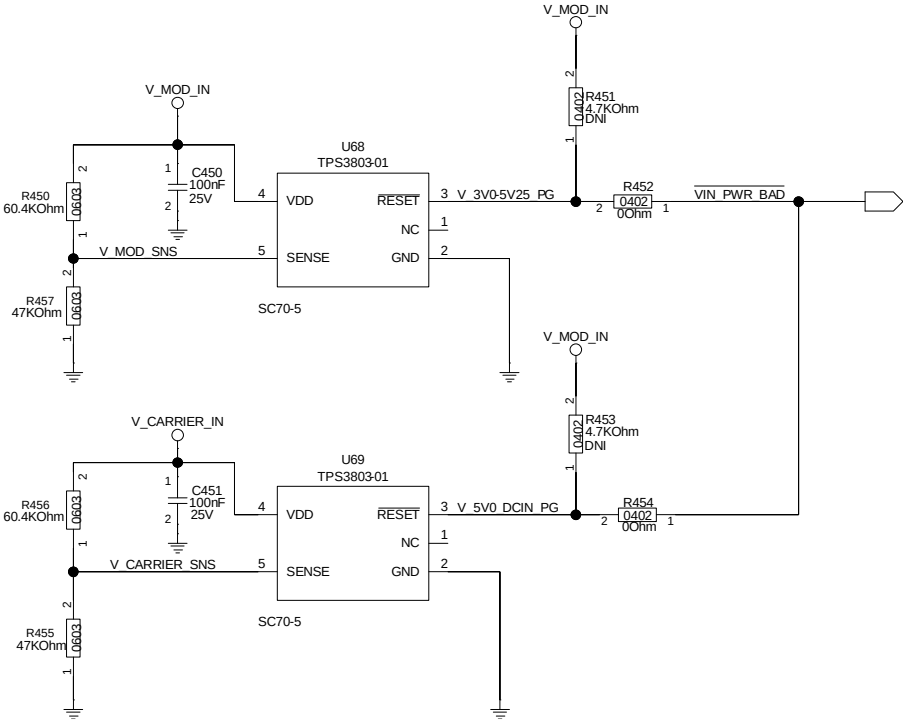
If the load on the Carrier 3.3V is high, it may be worth having a second wide input range switcher per the above figure, configured for the 3.3V output.

9.10 Power Monitoring

The SMARC specification document defines a VIN_PWR_BAD# input. If VIN_PWR_BAD# is held low by a Carrier or power supply circuit, the Module assumes that the source power is not ready and does not boot.

VIN_PWR_BAD# is typically generated by a power monitor / reset generator IC on the Carrier, such as those shown in the figure below. This figure shows two of them, although this is not really necessary if the Module and the Carrier circuits are powered by a single source and you don't want to keep them separate.

Figure 78 Power Monitor - Incoming Power



Note: Modules with fixed 5V input range expect the carrier to hold the VIN_PWR_BAD# low until the V_MOD_IN voltage is above 4.75V. Modules with wide input voltage support expect at least 3.0V for V_MOD_IN. Please also consider some time delay for the signal so that a inrush current may not bring the V_MOD_IN underneath the critical voltage levels.

9.11 Power Over Ethernet

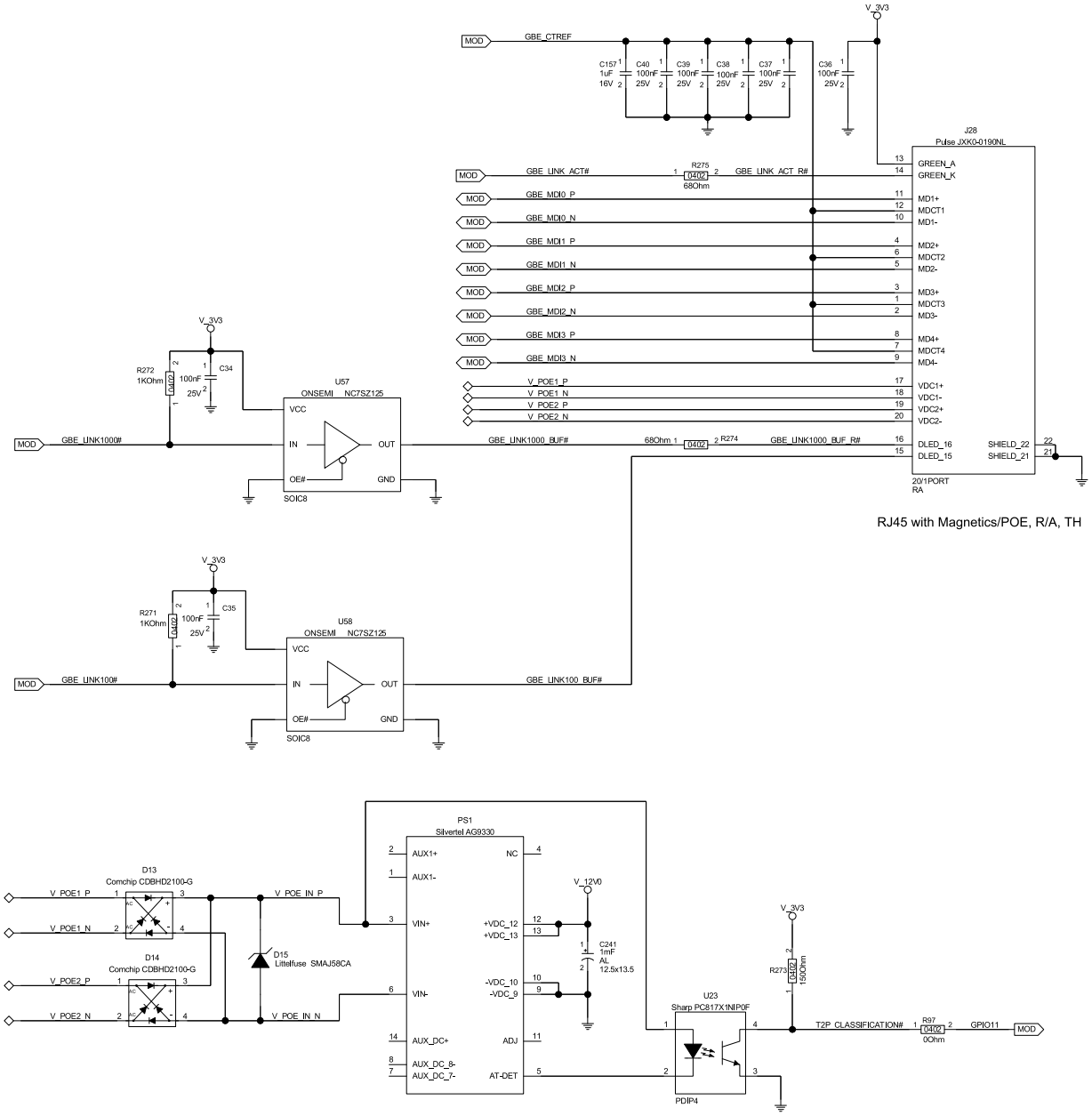
Power may be delivered to a SMARC system over the Gigabit Ethernet cabling, cohabiting with the GBE data traffic. The 48V DC power is extracted from the isolated GBE cabling by a diode bridge and a specialized transformer isolated switching power supply. POE is defined by the IEEE 802.3af – Type 1 (from 2003) and IEEE 802.3at Type 2 (from 2009) standards. The Type 1 payload power is limited to 12.5W and the Type 2 to a maximum of 25.5W. With the standard 802.3bt type 3 and type 4 (from 2018) payload power is defined as 51W (type 3) or 71W (type 4). These are the maximum power ratings for POE powered devices. Depending on the Carrier design (DC/DC circuitries and other losses) the real usable power will be smaller than the rating from the POE interface.

Many semiconductor vendors offer POE solutions. Designing a POE power supply for your device is a bit more complex than designing your average switching supply, as the POE supply is transformer coupled, there are isolation requirements to meet, and some sort of DC isolated feedback mechanism must be incorporated. If your product volume is high, it may be worth the trouble of implementing your own Carrier-down circuit. See Texas Instruments and Micro-Semi for POE device power supply IC solutions. Even if you don't go for the do-it-yourself approach, there are some very instructive Application Notes available from these vendors.

In many cases it is more straightforward to make use of a POE module, available from various vendors. One attractive POE module line comes from Silver Telecom (**www.silvertel.com**). IEEE 802.at and 802.bt compliant modules with output voltage options of 24V, 12V or 5V are available. The sample circuit below uses a Silvertel module with a 12V output. The 12V output cannot be fed directly to a SMARC Module – a step down converter would be needed. However, many SMARC systems incorporate LCD displays that utilize 12V backlights – hence the POE output option of 12V may make sense. If not, then the 5V POE output option could be considered (and the 5V POE module output can be fed directly to the SMARC Module).

Note that for POE use, a particular type of GBE jack is required, to get access to the DC power coming in over the isolated GBE lines. The example shown here uses a Pulse Electronics JXK0-0190NL GBE POE Mag-Jack. Similar parts are available from Bel-Fuse, Tyco and others – but beware of differing PCB footprints.

Figure 79 GBE with 30W POE



9.12 Li-ION Battery Charger

Caution: Improper battery charging can be a serious safety hazard. This section serves as a brief introduction to what is involved in designing a battery management system, but it is not enough to go on. Other source materials, from IC companies, battery vendors and the technical literature will be necessary for you to implement a safe and effective system.

Lithium Ion batteries have a fully charged cell voltage of 4.2V, nominal cell voltage level of 3.7V, and a depleted voltage of 3.0V. They are used in series combinations and parallel combinations. The voltages for various series combinations are shown in the following table.

Table 18 Lithium- Ion Battery Cell Voltages

Series Cells	Nominal Voltage	Fully Charged	Fully Depleted
1	3.7V	4.2V	3.0V
2	7.4V	8.4V	6.0V
3	11.1V	12.6V	9.0V
4	14.8V	16.8V	12.0V

Battery capacities are measured in Ampere-Hours (Ah). A fully charged battery with a 2Ah capacity can deliver 2A for 1 hour, or 1A for 2 hours and so on. The capacity is sometimes designated as ‘C’ in battery datasheets.

Lithium-ion batteries are typically charged in two phases: a constant current portion (for the deeply depleted battery) and a constant voltage portion (when the charging process nears completion).

The constant current charging is typically done at a maximum constant current equal to the battery capacity – for example, a 2Ah battery is charged at a maximum charging current of 2A. The constant voltage portion is done at the cell fully charged voltage – 4.2V for a single series cell, 8.4V for two series cells, and so on. The battery datasheet and vendor’s application notes should of course be consulted for more specific recommendations that apply to the situation at hand.

The battery temperature should be monitored during charging and use. The charging is disabled if the battery temperature exceeds a threshold set by the battery charger implementation.

9.12.1 Battery Charger Circuit Example

A battery charger implementation is shown in the following four figures. This example uses Texas Instruments parts. Similar devices are available from Analog Devices, Maxim integrated and others.

The first of the four figures show the overall charging system in block diagram format. The actual circuit schematics are shown in the three subsequent figures.

Caution: Many of the component values shown here need to be adjusted to suit the details of the situation at hand – the number of series cells, the battery capacity, the battery thermistor particulars.

With reference to the following four figures:

- FETs Q40 and Q46 form an analog switch that the charger IC can use to gate power from the external DC adapter into the system. Charger current is sensed through RS1. The FETs are turned off if the charger voltage is too high, too low or if the current draw is excessive.
- FET Q47 is turned on by the charger IC to allow battery power to be delivered to the target system.

- FET Q47 is off when Q40 and Q46 are on.
- The charger IC includes charge pumps to drive the N channel FET gates to a sufficiently high voltage to turn them on.
- The charger IC in this example has an internal switch-mode power supply, with internal high side FET, that are used when charging the battery. The external components of this supply are L1 and D53 in the diagrams.
- Battery charging current is measured through RS2.
- It is important to monitor the battery temperature. Usually an NTC (negative temperature coefficient) thermistor attached to or internal to the battery is used for this. The charger IC has support for the thermistor.
- A fuel gauge IC is used to collect information about battery charge levels. The gauge tracks current into and out of the battery, via sense resistor RS3. This sense resistor is in series with the battery GND terminal. The gauge has an I2C interface to the SMARC Module.
- There are three status signals from the charger system to the SMARC Module: CHARGING#, BATLOW# and CHARGER_PRSNT#.

Figure 80 Li-ION Battery Charger - Block Diagram

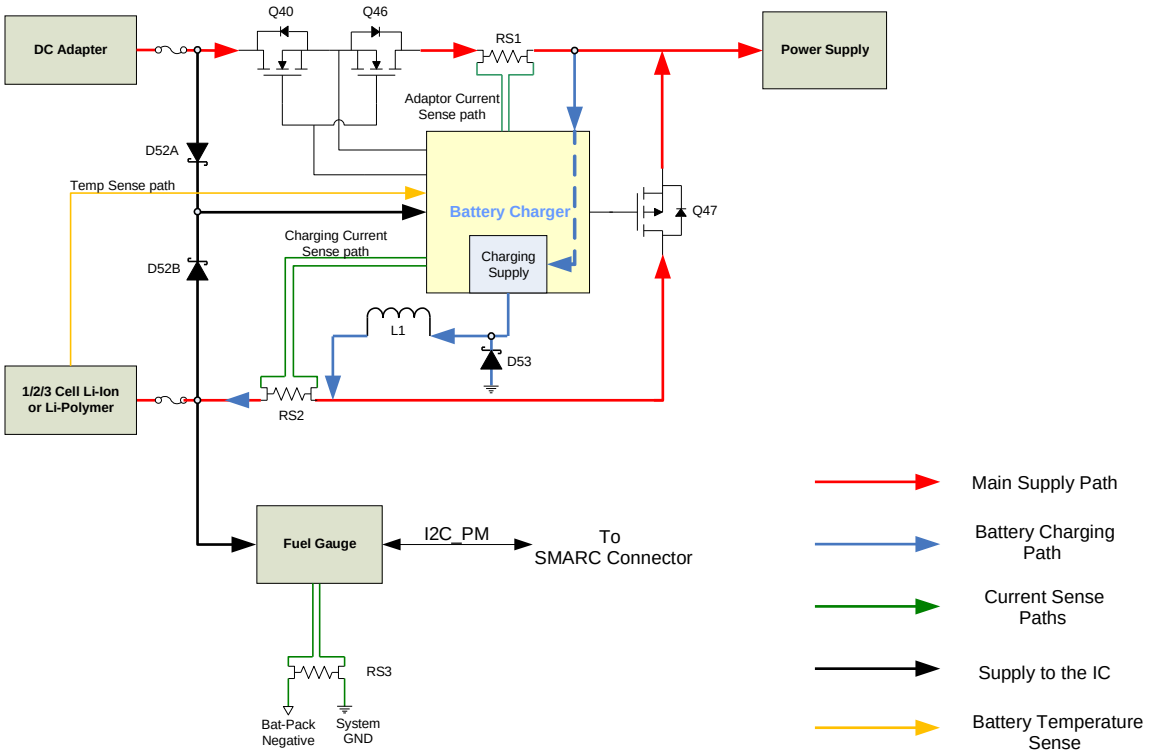
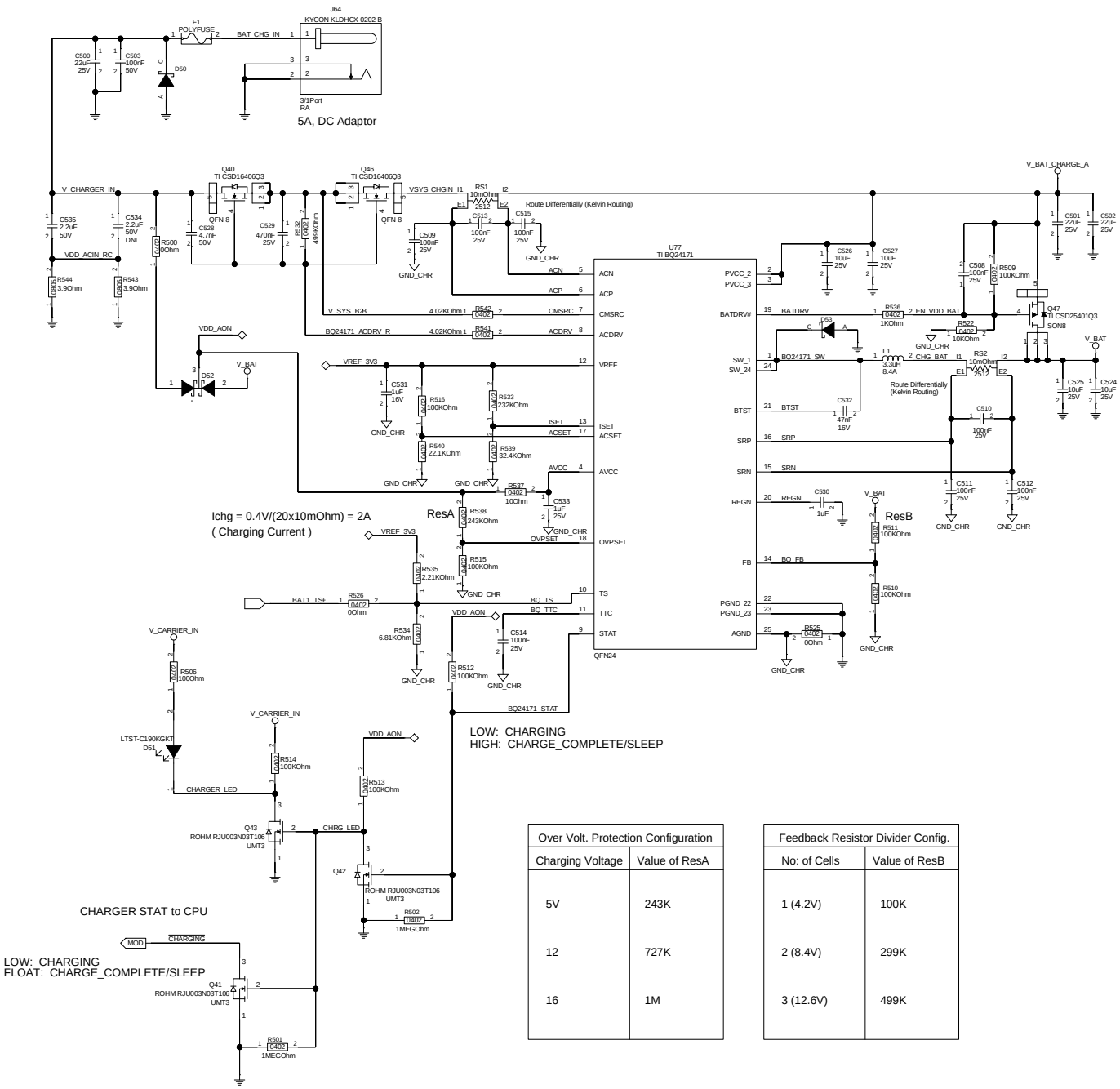


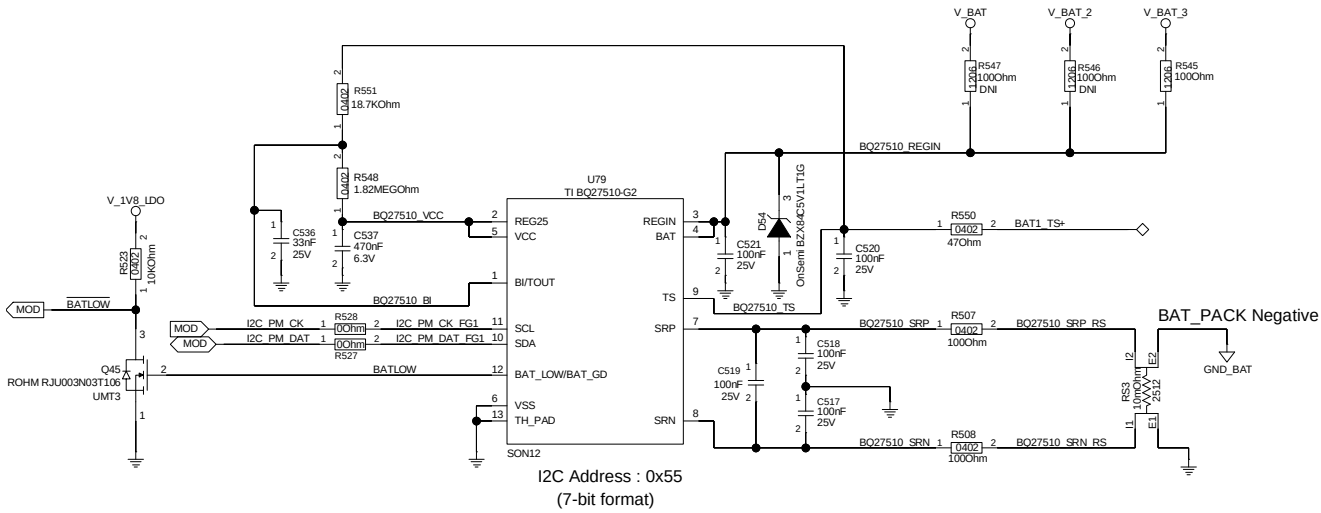
Figure 81 Li-ION Battery Charger - Schematic



Over Volt. Protection Configuration	
Charging Voltage	Value of ResA
5V	243K
12	727K
16	1M

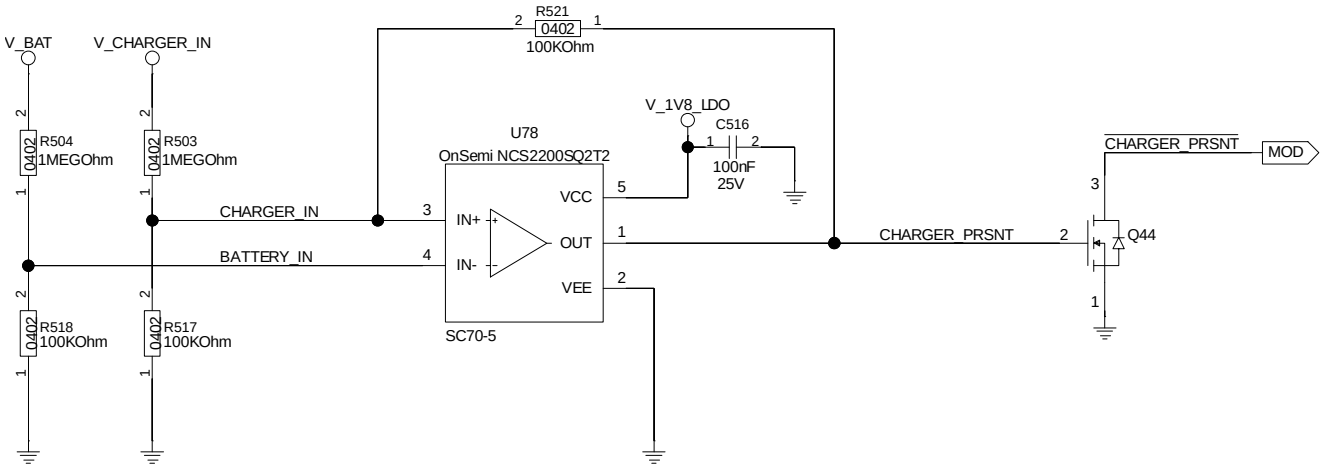
Feedback Resistor Divider Config.	
No: of Cells	Value of ResB
1 (4.2V)	100K
2 (8.4V)	299K
3 (12.6V)	499K

Figure 82 Battery Fuel Gauge



A comparator circuit such as the one shown below may be used to provide an indication to the SMARC Module that the battery charger power source is present. This circuit may be incorporated into some battery charger ICs.

Figure 83 Charger Present Detection



10 THERMAL MANAGEMENT

SMARC Modules generally have modest power dissipations. Nevertheless in a production environment, heat-sinking is usually necessary to keep the Module electronics die temperatures within limits, at the higher operating temperatures.

10.1 Heat Spreaders

Heat spreaders are available from SMARC Module vendors. Their purpose is to present a uniform thermal interface that is the same across various Module designs. A heat spreader is not a full heat sink – the heat spreader top surface is meant to be in contact with a system specific heat sink, such as the wall of an enclosure or other heat sink.

The figure below diagrams a typical heat spreader suitable for an 82mm x 50mm SMARC Module. The diagram plan view shows the heat spreader surface that the Module interfaces to. “TIM” is an abbreviation for “Thermal Interface Material” - a thermally conductive, compliant material to bridge the small gap between the heat-spreader surface and the surface of the system SOC. The Module is 82mm x 50mm, but the heat spreader is sized at 82mm x 42mm to allow the Module edge fingers to mate to the Carrier board MXM3-style socket. The heat spreader top, or “far side” surface, is 6mm above the Module PCB surface.

Figure 84 Heat Spreader Example – 82mm x 50mm Module

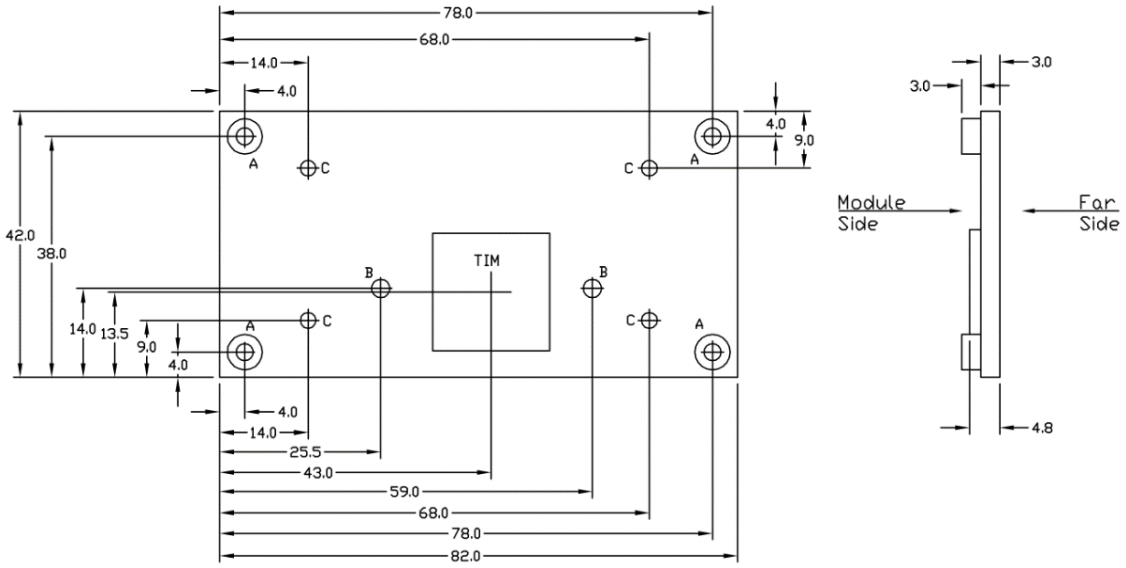


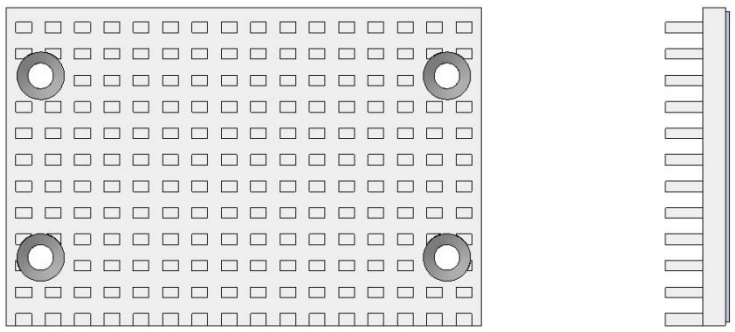
Table 19 Heat Spreader Hole Types

Figure Notation	Hole / Standoff Type	Notes
Holes marked 'A'	Clearance holes for M2.5 screws; 3mm tall clearance standoffs	These holes coincide with the SMARC mounting holes for 82mm x 50mm Modules
Holes marked 'B'		Module design specific holes and standoffs X-Y locations of these holes are also Module design specific. The TIM location is design specific.
Holes marked 'C'	M3 thread in heat spreader	These holes allow either a heat sink to be attached to the heat spreader, or they can allow the heat spreader (and the SMARC Module / Carrier assembly) to be secured to an enclosure wall or other heat-sinking structure.

10.2 Heat Sinks

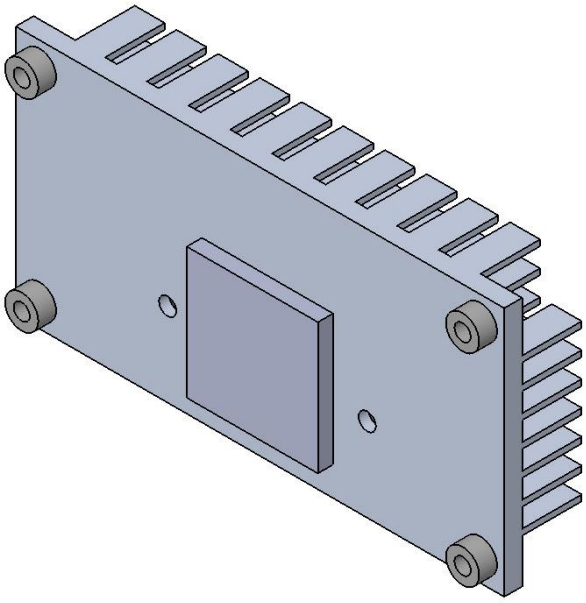
The figure below shows a heat sink that can be added to the heat spreader described in the figure above. This add-on heat sink attaches to the heat spreader through the 'C' holes marked on the heat spreader drawing above. A thermal interface material – thermally conductive paste, grease, or a gap pad – is needed between the heat spreader and the add-on heat sink, on the heat spreader "far" side.

Figure 85 Heat Sink Add-On to Heat Spreader



The best thermal transfer characteristics are usually obtained by a stand-alone heat sink. An example is shown in the following figure. The heat sink is secured to the SMARC Module through two design – specific interior holes (and design specific standoffs) that are straddling the TIM (the TIM in the figure is the square piece of foam that contacts the SMARC SOC). The four corner holes and standoffs coincide with the four SMARC Module holes (for 82mm x 50mm Modules). M2.5 screws pass through the heat-sink corner holes and standoffs, and pass through the SMARC Module, and catch the threads in the corresponding Carrier board hardware. Check with your SMARC Module vendor for the heat sinks that they offer.

Figure 86 Stand-Alone Heat Sink



10.3 Thermal Resistance Calculations

It is easy to estimate the thermal performance of a SMARC system if you have thermal resistance data from the vendors. The vendor sources can include silicon vendors, SMARC Module and Carrier board vendors and heat sink vendors.

Thermal resistance is a simple concept, analogous to Ohm's law and electrical resistance. Thermal resistance is expressed in degrees Celsius per Watt (˚C/W). If a particular thermal interface has a thermal resistance of 8 ˚C/W and the source device dissipates 4W, then there will be a temperature rise of 8 * 4 = 32 ˚C across that interface.

Some hypothetical thermal parameters are given in the table below, followed by some sample calculations for various situations. The calculations are just estimates, which can be useful for design guidance. The estimates should be followed up by measurements on physical samples. It may be useful to use thermal CAD simulations as well – after the "back of the envelope" calculations and before building hardware.

Table 20 Hypothetical Thermal Parameters

Parameter	Symbol	Value (Hypothetical)
Max SOC junction Temperature(Tj)	$T_{J\text{-}MAX}$	90 °C
Thermal Resistance, CPU Junction to ambient (θ_{JA})	θ_{JA}	12 °C/W
Thermal Resistance, CPU Junction to case (θ_{JC})	θ_{JC}	0.4 °C/W
TIM interface (CPU to heat spreader or sink)	θ_{TM1}	0.5 °C/W
Heat Spreader	θ_{HS}	0.1 °C/W
TIM interface (heat spreader to add-on heat sink)	θ_{TM2}	0.4 °C/W
Add-on Heat Sink - still air (natural convection)	θ_{HS1}	4 °C/W
Stand-alone Heat Sink – still air (natural convection)	θ_{HS2}	3 °C/W
SOC maximum power dissipation	$W_{SOC\text{-}MAX}$	5W
Maximum Environmental Temperature	$T_{OP\text{-}MAX}$	To be calculated

Sample Calculations Using Hypothetical Thermal Parameters

No heat sink at all

$$T_{OP\text{-}MAX} = T_{J\text{-}MAX} - \theta_{JA} * W_{SOC\text{-}MAX}$$
$$= 90 - 12 * 5 = 30\ °C$$

Heat Spreader + Add-On Heat Sink

$$T_{OP\text{-}MAX} = T_{J\text{-}MAX} - (\theta_{JC} + \theta_{TM1} + \theta_{HS} + \theta_{TM2} + \theta_{HS1}) * W_{SOC\text{-}MAX}$$
$$= 90 - (0.4 + 0.5 + 0.1 + 0.4 + 4) * 5 = 63\ °C$$

Heat Spreader + Stand-alone Heat Sink

$$T_{OP\text{-}MAX} = T_{J\text{-}MAX} - (\theta_{JC} + \theta_{TM1} + \theta_{HS2}) * W_{SOC\text{-}MAX}$$
$$= 90 - (0.4 + 0.5 + 3) * 5 = 70.5\ °C$$

11 CARRIER PCB DESIGN RULE SUMMARY

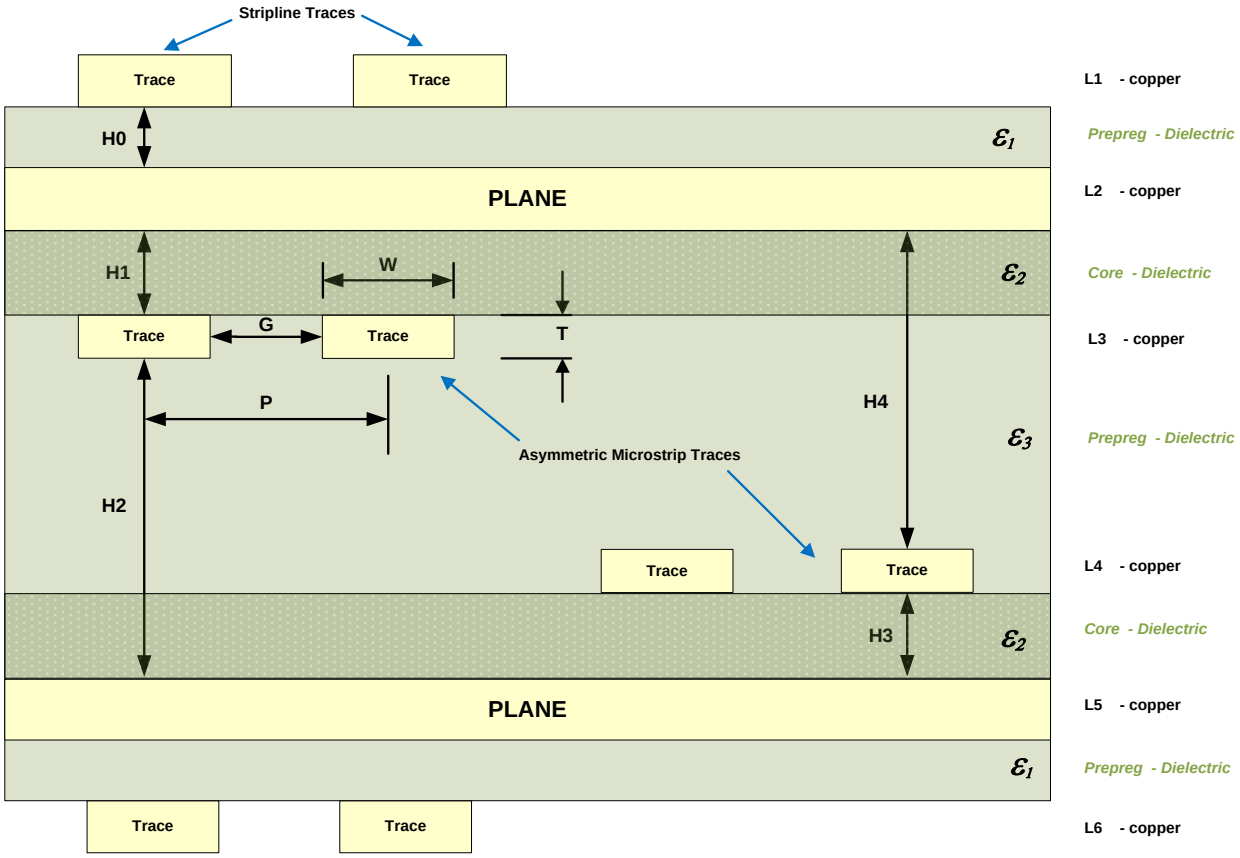
11.1 General – PCB Construction Terms

The Table and Figure below serve to define and illustrate some terms used in describing PCB construction and in trace impedances.

Table 21 PCB Terms and Symbols

Term / Symbol	Definition
Stripline	Outer layer traces routed a fixed distance above an internal plane layer
Asymmetric Microstrip	Inner layer signal traces, mounted a fixed distance to a Primary Reference Plane (H1 or H3 in the figure below) and mounted a larger distance to a Secondary Reference Plane (H2 or H4 in the figure)
H	Distance (or “height”) of a trace to the reference plane(s) – H0, H1, H2 etc. in the figure
W	The width of the trace. Outer layer traces generally need to be a bit wider than inner layer traces to meet the same impedance. It is best to arrange that all inner layer traces for a given impedance class have the same width.
T	The thickness of the trace. Inner layer traces are generally thinner than outer layer traces.
G	The gap (or space) between two traces that are part of an edge-coupled differential pair.
P	The pitch (or center-to-center distance) between two traces that are part of an edge-coupled differential pair. P = G + W for a given differential pair. A fairly common mistake in PCB design and fabrication is to get the pitch and the gap confused.
Clearance	(Not shown in the figure) The distance to “other” traces and features (vias, holes, pours) on the same layer
ε_1 ε_2 ε_3	The dielectric constants of the materials used in the PCB construction
Zo	Trace impedance
SE	Single Ended – trace that is single ended, not part of a differential pair
DE	Differential Ended – trace pair that are used for differential signaling

Figure 87 PCB Cross Section – Striplines and Asymmetric Microstrips



11.2 Differential Pair Cautions

Modern high speed interfaces (CSI, GBE, HDMI, LCD LVDS, PCIe, SATA and USB) must be routed as differential pairs over a ground plane. They should be routed as a pair on the same layer (edge-coupled pairs) and not as pairs on different layers (known as broad-side coupled pairs) that follow the same X-Y path. There should be a minimum of layer transitions – ideally, just two (SMARC connector to internal layer, and internal layer to the destination connector or IC).

For edge coupled differential pairs, there are several parameters of interest:

- Differential impedance: the impedance of the trace pair as seen by a differential driving source.
- Single impedance: the impedance of one of the traces in the pair, if it were removed from the pair and driven by a single ended source.
- Gap: the inside edge to inside edge spacing between the traces in a differential pair. Labeled ‘G’ in the figure above.
- Pitch: the center-to-center distance between the pairs in a differential pair. Labeled ‘P’ in the figure above.

It is fairly common for people to mix up the Gap and the Pitch. Make sure you don’t make this mistake.

11.3 General Routing Rules and Cautions

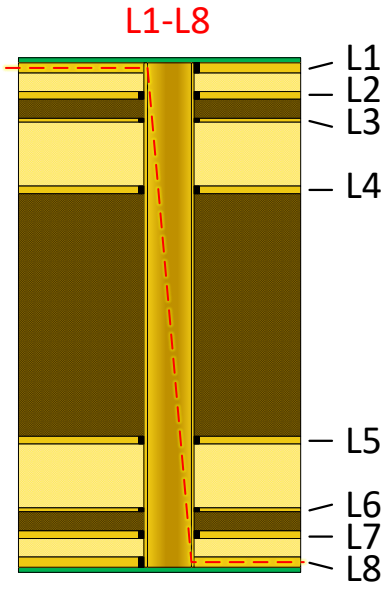
- High speed differential signals must be routed as differential pairs.
  - Keep the pairs symmetrical
  - Stubs are not allowed
  - Avoid tight (right angle) bends
  - Match the pair lengths, on each layer used
- Routing with reference to a GND plane is preferred:
  - If GND plane referencing is not possible, then routing against a well bypassed power plane will have to suffice.
- Do not route over plane splits.
- Layer transitions should be minimized. Ideally, there are a maximum of two vias per net: a transition at the SMARC connector to get to an inner layer, and a transition at the destination device, to get to the device pins.
- If a layer change is made and the layer change results in a reference plane change, then the two reference planes should be tied together in the same vicinity as the trace layer via. If the two reference planes are at different potentials, then they should be tied together through a “stitching capacitor”. The stitching cap isolates the DC potential between the planes but allows the high speed return currents associated with the trace. If the two reference planes are at the same potential, then they should be tied together with a “stitching via” – a seemingly useless via, except that it allows the high frequency trace return currents to flow between the reference planes. Following this advice results in lower EMI (as “loop area” is reduced) and better signal integrity.
- Controlled impedance design must be used:
  - All traces have a single ended (SE) impedance.
  - Differential pair traces have a SE impedance, and the pair has a differential (DE) impedance.
  - Recommended SE and DE impedances are given in the following sections of this Design Guide.
- Differential pairs have pair matching requirements (the two traces that make up a pair need to be matched to a certain tolerance). There are also group matching requirements: if more than one pair is needed for the function, then there are group matching requirements as well (for example LVDS[0]+/- needs to match LVDS[1]+/1 and LVDS[2]+/- and so on).
- The propagation speed of inner layer traces and outer layer traces is different.
- Differential pairs that are part of a common group (for example, the four LVDS data pairs in a 24 bit LVDS implementation) should be routed such that each pair in the group has the same per-layer routing length as the others.
- Routing on inner layers may reduce EMI. It is said that good EMI characteristics may be obtained by careful outer layer routing as well.
- Routing high speed traces across plane splits should be avoided. If it cannot be avoided, then stitching caps to bridge the split should be used.
- Cross-talk effects result from traces running in parallel, too close and for too long, either side by side on the same layer, or directly above / beneath each other on adjacent inner layers. For the same layer case, the mitigation is to increase the spacing to other traces. For the adjacent layer case, the traces on the adjacent layers should not run in parallel. Ideally, they are routed orthogonal to each other. If orthogonal routing is not possible, they should be at least 30 degrees off from each other.
- IC power pins need to be properly bypassed, as close as possible to the power pin.

11.4 Via Stub Influence To High Speed Signals

The higher the signal frequency is raising the higher the influence of via stubs is present. A simulation based upon the reference stack up from **Table 29 PCB Construction Example - 8 Layers** provides the following results.

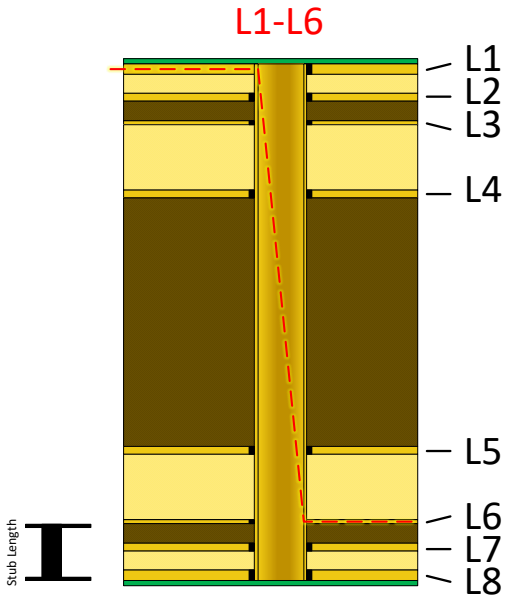
The ideal situation is to use vias to transit from the Top Layer to the Bottom Layer as shown in **Figure 88 Signal Transition** and with that to avoid stubs.

Figure 88 Signal Transition - L1-L8



In case the signal cannot be routed on the outer layers it is preferred to go as much trough the material as possible to minimize stubs, as shown in **Figure 89 Signal Transition - L1-L6**.

Figure 89 Signal Transition - L1-L6



Worst case for high speed signals are short transitions as in **Figure 90 Signal Transition - L1-L3**.

Figure 90 Signal Transition - L1-L3

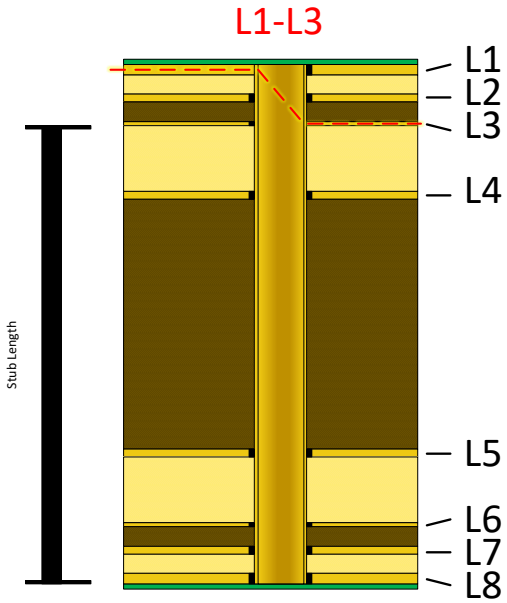
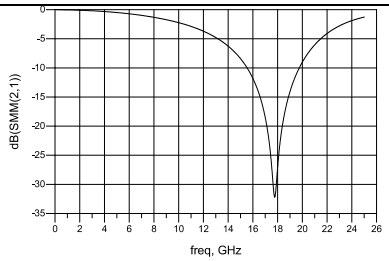
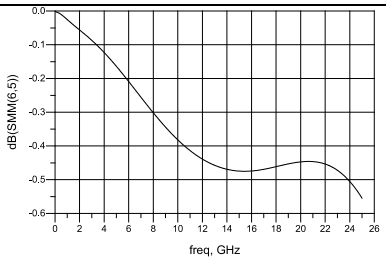
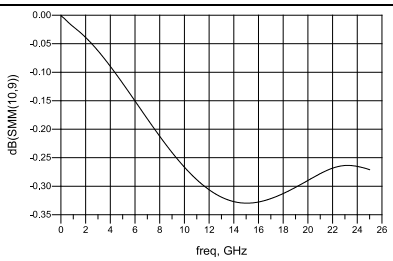


Table 22 Via Loss Simulation Results - 8 Layer PCB

	Loss on via [dB]		
	L1-L3	**L1-L6**	**L1-L8**
Freq. [GHz]			
0.13	0.003	0.003	0.003
0.25	0.005	0.005	0.005
0.31	0.006	0.006	0.006
0.75	0.023	0.018	0.016
0.80	0.025	0.019	0.017
1.25	0.05	0.033	0.025
1.50	0.066	0.041	0.029
2.50	0.147	0.071	0.050
2.70	0.166	0.078	0.055
3.00	0.198	0.087	0.062
4.00	0.327	0.123	0.090
5.00	0.496	0.164	0.119
8.00	1.318	0.302	0.212
12.90	4.663	0.456	0.318

Note: The higher the signal frequency the shorter the trace lengths and the via stubs need to be.

11.5 Trace Parameters for High-Speed Differential Interfaces

The routing suggestions for high speed interfaces varies over time when silicon structures get smaller but also different driver implementations are integrated to the chips. Therefore also the design for one and the same interface is changing over time. This means that the values in below tables are collected in best interest but might not apply for the platform that you intend to use today. But as a rule of thumb indication they are certainly usable.

Routing rules for high speed differential traces are summarized in the table below. Some notes on the table:

The “Max Symbol Rate” in the chart below is not the data transfer rate. It is the maximum transition rate on a single differential pair of the link, including the link encoding overhead.

- For example: 24 bit LCD LVDS is packed into four lanes. Including the control bits, there are actually 28 bits packed into the four LVDS lanes. There is no encoding overhead in LCD LVDS – it is just raw data – because there is a separate LVDS clock. So the “symbol rate” on an LVDS differential data pair, for a 40 MHz LVD clock, is (28 bits x 40 MHz / 4 lanes) = 280 Mbps.

- The “Sym Width” is the width of the pair Symbol, in ps. It is the inverse of the Max Symbol Rate.
  - Recall that the propagation speed of a micro-strip (outer layer) trace signal is about 150 ps / inch, and for a stripline (inner layer) trace signal, about 180 ps / inch.
  - The differential pair length mis-match, when expressed in units of time, needs to be small compared to the Symbol Width.
- Lengths are shown in mils (thousandths of an inch, or 0.0254 mm). The American convention for the decimal point and comma meaning is used. The 5,000 mil max length is 5.0 inches or 127 mm.
- “Pair Match” refers to the length matching of the two parts of the differential pair.
- Group Match refers to the length matching of the different pairs in a group.
- N/A means “Not Applicable”.
- “TX/RX Match” means the length matching between the TX and RX pairs.

Table 23 High-Speed Differential Trace Parameters (Example)

Interface	Max Symbol Rate (approximate)	Sym Width (ps)	Zo Diff (ohms)	Zo SE (ohms)	Max Length [1] (mils)	Pair Match (mils)	Group Match (mils)	TX / RX Match (mils)
PCIe Device Down	16 Gbps (Gen 4) [2]	62.5	85	50	5,900	< 2.5	N/A	< 1000
	8 Gbps (Gen 3)	125	(+-15%)	(+-10%)	4,400			
	5 Gbps (Gen 2)	200			6,400			
	2.5 Gbps (Gen 1)	500			9,400			
PCIe Addin Card	16 Gbps (Gen 4) [2]	62.5	85	50	4,000	< 2.5	N/A	< 1000
	8 Gbps (Gen 3)	125	(+-15%)	(+-10%)	3,600			
	5 Gbps (Gen 2)	200			4,500			
	2.5 Gbps (Gen 1)	500			8,500			
SATA	6 Gbps (Gen 3)	167	85	50	3,200	< 2.5	N/A	< 1000
	3 Gbps (Gen 2)	333	(+-20%)	(+-15%)	3,700			
	1.5 Gbps (Gen 1)	667			3,800			
HDMI	6 Gbps (HDMI 2.0) [3]	167	90	45	9,000	< 5	< 415	N/A
	3.4 Gbps (HDMI 1.3-1.4) [4]	294			5,100			
	1.6 Gbps (HDMI 1.0-1.2) [5]	625			2,700 [5]			
DP++ / DP / eDP	8.1 Gbps (DP 1.3-1.4) [2]	123	85	50	1,400	< 2.5	< 500	N/A
	5.4 Gbps (DP 1.2)	185	(+-10%)	(+-10%)	2,000			
LVDS	770 Mbps (24b 110 MHz)	1299	100	50	6,700	< 10	< 10	N/A
	280 Mbps (24b 40 MHz)	3571	(+-20%)		6,700			
MIPI-DSI	2.5 Gbps (DSI 1.2) D-Phy	400	90	45	3,500	< 2.5	< 20	N/A
MIPI-CSI	2.5 Gbps (CSI-2) D-Phy	400	90	45	3,700	< 2.5	< 20	N/A
USB 3.2 gen2	10 Gbps (SuperSpeed lines) [2]	100	85 (+-10%)	50 (+-15%)	500 [6]	< 2.5	N/A	N/A
USB 3.2 gen1	5 Gbps (SuperSpeed lines)	200	85 (+-10%)	50 (+-15%)	4,000	< 2.5	N/A	N/A
USB 2.0	480 Mbps (HS)	2083	90	45	8,000	< 50	N/A	N/A
	12 Mbps (FS)	23333			8,000			
2.5 GBE	625 Mbps	N/A	100	50	3,000	< 2.5	< 15	N/A
1 GBE	250 Mbps	N/A	100	50	7,200	< 2.5	< 15	N/A

Reference Plane: GND is preferred

Clearance to other traces: 20 mil or more

Max Vias: 2 (or less preferred)

1. Trace lengths are calculated based on the provided loss budget of the used IC in combination with a PCB material and stack up.
2. Maximum via stub length shall be less than 10mil at each via.

3. Retiming level shifter should be used (TI SN75DP159 or Parade PS8409A).
   Maximum total length between SMARC connector and retiming level shifter.
   Maximum total length between retiming level shifter and HDMI connector is 1 inch.
4. Active level shifter should be used (Parade PS8203).
   Maximum total length between SMARC connector and active level shifter.
   Maximum total length between active level shifter and HDMI connector is 3 inch.
5. Cost reduced level shifter used.
6. A re-driver or re-timer needs to be placed within 500mils distance from the SMARC connector.

Table 24 High-Speed Differential Trace Parameters (Loss Budget)

Interface	Max Symbol Rate (approximate)	Carrier board loss budget IC dependent (dB)	MXM con. loss FOXCON_AS0B82X-S43B-7H (Stack Height= 1.5mm) (dB)	Carrier board Vias Count	Carrier board vias loss Design and PCB material dependent (dB)	PCB trace loss/inch Design and PCB material dependent (dB/inch)		Approximately Max. carrier board trace (mils)
PCIe Device Down	16 Gbps (Gen 4)	11.75	0.37	2 *	0.302	1.76	≈	5,900
	8 Gbps (Gen 3)	4.68	0.36	2 *	0.123	0.88	≈	4,400
	5 Gbps (Gen 2)	4.19	0.23	2 **	0.147	0.55	≈	6,400
	2.5 Gbps (Gen 1)	2.85	0.09	2 **	0.05	0.28	≈	9,400
PCIe Addin Card	16 Gbps (Gen 4)	8.39	0.37	2 *	0.302	1.76	≈	4,000
	8 Gbps (Gen 3)	3.96	0.36	2 *	0.123	0.88	≈	3,600
	5 Gbps (Gen 2)	3.14	0.23	2 **	0.147	0.55	≈	4,500
	2.5 Gbps (Gen 1)	2.59	0.09	2 **	0.05	0.28	≈	8,500
SATA	6 Gbps (Gen 3)	2.97	0.28	2 **	0.198	0.66	≈	3,200
	3 Gbps (Gen 2)	1.54	0.11	2 **	0.066	0.33	≈	3,700
	1.5 Gbps (Gen 1)	0.76	0.05	2 **	0.023	0.17	≈	3,800
HDMI	6 Gbps (HDMI 2.0)	6.75	0.28	2 **	0.198	0.66	≈	9,000
	3.4 Gbps (HDMI 1.3-1.4)	2.03	0.11	2 **	0.066	0.33	≈	5,100
	1.6 Gbps (HDMI 1.0-1.2)	0.58	0.05	2 **	0.025	0.17	≈	2,700
DP++ / DP / eDP	8.1 Gbps (DP 1.3-1.4)	2.03	0.36	2 *	0.123	0.88	≈	1,400
	5.4 Gbps (DP 1.2)	1.93	0.25	2 *	0.041	0.59	≈	2,000
MIPI-DSI	2.5 Gbps (DSI 1.2) D-Phy	1.23	0.09	2 **	0.05	0.28	≈	3,500
MIPI-CSI	2.5 Gbps (CSI-2) D-Phy	1.28	0.09	2 **	0.05	0.28	≈	3,700
USB 3.2 gen2	10 Gbps (SuperSpeed lines)	1.55	0.39	2 *	0.164	1.10	≈	500
USB 3.2 gen1	5 Gbps (SuperSpeed lines)	2.84	0.23	2 **	0.147	0.55	≈	4,000

*) L1-L6 via used

**) L1-L3 via used

Calculation of Max. Carrier board trace:

(Carrier board loss budget – MXM con. loss – Via loss * Via count) / PCB trace loss/inch * 1000mil/inch – 200mil safety= Max. Carrier board trace

Example: (11.75dB - 0.37dB – 0.302dB * 2) / 1.76db/inch * 1000mil/inch – 200mil = 5923mil ≈ 5900mil

Note: The loss of the interface connector is not included to the calculation since the provided design values from the IC manufacturers include them already. Also there are different solutions on the market, through hole vs. SMD type for example, and make a difference that can decide whether your design will work properly or not. Especially for the highest speed interface designs such as USB 3.2, SATA gen3 and PCIe gen3 and 4, design simulations and compliance measurements are recommended to ensure the proper function.

Note: The MXM con. loss values depend on the chosen type and manufacturer. Please replace the loss values according to your chosen solution. In this example the simulated loss values from AS0B82X-S43B-7HMPN from FOXCON had been used.

Note: Re-drivers and Re-timers are recommended to be used for the highest speed interface designs such as USB 3.2, SATA gen3 and PCIe gen3 and 4.

Note: The via loss is based upon **Table 22 Via Loss Simulation Results - 8 Layer PCB** and will vary based on the stub length, PCB and via design.

Note: In the calculation formula a safety reduction of 200mil is recommended. In case simulations and compliance measurements are used to verify the compliance this buffer can be removed.

11.6 Trace Parameters for Single Ended Interfaces

Table 25 Single Ended Trace Parameters

Interface	Zo SE (ohms)	Max Length (mils)
General	50	12,000
SD Card	50	4,000
SPI	50	3,500
eSPI	50	3,500

11.6.1 SPI Topology considerations

The SPI topology is not specified but simulation results show that the SPI bus routing should follow the considerations in **Figure 91 SPI bus suggested topology** to allow multiple devices connected to it.

It depends on the CPU platform how many SPI bus devices can be supported (how many SPI_CSx# signals are provided). The more devices are connected to one bus the more important it is to keep the suggested “Star” or “Balanced Tree” topology.

The visible Resistors R in **Figure 91 SPI bus suggested topology** should be 15 ohms and should be placed near the Center Point (red marked CP in **Figure 91 SPI bus suggested topology**). The Center Point is the SMARC connector, where all branches are connected to.

Figure 91 SPI bus suggested topology

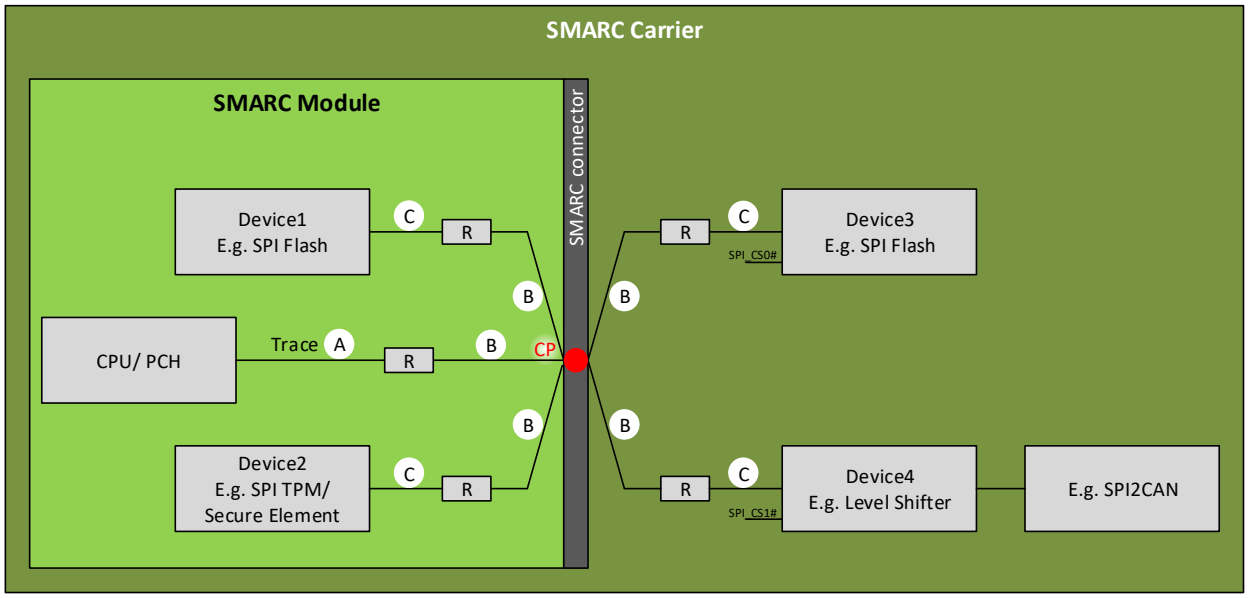


Figure 91 SPI bus suggested topology shows a worst case scenario. In real design applications some of the branches may be absent. In this case the branch trace length should be 0 mils. The impedance for all traces should be designed to match 50 ohms single ended and a cumulated length matching between the clock and data lanes within one bus should not exceed 125mils on the Carrier.

This topology should be kept for all SPIx_CK, SPIx_DIN, SPI_DO and also QSPI_CK and QSPI_IO[0:3] signals. The length matching between the signal traces need only be considered for the relevant interface. In example the SPI0 signals should be matched to each other. SPI1 signal length doesn´t need to be matched to SPI0 signals. It is best practice to use a via that is close to the SMARC connector pin in the design.

Table 26 SPI Topology - CLK And Data Signals

Trace	Allowable Branch Segment Length Min / Max (mils)	Length Matching Within a Branch	Notes
A	500 / 2,500	Length match data and clock in this trunk branch to within + / - 125 mils	Includes SOC breakout
B	0 / 500	Length match data and clock in this branch to within + / - 125 mils	
C	1,500 / 3,000	Length match data and clock in this branch to within + / - 125 mils	Module Branch
B+C	2,000 / 3,500		Carrier Branch

Note: The example above provides the maximum amount of devices possible that can be attached to a SPI bus. The more devices are connected to the bus the higher the capacitive loading will be. Thus might lead into a reduced interface speed possible.

11.6.2 eSPI Topology considerations

The eSPI bus is electrically identical to the SPI bus. Therefore the same rules apply. Please refer to the chapter **11.6.1 SPI Topology considerations** for routing guidelines.

11.7 PCB Construction Suggestions

PCB construction suggestions with trace width and gap parameters are given in the following three tables for four, six and eight layer PCBs. These are meant as a starting point. It is wise to plan ahead with your PCB fabricator and get their input.

Four layer construction is difficult since the high speed signals should be referenced against a GND plane, and the four layer construction offers only a single trace layer that is GND referenced.

Table 27 PCB Construction Example - 4 Layers

Layer	Use		Layer Thickness (mils)	Copper (ounces)	Plane Ref	SE 50 Ohm W (mils)	Diff 90 Ohm W / G (mils)	Diff 92.5 Ohm W / G (mils)	Diff 100 Ohm W / G (mils)
		SM	0.8						
L1	Sig	Cu	1.6	0.5 + plating	L2	4.5	4.6 / 6.4	4.5 / 6.5	4.4 / 10
		Prepreg	2.9						
L2	PWR	Cu	1.2	1.0					
		Core	50.0						
L3	GND	Cu	1.2	1.0					
		Prepreg	2.9						
L4	Sig	Cu	1.6	0.5 + plating	L3	4.5	4.6 / 6.4	4.5 / 6.5	4.4 / 10
		SM	0.8						

Finished Thickness: 63.0 mil / 1.6 mm
Impedance tolerance: +/- 10%

Table 28 PCB Construction Example - 6 Layers

Layer	Use		Layer Thickness (mils)	Copper (ounces)	Plane Ref	SE 50 Ohm W (mils)	Diff 90 Ohm W / G (mils)	Diff 92.5 Ohm W / G (mils)	Diff 100 Ohm W / G (mils)
		SM	0.8						
L1	Sig	Cu	1.6	0.5 + plating	L2	4.5	4.6 / 6.4	4.5 / 6.5	4.4 / 10
		Prepreg	2.9						
L2	PWR	Cu	1.2	1.0					
		Core	3.0						
L3	Sig	Cu	0.6	0.5	L2/L5	4.0	4.0 / 6.5	4.0 / 6.5	3.5 / 8.0
		Prepreg	42.0						
L4	Sig	Cu	0.6	0.5	L5/L2	4.0	4.0 / 6.5	4.0 / 6.5	3.5 / 8.0
		Core	3.0						
L5	GND	Cu	1.2	1.0					
		Prepreg	2.9						
L6	Sig	Cu	1.6	0.5 + plating	L5	4.5	4.6 / 6.4	4.5 / 6.5	4.4 / 10
		SM	0.8						

Finished Thickness: 62.2 mil / 1.6 mm
Impedance tolerance: +/- 10%

The eight layer example below shows an 80 mil (2mm) PCB thickness. This is often desirable for Carrier boards, and can be arranged for the four, six or eight layer versions. The thicker PCB makes for a more rugged system: the ***stiffness*** of a sheet of material (PCB or other sheet material) is proportional to the ***cube*** of the material thickness.

The eight layer construction below offers the advantage of four signal layers (L1, L3, L6, L8) that are GND referenced. This is best for high speed signals. This construction also makes power distribution very easy.

The **Pri/Sec** notation in the **Plane Ref** column below means the following: the plane layer to which the signal is closest is the Primary reference plane. The further plane is the Secondary.

If a high speed signal or signal pair changes reference layers (for example, L6 is referenced to L7 and L3 is referenced to L2 - so if you transition from L6 to L3, you are changing reference planes) it is recommended to put in a stitching via or via pair. The stitching vias are single net vias (GND) that tie the two reference planes together (L2 to L6) for the high frequency return signals that are trying to follow the path of the signal traces. You will have better signal integrity and fewer EMI issues if you do this. It is not necessary if reference planes are not being changed (for example, a transition from L1 to L3 keeps both referenced to L2, hence there is no reference plane transition). But in this example the via stub is then long for the signal trace and will have a negative impact to the signal integrity for “highest” speed interfaces. It is recommended to minimize via stubs for PCIe gen4, USB 3.2 gen 1&2 and similar interfaces and to use stitching vias for the GND return path.

Table 29 PCB Construction Example - 8 Layers

Layer	Use		Layer Thickness (mils)	Copper (ounces)	Plane Ref Pri/Sec	SE 50 Ohm W (mils)	Diff 90 Ohm W / G (mils)	Diff 92.5 Ohm W / G (mils)	Diff 100 Ohm W / G (mils)
		SM	0.8						
L1	Sig	Cu	1.6	0.5 + plating	L2	4.5	4.6 / 6.4	4.5 / 6.5	4.4 / 10
		Prepreg	2.9						
L2	GND	Cu	1.2	1.0					
		Core	3.0						
L3	Sig	Cu	0.6	0.5	L2/L4	4.0	4.0 / 6.5	4.0 / 6.5	3.5 / 8.0
		Prepreg	10.0						
L4	PWR	Cu	1.2	1.0					
		Core	38.0						
L5	PWR	Cu	1.2	1.0					
		Prepreg	10.0						
L6	Sig	Cu	0.6	0.5	L7/L5	4.0	4.0 / 6.5	4.0 / 6.5	3.5 / 8.0
		Core	3.0						
L7	GND	Cu	1.2	1.0					
		Prepreg	2.9						
L8	Sig	Cu	1.6	0.5 + plating	L7	4.5	4.6 / 6.4	4.5 / 6.5	4.4 / 10
		SM	0.8						

Finished Thickness: 80.6 mil / 2.0 mm
Impedance tolerance: +/- 10%


SMARC
module