AUO Display+

CUSTOMER APPROVAL SHEET

COMPANY NAME

MODEL A027DTN01.F

CUSTOMER APPROVED Title :
Name :

☐ APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.0)

☐ APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver. 0.0)

☐ APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver. 0.0)

☐ CUSTOMER REMARK :

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Product Specification
2.7” COLOR TFT-LCD MODULE

Model Name ： A027DTN01.F

Planned Lifetime:

Phase-out Control:

EOL Schedule:

< > Preliminary Specification

< ● > Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Document Version	Module Version	Revise Date	Page	Content
0.0	0.0	2020/02/25	--	First Draft

Contents

A. General Information

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	2.658 (Diagonal)	
2	Display Resolution	dot	960 (H) × 240 (V)	
3	Overall Dimension	mm	63.5 (H) x 46.6 (V) x 2.4 (T)	
4	Active Area	mm	54 x 40.5	
5	Pixel Pitch	μm	56.25 x 168.75	
6	Color Configuration	--	R, G, B delta	
7	Color Depth	--	16.7M Colors	
8	Display Mode	--	Normally White	
9	Weight	g	15	
10	Viewing direction	--	6 o'clock (gray inversion)	
11	Panel surface treatment	--	Hardcoat	

B. Electrical Specifications

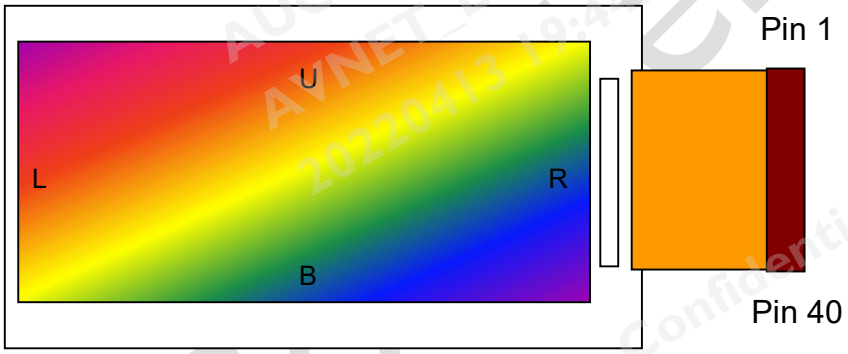
1. Pin Assignment

Pin no	Symbol	I/O	I/O Structure	Description	Remark
1	VCOM	I	-	Panel common voltage	
2	CS	I	Type 2	Serial command enable	
3	SDA	I/O	Type 3	Serial command data input	
4	SCL	I	Type 1	Serial command clock input	
5	HSYNC	I	Type 1	Horizontal sync input	
6	VSYNC	I	Type 1	Vertical sync input	
7	DCLK	I	Type 1	Data clock input	
8	D7	I	Type 1	Data input; MSB	
9	D6	I	Type 1	Data input	
10	D5	I	Type 1	Data input	
11	D4	I	Type 1	Data input	
12	D3	I	Type 1	Data input	
13	D2	I	Type 1	Data input	
14	D1	I	Type 1	Data input	
15	D0	I	Type 1	Data input; LSB	
16	GND	P	-	Ground for digital circuit	
17	ID_1	P	-	Ground for digital circuit	
18	ID_2	P	-	Ground for digital circuit	
19	VDD	P	-	System power	3.0V~3.6V
20	DVDD	C	-	Power setting capacitor connect pin	
21	V1	C	-	Power setting capacitor connect pin	
22	V2	C	-	Power setting capacitor connect pin	
23	V3	C	-	Power setting capacitor connect pin	
24	V4	C	-	Power setting capacitor connect pin	
25	VDD2	C	-	Power setting capacitor connect pin	
26	V5	C	-	Power setting capacitor connect pin	
27	V6	C	-	Power setting capacitor connect pin	
28	VDD3	C	-	Power setting capacitor connect pin	
29	VDD5	C	-	Power setting capacitor connect pin	
30	V7	C		Power setting capacitor connect pin	

31	V8	C		Power setting capacitor connect pin	
32	VGH	C		Power setting capacitor connect pin	
33	VGL	C		Power setting capacitor connect pin	
34	AGND	P	-	Ground for analog circuit	
35	FRP	O	Type 4	Frame polarity output for VCOM	
36	VCDC	O	Type 5	VCOM DC voltage output pin	
37	VCAC	C	-	Power setting capacitor for VCOM AC	
38	VCOM	I	-	Panel common voltage	
39	VLED-A	P	-	LED power anode	
40	VLED-C	P	-	LED power cathode	

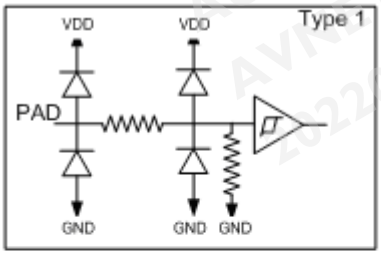
I：Input, O：Output, C：Capacitor, P：Power, D：Dummy

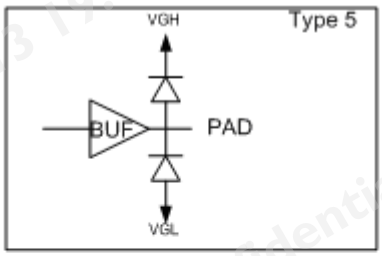
Note: Definition of scanning direction, Refer to figure as below：

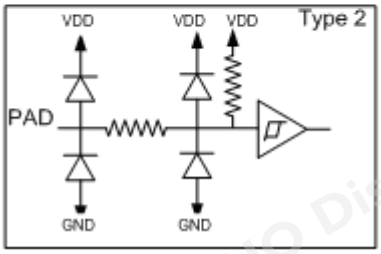


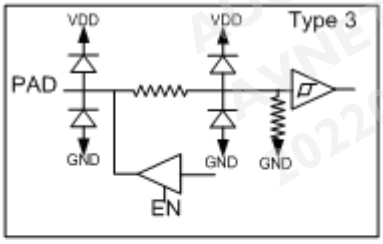
I/O Pin Structure:

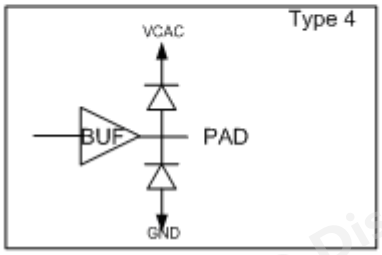
Pull high/low resistor is **700kΩ.**











2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Supply Voltage	VDD	AGND=GND=0V	-0.3	4.5	V	
TFT-LCD Power Voltage	VGH	AGND=GND=0V	-0.3	16	V	
	VGL	AGND=GND=0V	-16	0.3	V	
Input Signal Voltage	CS,SDA,SCL,Vsync, Hsync,DCLK,D0~D7	AGND=GND=0V	-0.3	4.5	V	
VCOM AC Output Voltage	FRP	AGND=GND=0V	-0.3	8	V	
VCOM AC Power Voltage	VCAC	AGND=GND=0V	-0.3	8	V	
VCOM DC Output Voltage	VCDC	AGND=GND=0V	-0.3	8	V	
VCOM Input Voltage	VCOM	AGND=GND=0V	-0.3	8	V	
Charge Pump Voltage	VDD2	AGND=GND=0V	-0.3	8	V	
	VDD3	AGND=GND=0V	-0.3	16	V	
	VDD5	AGND=GND=0V	-0.3	20	V	
	V1	AGND=GND=0V	-0.3	8	V	
	V2	AGND=GND=0V	-0.3	8	V	
	V3	AGND=GND=0V	-0.3	8	V	
	V4	AGND=GND=0V	-0.3	8	V	
	V5	AGND=GND=0V	-0.3	16	V	
	V6	AGND=GND=0V	-0.3	16	V	
	V7	AGND=GND=0V	-0.3	16	V	
	V8	AGND=GND=0V	-16	8	V	
Storage Temperature	Tstg	-	0	70	□	Ambient temperature
Operating Temperature	Topa	-	0	60	□	Ambient temperature

2. Electrical Characteristics

2.1 Recommended operating conditions (GND=AGND=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	Note 1
Input Signal voltage	H Level	V_{IH}	0.7* VDD	--	VDD	V	
	L Level	V_{IL}	GND	--	0.3* VDD	V	

Note 1: A build-in power on reset circuit for VDD is provided within the integrated LCD driver IC. The LCD module is in power save mode in default, and a standby releasing is required after VDD power on through serial control. Please refer to the register STB setting for detail.

2.2 Electrical characteristics (GND=AGND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for V_{DD}	I_{DD}	V_{DD}=3.3V	--	10	--	mA	Note 1
	$I_{DD(STANDBY)}$		--	0.1	--		Note 1
DC-DC voltage	V_{GH}	V_{DD}=3.3V	14	15	16	V	Note 2
	V_{GL}	V_{DD}=3.3V	-11	-10	-9	V	Note 2
VCOM voltage	V_{CAC}	--	4.2	4.8	5.4	Vp-p	AC component, Note 3
	V_{CDC}	--	0.86	1.06	1.26	V	DC component, Note 4

Note 1: Test Condition: 8colorbar+Grayscale pattern, UPS051 mode, DCLK=27MHz, Frame rate: 60Hz, other registers are default setting.

Note 2: VGH and VGL are output voltages of integrated LCD driver IC.

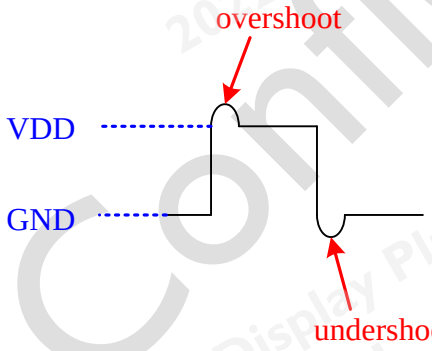
Note 3: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.

Note 4: VCDC could be adjusted, so as to minimize flicker and maximum contrast on each module.

2.3 Digital input signal overshoot and undershoot limitation

The digital input signal overshoot and undershoot voltage should keep under VDD+0.3V and over GND-0.3V.

Symbol	Overshoot	Undershoot
D0-D7	< VDD+0.3V	> GND-0.3V
DCLK		
HSYNC		
VSYNC		
SCL		
SDA		
CS		



2.4 Recommended Capacitance Values of External Capacitor

The recommended capacitance values of the external capacitor are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

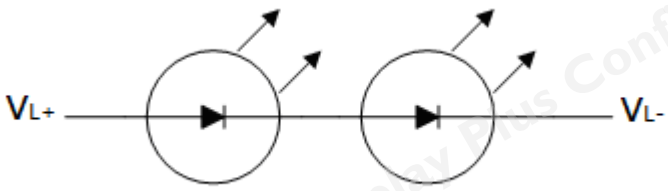
Pin name	Recommended value of capacitors (μF)	Withstanding voltage (V)
VGH	1.0 to 10	25
VGL	1.0 to 10	16
VDD5	1.0 to 10	16
VDD3	1.0 to 10	16
VDD2	2.2 to 10	6.3
DVDD	1.0 to 10	6.3
VCDC	2.2 to 10	10
VCAC	2.2 to 10	10
V1, V2	1.0 to 10	10
V3, V4	1.0 to 10	10
V5, V6	1.0 to 10	16
V7, V8	1.0 to 10	16
FRP	4.7	10

2.5 Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.[Note1]	Unit	Remark
Backlight Current	--	--	25	--	mA	**Note2**
Backlight voltage	V_{L+}-V_{L-}	--	6.4	7	V	

Note1: To consider LED driver tolerance.

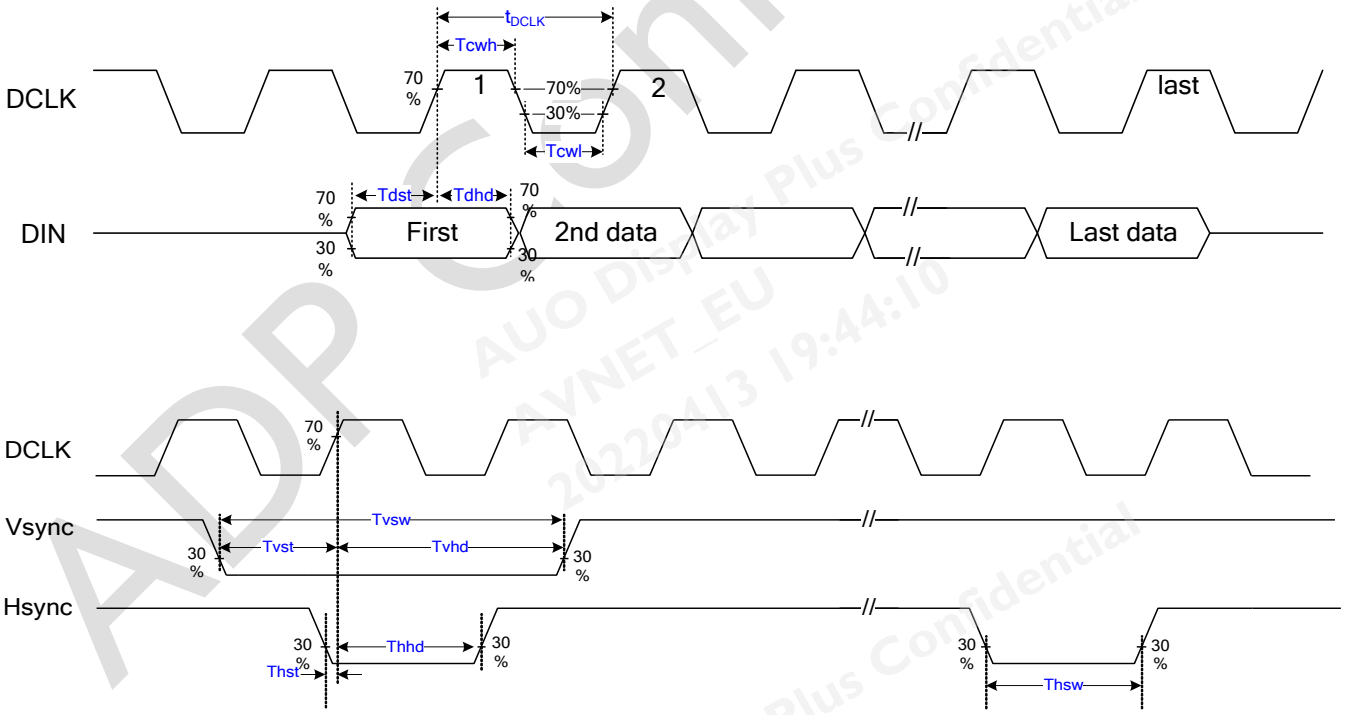
Note2: The maximum setting should be typical value. Ta=25□



4. Input timing AC characteristic

(VDD=3.0 ~3.6V, AGND=GND=0V, TA=25□)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK time	t_{DCLK}	33	-	188	ns	
DCLK width	Dcw	16.5	-	94	ns	D_{cw}=50%
DCLK duty cycle	Tcw	40	50	60	%	
VSYNC setup time	Tvst	6	-	-	ns	
VSYNC hold time	Tvhd	6	-	-	ns	
HSYNC setup time	Thst	6	-	-	ns	
HSYNC hold time	Thhd	6	-	-	ns	
Data setup time	Tdst	6	-	-	ns	
Data hold time	Tdhd	6	-	-	ns	
HSYNC width	Thsw	1	1	254	t_{DCLK}	
VSYNC width	Tvsw	1 t_{DCLK}	1 t_{DCLK}	6H	-	



t_H means: HSYNC period

5. Input timing format

5.1 UPS051 timing conditions (Refer to Fig.1 Fig.2 Fig.3)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	14.9	27	30	MHz	
HSYNC	Period	t_H	1024	1716	1728	t_{DCLK}	
	Display period	t_{hd}	960			t_{DCLK}	
	Back porch	t_{hbp}	50	70	255	t_{DCLK}	Note 1
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	1	1	t_{hbp-1}	t_{DCLK}	
VSYNC	Period	t_V	242	262	289	t_H	
	Display period	t_{vd}	240			t_H	
	Back porch	t_{vbp}	1	21	31	t_H	Note 2
	Front porch	t_{vfp}	$t_V - t_{vd} - t_{vbp}$			t_H	
	Pulse width	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	6 t_H		

Note 1: The t_{hbp} time is adjustable by setting register HBLK; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: The t_{vbp} time is adjustable by setting register VBLK. UPS051 accepts both interlace and non-interlace vertical input timing.

Fig.1 UPS051 Input Horizontal Timing Chart

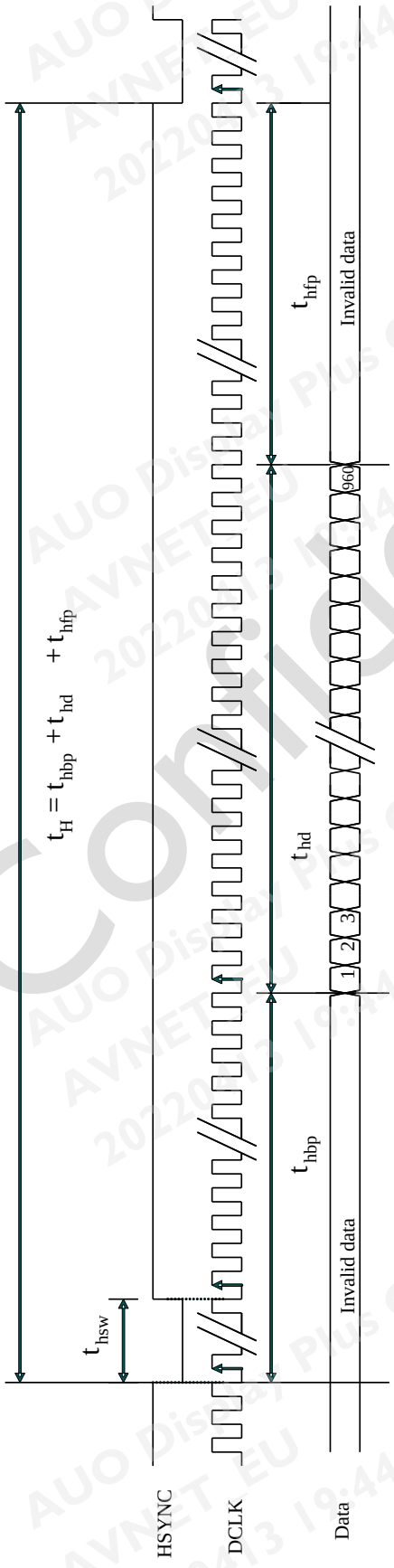


Fig.2 UPS051 Input Horizontal Data Sequence

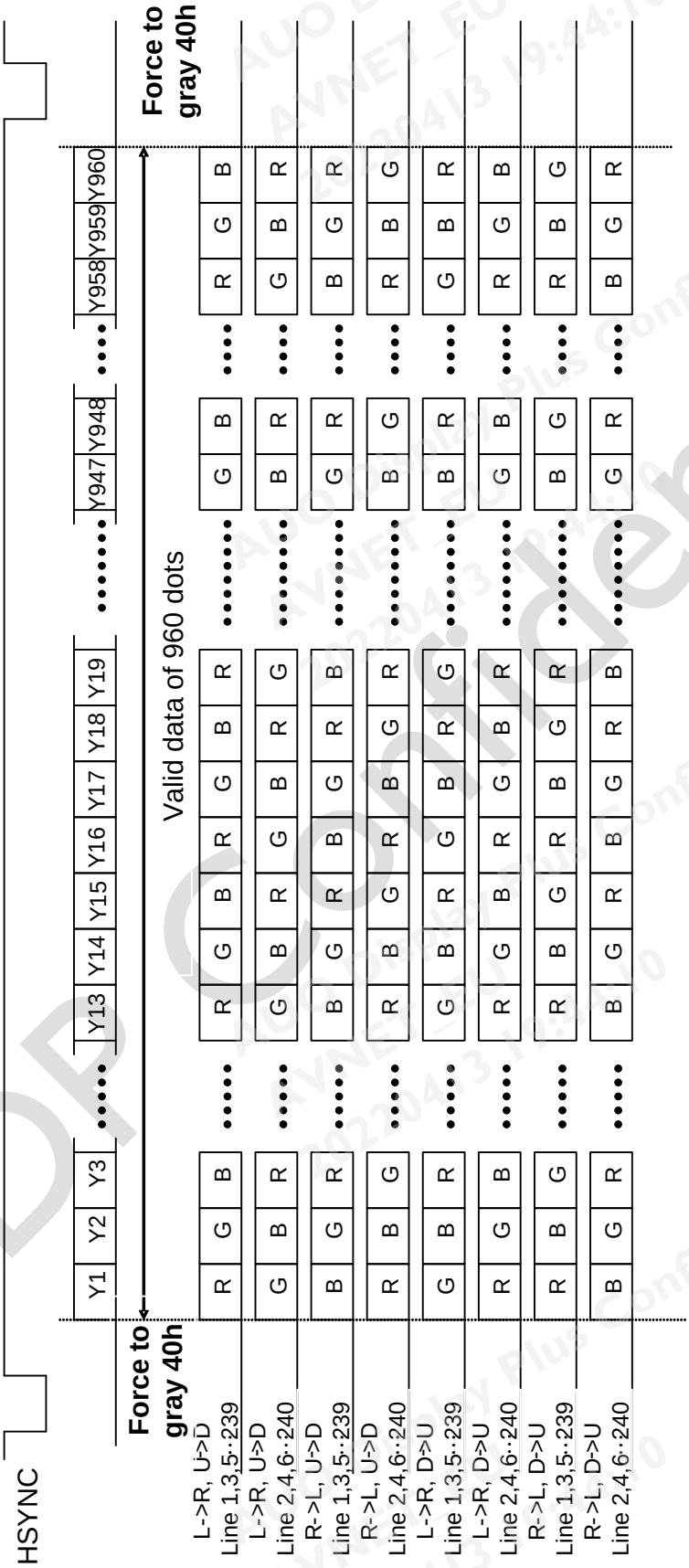
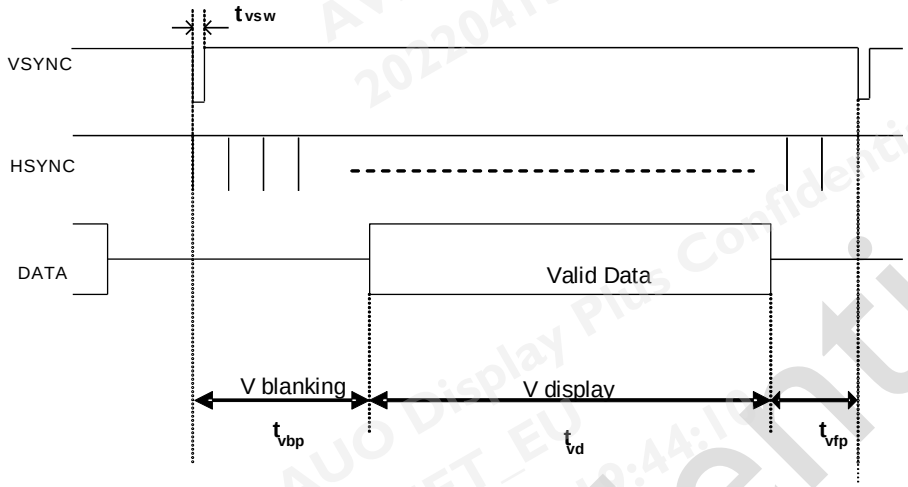


Fig.3 UPS051 Input Vertical Timing Chart



5.2 UPS052 timing

5.2.1 UPS052 (320 mode/NTSC/24.535MHz) timing specifications. (refer to Fig.4 Fig.5)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	19	24.535	30	MHz	
HSYNC	Period	t_H	1306	1560	1769	t_{DCLK}	
	Display period	t_{hd}	-	1280	-	t_{DCLK}	
	Back porch	t_{hbp}	2	241	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	t_V	242	262	282	t_H	
	Display period	t_{vd}	-	240	-	t_H	
	Back porch	t_{vbp}	1	21	31	t_H	
	Front porch	t_{vfp}	$t_V - t_{vd} - t_{vb}$			t_H	
	Pulse width	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	6 t_H		

5.2.2 UPS052 (320 mode/PAL/24.375MHz) timing specifications (refer to Fig.4 Fig.5)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	19.1	24.375	30	MHz	
HSYNC	Period	t_H	1306	1560	1804	t_{DCLK}	
	Display period	t_{hd}	-	1280	-	t_{DCLK}	
	Back porch	t_{hbp}	3	241	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	t_V	292	312	332	t_H	
	Display period	t_{vd}	-	288	-	t_H	
	Back porch	t_{vbp}	3	24	34	t_H	
	Front porch	t_{vfp}	$t_V - t_{vd} - t_{vb}$			t_H	
	Pulse width	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	6 t_H		

5.2.3 UPS052 (360 mode/NTSC/27MHz) timing specifications (refer to Fig.4 Fig.5)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	21.33	27	30	MHz	
HSYNC	Period	t_H	1466	1716	1769	t_{DCLK}	
	Display period	t_{hd}	-	1440	-	t_{DCLK}	
	Back porch	t_{hbp}	2	241	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	t_V	242	262	282	t_H	
	Display period	t_{vd}	-	240	-	t_H	
	Back porch	t_{vbp}	1	21	31	t_H	
	Front porch	t_{vfp}	$t_V - t_{vd} - t_{vb}$			t_H	
	Pulse width	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	6 t_H		

5.2.4 UPS052 (360 mode/PAL/27MHz) timing specifications (refer to Fig.4 Fig.5)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	21.44	27	30	MHz	
HSYNC	Period	t_H	1466	1728	1804	t_{DCLK}	
	Display period	t_{hd}	-	1440	-	t_{DCLK}	
	Back porch	t_{hbp}	3	241	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	t_V	292	312	332	t_H	
	Display period	t_{vd}	-	288	-	t_H	
	Back porch	t_{vbp}	3	24	34	t_H	
	Front porch	t_{vfp}	$t_V - t_{vd} - t_{vb}$			t_H	
	Pulse width	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	6 t_H		

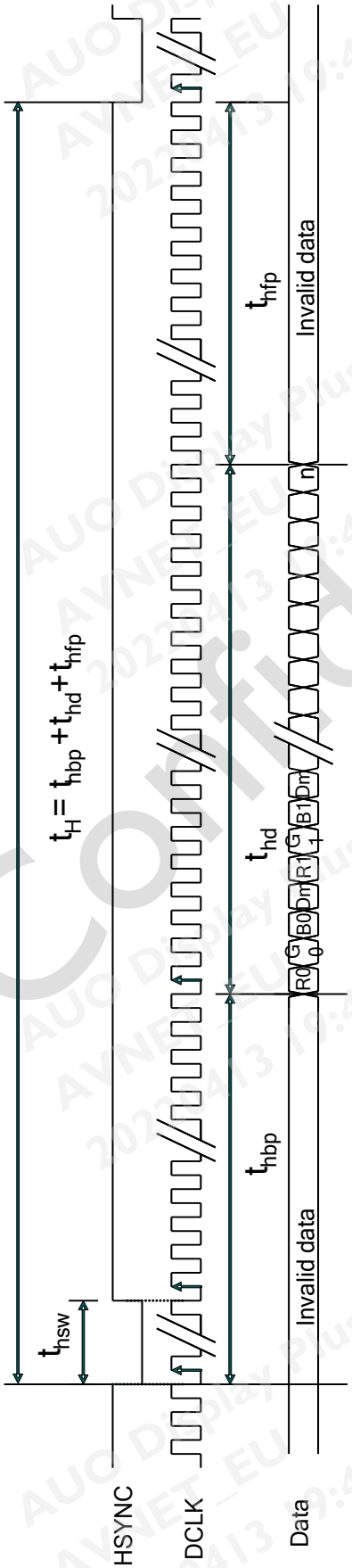
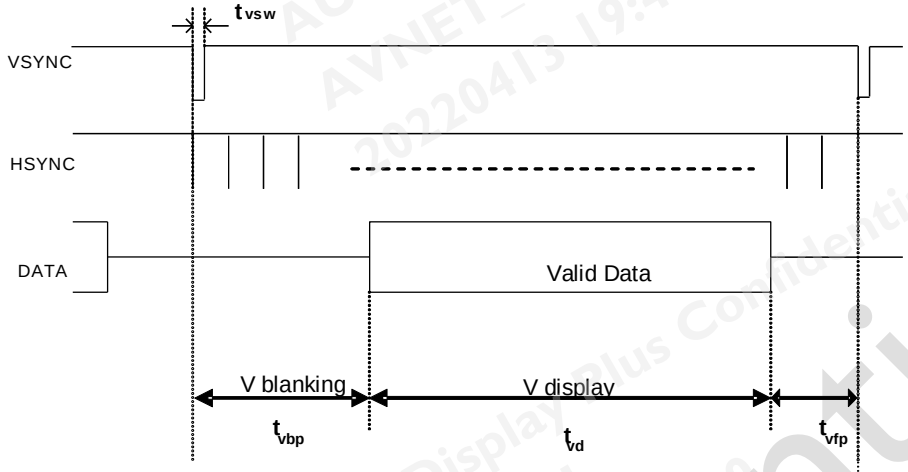


Fig.4 UPS052 Input Horizontal Timing Chart

Fig.5 UPS052 Input Vertical Timing Chart



5.3 CCIR656 Timing

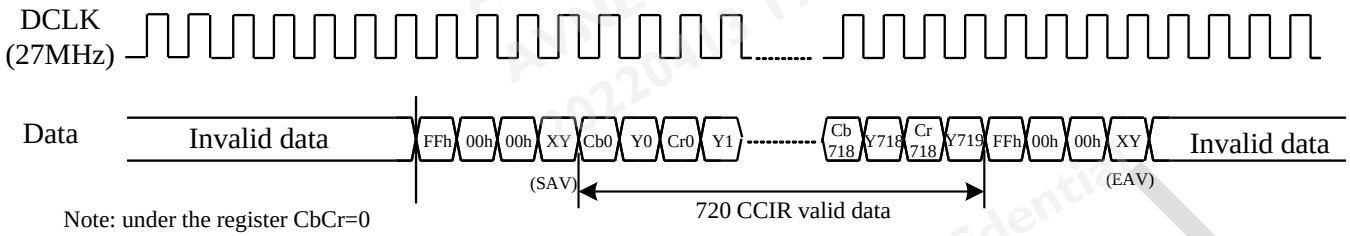


Fig.6 CCIR656 Data input format

5.3.1 CCIR656 decoding

- FF 00 00 < XY > signals are involved with HSYNC, VSYNC and Field
- <XY> encode following bits:

F=field select : F=0 for field 1, F=1 for field 2;

V=1 during vertical blanking

H=0 at SAV , H=1 at EAV ,

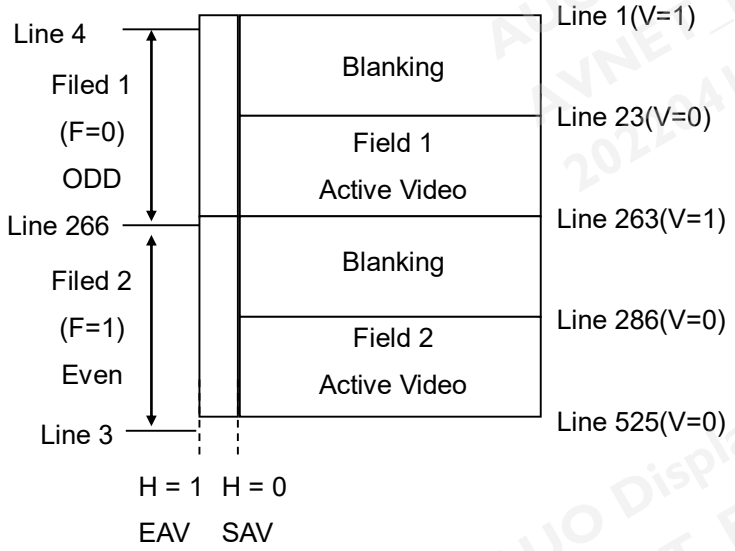
P3-P0=protection bits :

P3=V □ H P2=F □ H P1=F □ V P0=F □ V □ H □: represents the exclusive-OR function

- Control is provided through “End of Video” (EAV) and “Start of Video” (SAV) timing references.
- Horizontal blanking section consists of repeating pattern 80 10 80 10

XY							
D7(MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0(LSB)**
1	F	V	H	P3	P2	P1	P0

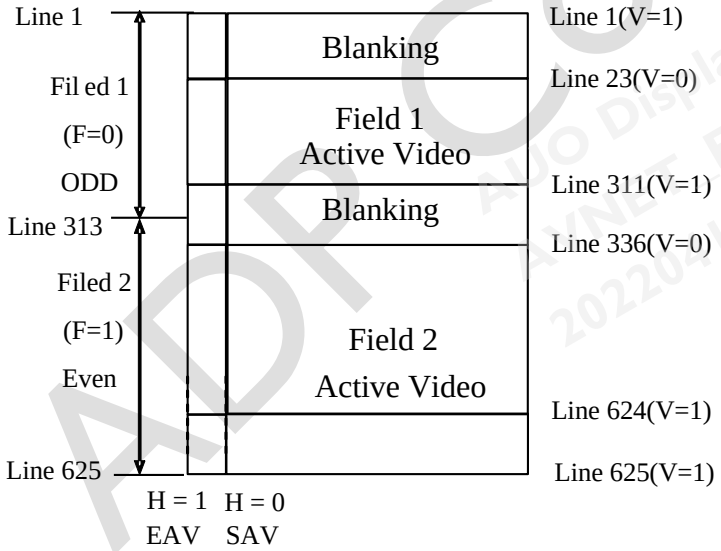
5.3.2 CCIR656 NTSC



Line Number	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	Even Field	EAV	Blanking
0	Odd Field	SAV	Active Video

5.3.3 CCIR656 PAL



Line Number	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
335-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	Even Field	EAV	Blanking
0	Odd Field	SAV	Active Video

5.4 YUV 720 and YUV 640 timing

5.4.1 YUV 720 mode/NTSC timing specifications (refer to Fig.7 Fig.9)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	21.5	27	30	MHz	
HSYNC	Period	t_H	1476	1716	1769	t_{DCLK}	
	Display period	t_{hd}	-	1440	-	t_{DCLK}	
	Back porch	t_{hbp}	2	240	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	t_V	242	262	282	t_H	
	Display period	t_{vd}	-	240	-	t_H	
	Back porch	t_{vbp}	1	21	31	t_H	
	Front porch	t_{vfp}	$t_V - t_{vd} - t_{vb}$			t_H	
	Pulse width	t_{vsw}	-	1	-	t_{DCLK}	

5.4.2 YUV 720 mode/PAL timing specifications (refer to Fig.7 Fig.9)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	21.6	27	30	MHz	
	Period	t_H	1476	1728	1804	t_{DCLK}	
	Display period	t_{hd}	-	1440	-	t_{DCLK}	
	Back porch	t_{hbp}	2	240	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	t_V	292	312	332	t_H	
	Display period	t_{vd}	-	288	-	t_H	
	Back porch	t_{vbp}	3	24	34	t_H	
	Front porch	t_{vfp}	$t_V - t_{vd} - t_{vb}$			t_H	
	Pulse width	t_{vsw}	-	1	-	t_{DCLK}	

5.4.3 YUV 640 mode/NTSC timing specifications (refer to Fig.8 Fig.9)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	19.12	24.535	30	MHz	
HSYNC	Period	t_H	1314	1560	1769	t_{DCLK}	
	Display period	t_{hd}	-	1280	-	t_{DCLK}	
	Back porch	t_{hbp}	2	240	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	t_V	242	262	282	t_H	
	Display period	t_{vd}	-	240	-	t_H	
	Back porch	t_{vbp}	1	21	31	t_H	
	Front porch	t_{vfp}	$t_V - t_{vd} - t_{vb}$			t_H	
	Pulse width	t_{vsw}	-	1	-	t_{DCLK}	

5.4.4 YUV 640 mode/PAL timing specifications (refer to Fig.8 Fig.9)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	19.22	24.375	30	MHz	
HSYNC	Period	t_H	1314	1560	1804	t_{DCLK}	
	Display period	t_{hd}	-	1280	-	t_{DCLK}	
	Back porch	t_{hbp}	2	240	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	t_V	292	312	332	t_H	
	Display period	t_{vd}	-	288	-	t_H	
	Back porch	t_{vbp}	3	24	34	t_H	
	Front porch	t_{vfp}	$t_V - t_{vd} - t_{vb}$			t_H	
	Pulse width	t_{vsw}	-	1	-	t_{DCLK}	

Fig.7 YUV720 Input Horizontal Timing Chart

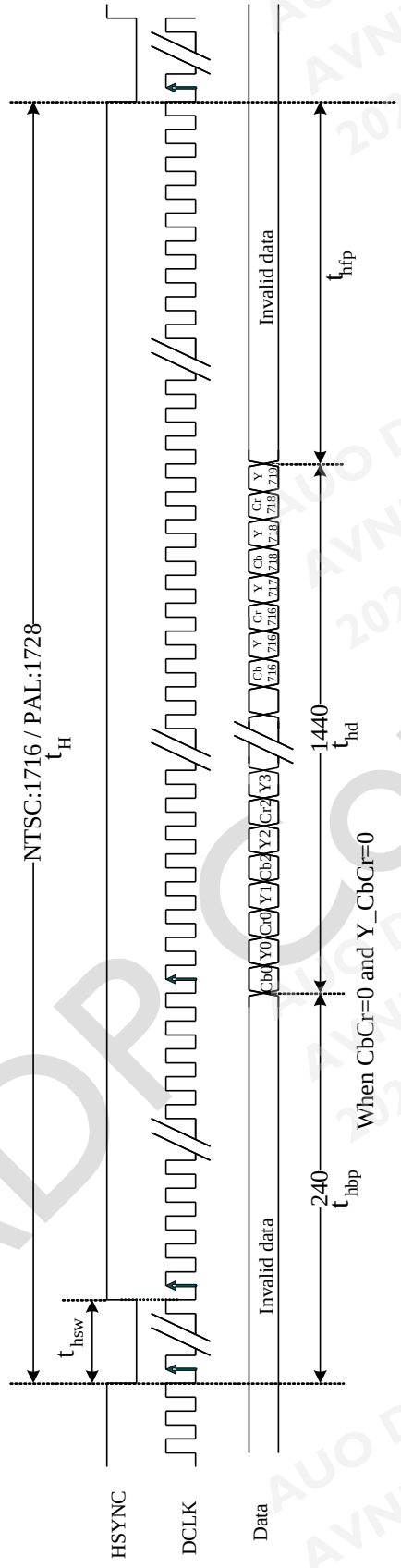


Fig.8 YUV640 Input Horizontal Timing Chart

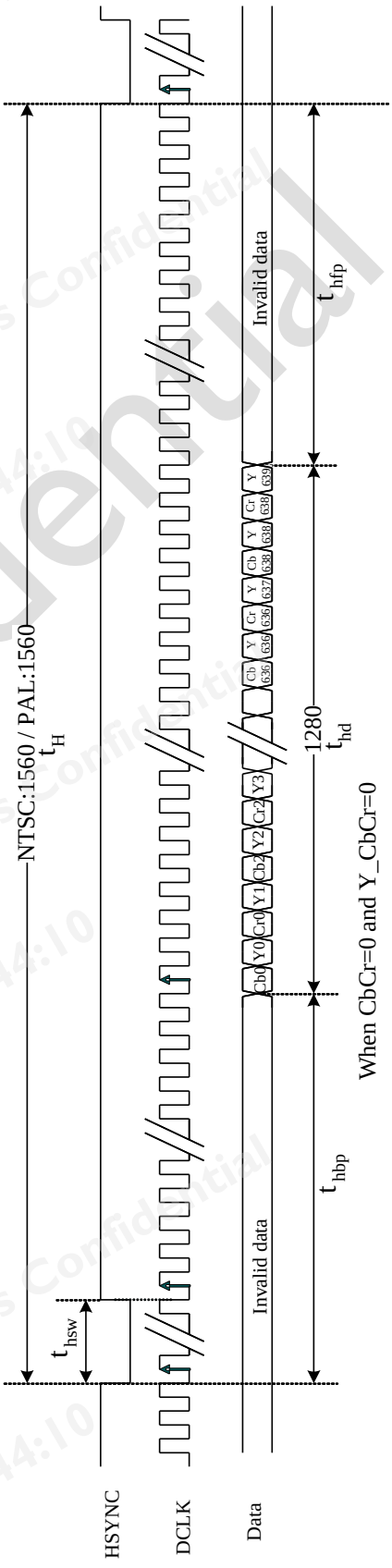
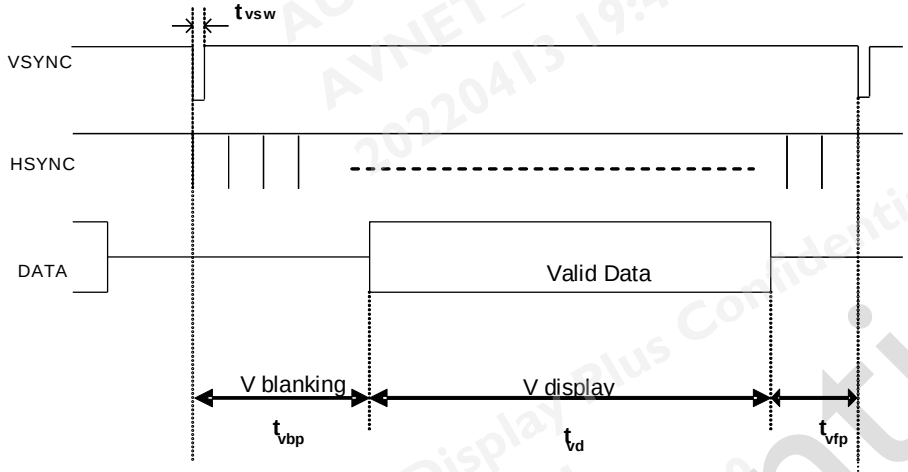


Fig.9 YUV Input Vertical Timing Chart



5.5 CCIR656/YUV 720/YUV 640 to RGB conversion

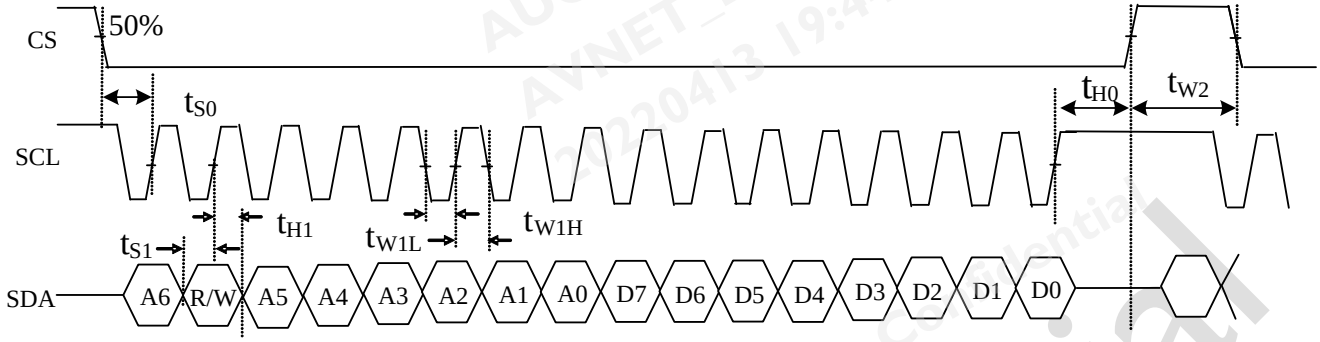
$R_n=1.164*[(Y_{2n-1}+Y_{2n})/2-16] + 1.596*(C_{rn}-128)$

$G_n=1.164*[(Y_{2n-1}+Y_{2n})/2-16] - 0.813*(C_{rn}-128) - 0.392*(C_{bn}-128)$

$B_n=1.164*[(Y_{2n-1}+Y_{2n})/2-16] + 2.017*(C_{bn}-128)$

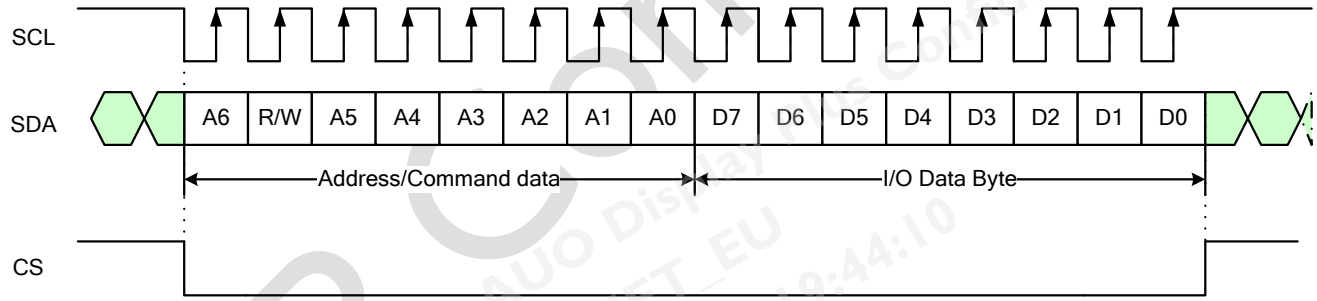
Where Y:16~235 C_r:16~240 C_b:16~240

6. Serial control interface AC characteristic



Item	Symbol	Min	Typical	Max	Unit
CS input setup Time	t_{S0}	50	-	-	ns
Serial data input setup Time	t_{S1}	50	-	--	ns
CS input hold Time	t_{H0}	50	-	-	ns
Serial data input hold Time	t_{H1}	50	-	-	ns
SCL pulse low width	t_{W1L}	50	-	-	ns
SCL pulse high width	t_{W1H}	50	-	-	ns
CS pulse high width	t_{W2}	400	-	-	ns

6.1 Timing chart



1. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.
2. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
3. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.
4. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
5. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data after the falling edge of CS pulse are valid data.
6. Serial block operates with the SCL clock.
7. Serial data can be accepted in the standby (power save) mode.

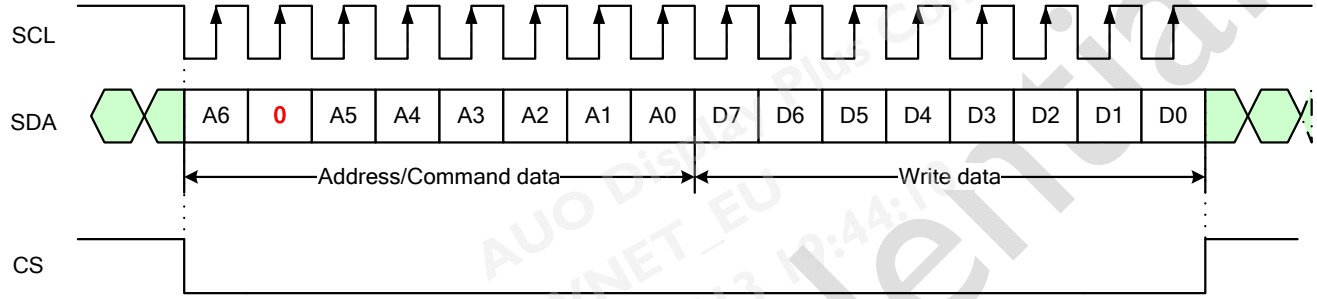
6.2 The configuration of serial data at SDA terminal is at below

MSB LSB

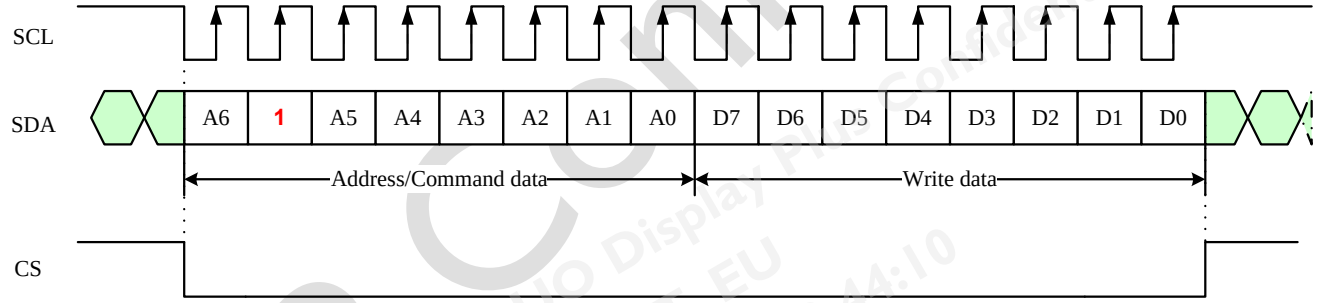
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Address	R/W	Address						DATA							

R/W: Establishes the Read mode when set to '1', and the Write mode when set to '0'.

Write Mode:



Read Mode:



6.3 Register table

No.	Register address								MSB	Register data (default setting)						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	Y_CbCr (0)	CCIR601 (0)	UPS051_S2D (0)	Scaling (1)	VCOM_AC (0011)			
R1	0	0	0	0	0	0	0	1	VCDCE (1)	VCOM_DC (5Bh)						
R3	0	0	0	0	0	0	1	1	Brightness (40h)							
R4	0	0	0	0	0	1	0	0	Narrow (0)	YUV (0)	SEL (00)		NTSC/PAL (10)		VDIR (1)	HDIR (1)
R5	0	0	0	0	0	1	0	1	x	GRB (1)	x	x	x	SHDB2 (1)	SHDB1 (1)	STB (0)
R6	0	0	0	0	0	1	1	0	HBLK_EN (0)	x	x	VBLK (15h)				
R7	0	0	0	0	0	1	1	1	HBLK(46h)							
R12	0	0	0	0	1	1	0	0	PAIR (00)		x	CbCr (0)	x	Vdpol (1)	Hdpol (1)	DCLKpol (0)
R13	0	0	0	0	1	1	0	1	CONTRAST_RGB (40h)							
R14	0	0	0	0	1	1	1	0	x	SUB-CONTRAST_R (40h)						
R15	0	0	0	0	1	1	1	1	x	SUB-BRIGHTNESS_R (40h)						
R16	0	0	0	1	0	0	0	0	x	SUB-CONTRAST_B (40h)						
R17	0	0	0	1	0	0	0	1	x	SUB-BRIGHTNESS_B (40h)						
R36~R79	Gamma adjustment registers															
R97	1	0	1	0	0	0	0	1	x	x	x	x	x	x	GAMMA setting (10)	

Note1 : “x” => please set to ‘0’.
Note2 : Inside () is IC design default value, not AUO recommend SPI.
Note3 : Please reference to Recommended Power On/Off serial command settings.
Note4 : If customer’s power on command is different from recommend Power On/Off serial command settings, please double check with AUO.

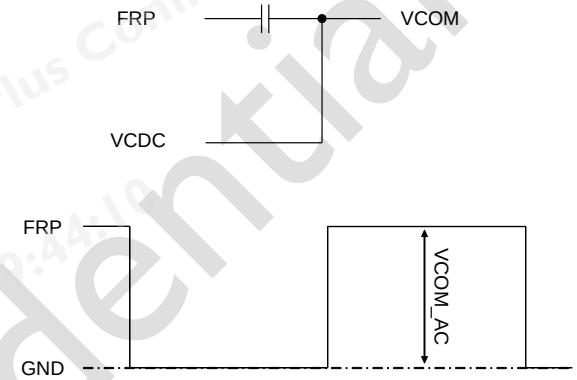
6.4 Register description

R0:

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	Y_CbCr(0)	CCIR601 (0)	UPS051_S2D(0)	Scaling(1)	VCOM_AC(0011)			

VCOM_AC: Common voltage AC level selection (deviation ±0.1V)

VCOM_AC				Voltage (V)
D2	D1	D0	D3	
0	0	0	0	4.2
0	0	0	1	4.3
0	0	1	0	4.4
0	0	1	1	4.5
0	1	0	0	4.6
0	1	0	1	4.7
0	1	1	0	4.8(Default)
0	1	1	1	4.9
1	0	0	0	5.0
1	0	0	1	5.1
1	0	1	0	5.2
1	0	1	1	5.3
1	1	X	X	5.4



Note: FRP and VCDC are IC hardware output pins, which can refer to "Application circuit"

CCIR601: CCIR601 input timing selection

CCIR601	Function
0(Default)	Disable CCIR601 (Default)
1	Enable CCIR601. (Please refer to the table of R4(SEL) for detail description)

Y_CbCr: Y & CbCr exchange position (only valid for 8-bit input YUV640 / YUV720)

	CbCr(R12[4])='0'	CbCr(R12[4])='1'
Y_CbCr='0', (Default)	Cb0 Y0 Cr0 Y1 Cb2 Y2 Cr2 Y3	Cr0 Y0 Cb0 Y1 Cr2 Y2 Cb2 Y3
Y_CbCr='1',	Y0 Cb0 Y1 Cr0 Y2 Cb2 Y3 Cr2	Y0 Cr0 Y1 Cb0 Y2 Cr2 Y3 Cb2

UPS051_S2D : UPS051 Stripe to Delta mode selection

UPS051_S2D	Function
0	Original UPS051 mode (Default)
1	Stripe data input (RGB/RGB), delta data output (RGB/GBR).

Scaling : Scaling selection

Scaling	Function

0	Scaling disable
1	Scaling enable. (Default)

Note : Disable Scaling function when UPS051_S2D = '0'

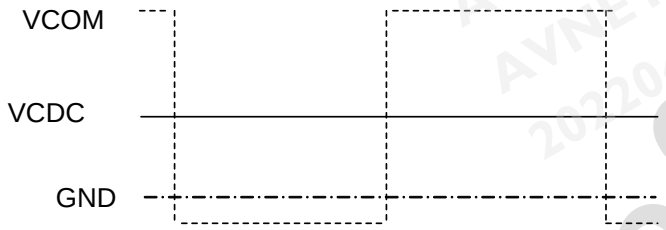
R1:

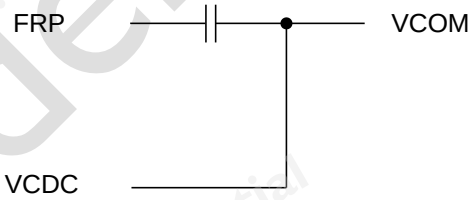
No	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R1	0	0	0	0	0	0	0	1	VCDCE (1)	VCOM_DC (5Bh)						

VCOM_DC: Common voltage DC level selection (10mV/step)

D6~D0	VCOM_DC level (V)
00h	0.54
:	:
5Bh(Default)	1.45(Default)
:	:
7Fh	1.81

Note: For model A027DTN01.9, the recommendatory VCDC is 1.06V





Note: FRP and VCDC are IC hardware output pins, which can refer to "Application circuit"

VCDCE: VCOM_DC function enable setting

VCDCE	Function
0	VCOM _DC function disable. The VCDC pin is Hi-Z.
1	VCOM_DC function enable. The VCDC voltage follows VCOM_DC setting. (Default)

R3:

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R3	0	0	0	0	0	0	1	1	Brightness (40h)							

BRIGHTNESS: RGB bright level setting, setting accuracy: 1 step / bit

D7 ~ D0	Brightness gain
00h	Dark (-64)
40h(Default)	Center (0) (Default)
FFh	Bright (+191)

R4:

No.	Register address								MSB		Register data					LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R4	0	0	0	0	0	1	0	0	Narrow(0)	YUV(0)	SEL(00)		NTSC/PAL(10)		VDIR(1)	HDIR(1)

HDIR: Horizontal scan direction setting

HDIR	Function
0	Right to left scan
1	Left to right scan (Default)

VDIR: Vertical scan direction setting

VDIR	Function
0	Down to up scan
1	Up to down scan (Default)

NTSC/PAL: NTSC or PAL input mode selection (except UPS051 timing doesn't apply this setting)

NTSC/PAL		Mode
D3	D2	
0	0	PAL
0	1	NTSC
1	X	Auto detection (Default)

SEL: Input data timing format selection

CCIR601	YUV	SEL		INPUT TIMING FORMAT
		D5	D4	
0	0	0	0	UPS051 (Default)
0	0	0	1	UPS052 320 × 240
0	0	1	X	UPS052 360 × 240
0	1	1	X	CCIR656
1	1	0	X	YUV 640(*)
1	1	1	0	YUV 720(*)

(*)Please refer to YUV640/YUV720 horizontal timing spec for detailed description.

YUV: YUV (CCIR656, YUV640, YUV720) or RGB input selection

YUV	Function
0	RGB input (Default)
1	CCIR656 / YUV640 / YUV720 input.

When this command is sent to driver ic,it will be executed immediately

Narrow: Normal display and Narrow display selection.

Narrow	Function
0	Normal display (Default)
1	Narrow Display

Narrow=0

Narrow=1

R5:

No	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R5	0	0	0	0	0	1	0	1	x	GRB(1)	x	x	x	SHDB2(1)	SHDB1(1)	STB(0)

STB: Standby (Power saving) mode setting

STB	Function
0	Standby mode (Default)
1	Normal operation

SHDB1: Shut down for back light power converter

SHDB1	Function
0	The back light power converter is off
1	The back light power converter is controlled by STB's power in/off sequence (Default)

Note: Use external LED driver must set SHDB1= "0"

SHDB2: Shut down for VGH/VGL charge pump

SHDB2	Function
0	VGH/VGL charge pump is always off
1	VGH/VGL charge pump is controlled by power on/off sequence (Default)

GRB: Register reset setting

GRB	Function
0	Reset all registers to default value
1	Normal operation (Default)

When this command is sent to driver ic,it will be executed immediately

R6:

No	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R6	0	0	0	0	0	1	1	0	HBLK_EN(0)	x	x	VBLK(15h)				

VBLK: Vertical blanking setting

UPS051, UPS052, YUV640 and YUV720 NTSC mode

D4 ~ D0	VBLK	Unit
01h	1	H (line)
15h	21(Default)	
1Fh	31	

CCIR656 NTSC mode

D4 ~ D0	VBLK	Unit
01h	1	H (line)
16h	22(Default)	
1Fh	31	

UPS052, CCIR656 and YUV640 and YUV720 PAL mode(Vertical blanking + 3)

D4 ~ D0	VBLK	Unit
00h	3	H (line)
15h	24(Default)	
1Fh	34	

Note: V-blanking must be adjusted based on the input data.

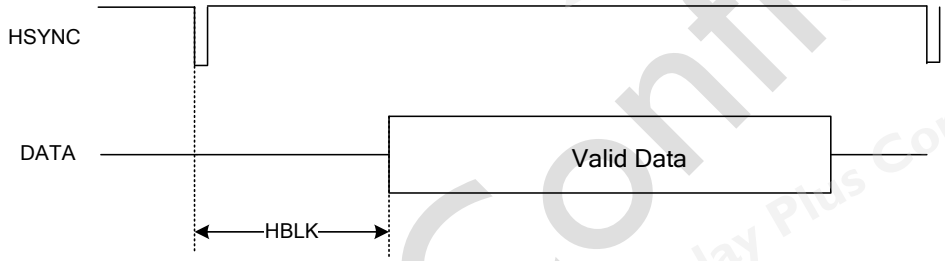
R6 & R7:

No	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R6	0	0	0	0	0	1	1	0	HBLK_EN(0)	LED_Current(00)		VBLK(15h)				
R7	0	0	0	0	0	1	1	1	HBLK(46h)							

HBLK_EN & HBLK: Horizontal blanking setting

HBLK_EN	HBLK(D7~D0)	HBLK	Unit	Remark
x	32h	50	DCLK(*)	UPS051
x	46h	70(Default)		
x	FFh	255		
0	-	241(fixed)	DCLK(*)	UPS052
1	02h~FF	2~255	DCLK(*)	
0	-	240(fixed)	DCLK(*)	YUV640, YUV720
1	02h ~ FFh	2 ~ 255	DCLK(*)	

*The frequency of DCLK is different under different input timing.



R12:

No.	Register address								MSB			Register data				LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R12	0	0	0	0	1	1	0	0	PAIR(00)		x	CbCr(0)	x	Vdpol(1)	Hdpol(1)	DCLKpol(0)

DCLKpol: DCLK polarity selection

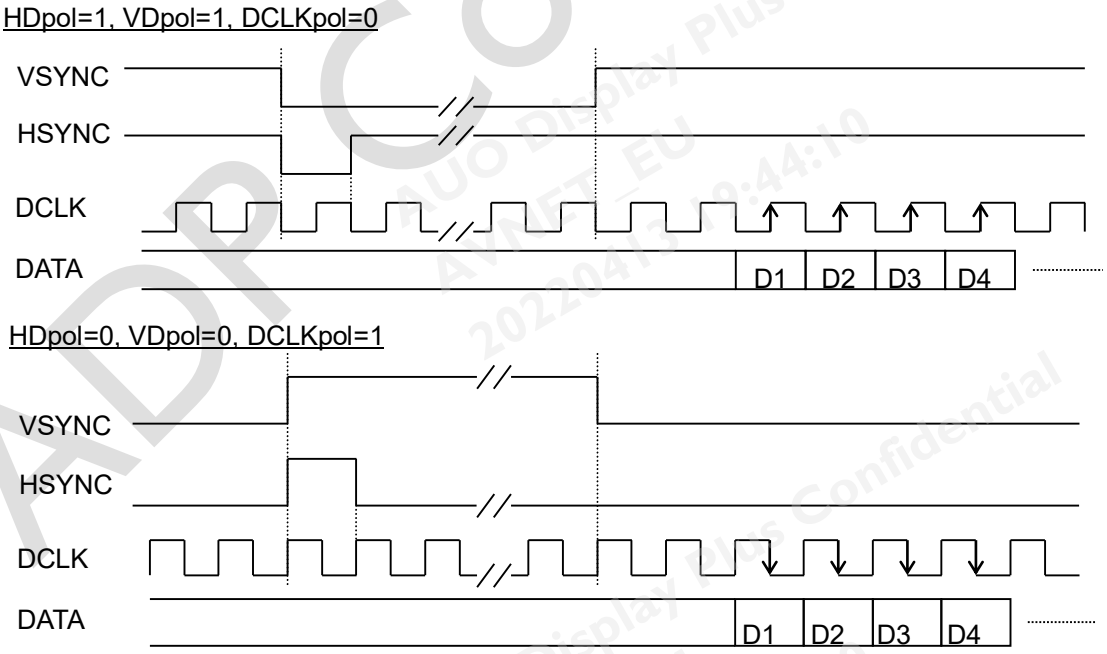
DCLKpol	Function
0	Positive polarity (Default)
1	Negative polarity

HDpol: HSYNC polarity selection

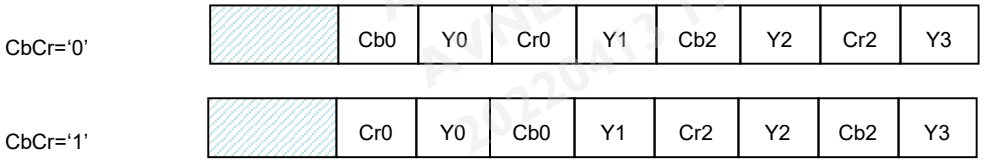
HDpol	Function
0	Positive polarity
1	Negative polarity (Default)

VDpol: VSYNC polarity selection

VDpol	Function
0	Positive polarity
1	Negative polarity (Default)



CbCr: Cb & Cr exchange position, (Please refer to the table of R0(Y_CbCr) for detail description)



PAIR: Vertical start time setting for Odd/Even frame

UPS051 / UPS052 NTSC / UPS052 PAL (*)

PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
x	0	21/21(Default)	H (line)
x	1	21/20	

CCIR656/YUV640/YUV720 NTSC/PAL (**)

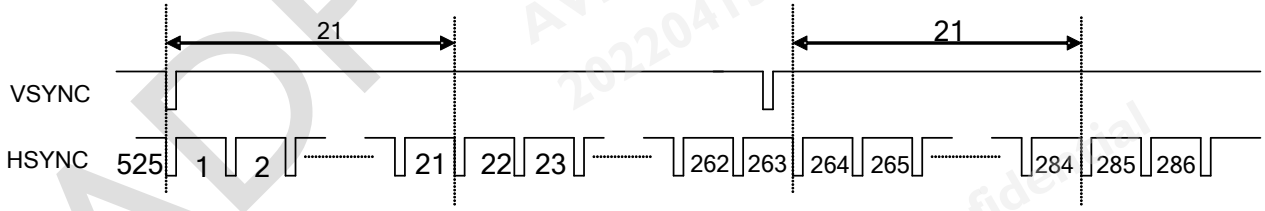
PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
0	0	22/22	H (line)
0	1	22/23	
1	0	23/22	
1	1	23/23	

(*)The typical value of VBLK of UPS052 PAL(24 H) is different than UPS051/UPS052 NTSC(21H).

(**) The typical value of VBLK of CCIR656 PAL(24 H) is different than CCIR656 NTSC(22H).

Note: V-blanking must be adjusted based on the input data.

For example:



	PAIR=0		PAIR=1	
Field \ Line	START	END	START	END
ODD	22	261	22	261
EVEN	285	524	284	523

This table is based on VBLK=21.

R13:

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R13	0	0	0	0	1	1	0	1	CONTRAST_RGB(40h)							

CONTRAST_RGB: RGB contrast level setting, the gain changes (1/64) / bit

D7 ~ D0	Contrast gain
00h	0
40h	1(Default)
FFh	3.984

R14~R17:

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R14	0	0	0	0	1	1	1	0	x	SUB-CONTRAST_R(40h)						
R16	0	0	0	1	0	0	0	0	X	SUB-CONTRAST_B(40h)						

SUB-CONTRAST: R/B sub-contrast level setting, the gain changes (1/256) / bit

D6 ~ D0	Brightness gain
00h	0.75
40h	1(Default)
7Fh	1.246

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R15	0	0	0	0	1	1	1	1	X	SUB-BRIGHTNESS_R(40h)						
R17	0	0	0	1	0	0	0	1	X	SUB-BRIGHTNESS_B(40h)						

SUB-BRIGHTNESS: R/B sub-bright level setting, setting accuracy : 1 step / bit

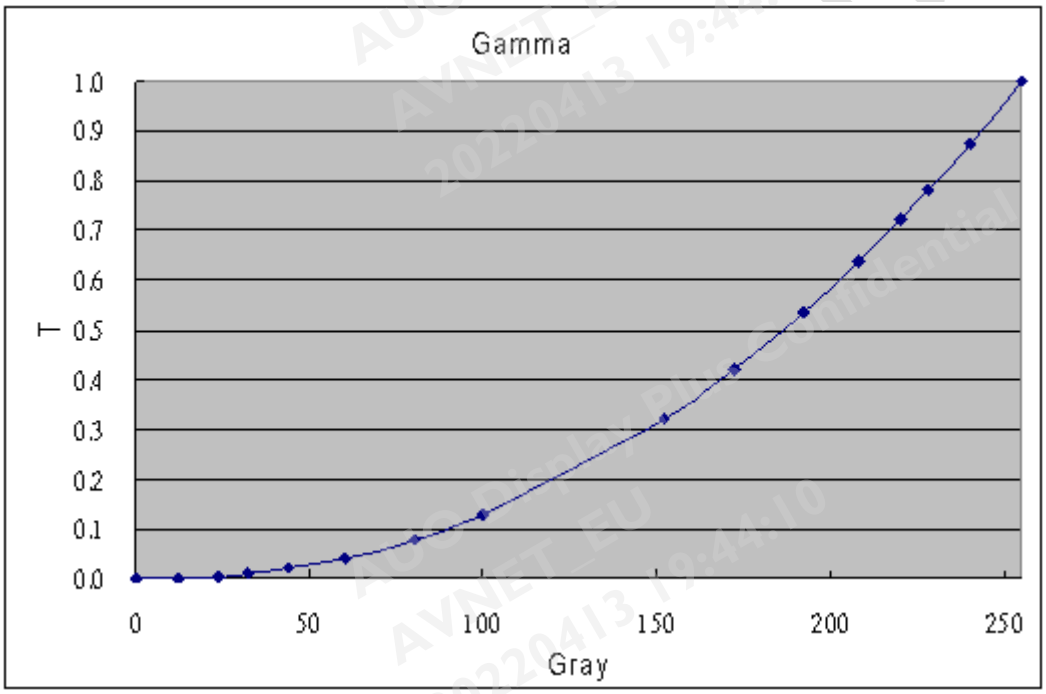
D6 ~ D0	Brightness gain
00h	Dark (-64)
40h	Center (0)(Default)
7Fh	Bright (+63)

R36 ~ R79:

No.	Register address								MSB		Register data					LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R36	0	0	1	0	0	1	0	0	x	x	GMA_V1+ (010101)					
R37	0	0	1	0	0	1	0	1	x	x	GMA_V2+ (011110)					
R38	0	0	1	0	0	1	1	0	x	x	x	x	GMA_V26+ (1011)			
R39	0	0	1	0	0	1	1	1	x	x	x	x	GMA_V37+ (0010)			
R40	0	0	1	0	1	0	0	0	x	x	GMA_V61+ (100100)					
R41	0	0	1	0	1	0	0	1	x	x	GMA_V62+ (100000)					
R42	0	0	1	0	1	0	1	0	x	x	GMA_V62- (011000)					
R43	0	0	1	0	1	0	1	1	X	x	GMA_V61- (011111)					
R44	0	0	1	0	1	1	0	0	x	x	x	x	GMA_V37- (0011)			
R45	0	0	1	0	1	1	0	1	x	x	x	x	GMA_V26- (1011)			
R46	0	0	1	0	1	1	1	0	x	x	GMA_V2- (011000)					
R47	0	0	1	0	1	1	1	1	x	x	GMA_V1- (001111)					
R48	0	0	1	1	0	0	0	0	x	x	GMA_V0+(001100)					
R49	0	0	1	1	0	0	0	1	x	x	GAM_V3+(100011)					
R50	0	0	1	1	0	0	1	0	x	x	GMA_V6+(101101)					
R51	0	0	1	1	0	0	1	1	x	x	x	GMA_V8+(01110)				
R52	0	0	1	1	0	1	0	0	x	x	x	GMA_V11+(01110)				
R53	0	0	1	1	0	1	0	1	x	x	x	GMA_V15+(10110)				
R54	0	0	1	1	0	1	1	0	x	x	x	x	GMA_V20+(1110)			
R55	0	0	1	1	0	1	1	1	x	x	x	x	GMA_V25+(1001)			
R56	0	0	1	1	1	0	0	0	x	x	x	x	GMA_V38+(0001)			
R57	0	0	1	1	1	0	0	1	x	x	x	x	GMA_V43+(1000)			
R58	0	0	1	1	1	0	1	0	x	x	x	GMA_V48+(00110)				
R59	0	0	1	1	1	0	1	1	x	x	x	GMA_V52+(01111)				
R60	0	0	1	1	1	1	0	0	x	x	x	GMA_V55+(01111)				
R61	0	0	1	1	1	1	0	1	x	x	GMA_V57+(101001)					
R62	0	0	1	1	1	1	1	0	x	x	GMA_V60+(100110)					
R63	0	0	1	1	1	1	1	1	x	x	GMA_V63+(001110)					
R64	1	0	0	0	0	0	0	0	x	x	GMA_V63-(000100)					
R65	1	0	0	0	0	0	0	1	x	x	GMA_V60-(100000)					
R66	1	0	0	0	0	0	1	0	x	x	GMA_V57-(00100100)					
R67	1	0	0	0	0	0	1	1	x	x	x	GMA_V55-(01110)				
R68	1	0	0	0	0	1	0	0	x	x	x	GMA_V52-(01101)				
R69	1	0	0	0	0	1	0	1	x	x	x	GMA_V48-(01001)				

R70	1	0	0	0	0	1	1	0	x	x	x	x	GAM_V43-(1001)
R71	1	0	0	0	0	1	1	1	x	x	x	x	GMA_V38-(0001)
R72	1	0	0	0	1	0	0	0	x	x	x	x	GMA_V25-(1001)
R73	1	0	0	0	1	0	0	1	x	x	x	x	GMA_V20-(1110)
R74	1	0	0	0	1	0	1	0	x	x	x	GAM_V15-(10010)	
R75	1	0	0	0	1	0	1	1	x	x	x	GMA_V11-(10000)	
R76	1	0	0	0	1	1	0	0	x	x	x	GMA_V8-(10000)	
R77	1	0	0	0	1	1	0	1	x	x	GMA_V6-(101000)		
R78	1	0	0	0	1	1	1	0	x	x	GMA_V3-(011101)		
R79	1	0	0	0	1	1	1	1	x	x	GMA_V0-(000110)		

16 adjustable points



R97:

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R97	1	0	1	0	0	0	0	1	x	x	x	x	x	x	GAMMA_ENABLE(10)	

GAMMA_ENABLE : Select auto or manual gamma setting

GAMMA_ENABLE	Description
11	Manual set gamma by R36~ R79.
10	Auto set to Default Gamma (Close to 2.2).

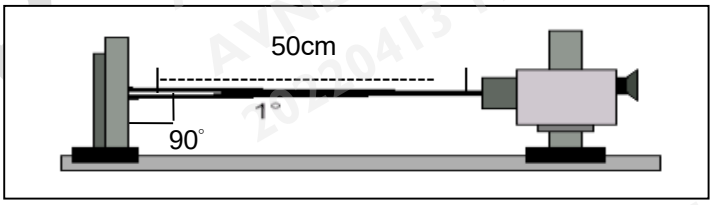
C. Optical Specification (Note1, Note 2 and Note 3)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall		 Tr Tf	θ=0°	 -- --	 10 25	 40 50	 ms ms	Note 4
Contrast ratio		CR	At optimized viewing angle	300	400	--		Note 5
Viewing Angle	Top	Φ_T	CR≧ 10	40	50	--	deg.	Note 6
	Bottom	Φ_B		50	60	--		
	Left	Φ_L		50	60	--		
	Right	Φ_R		50	60	--		
Brightness		Y_L	θ=0°	250	310	--	cd/m^2	Note 7, 8
Chromaticity	White	X	θ=0°	0.251	0.291	0.331		
		Y	θ=0°	0.272	0.312	0.352		
Uniformity		ΔY_L	%	70	75	--	%	Note 9

Note 1. Ambient temperature =25□.

Note 2. To be measured in the dark room.

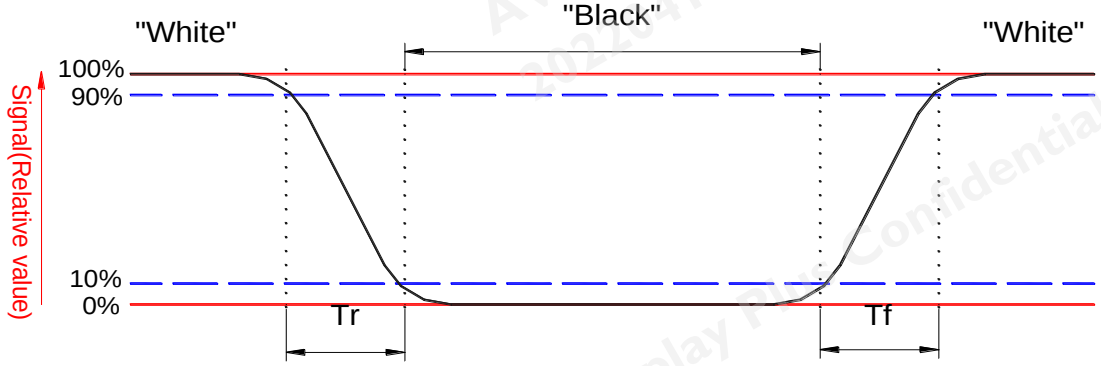
Note 3. To be measured on the center area of panel with a field angle of 1° by Topcon luminance meter BM-5A, after 10 minutes operation.



Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

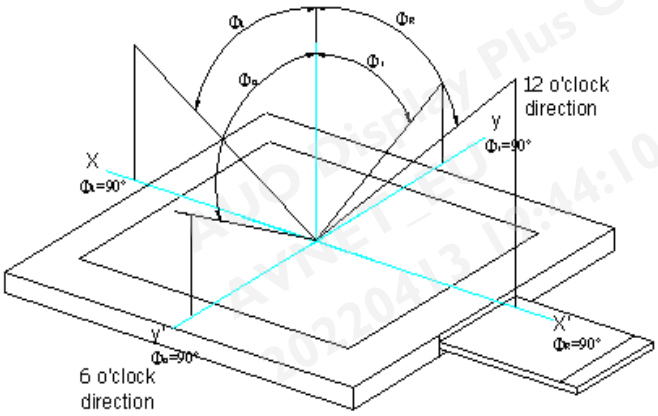


Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

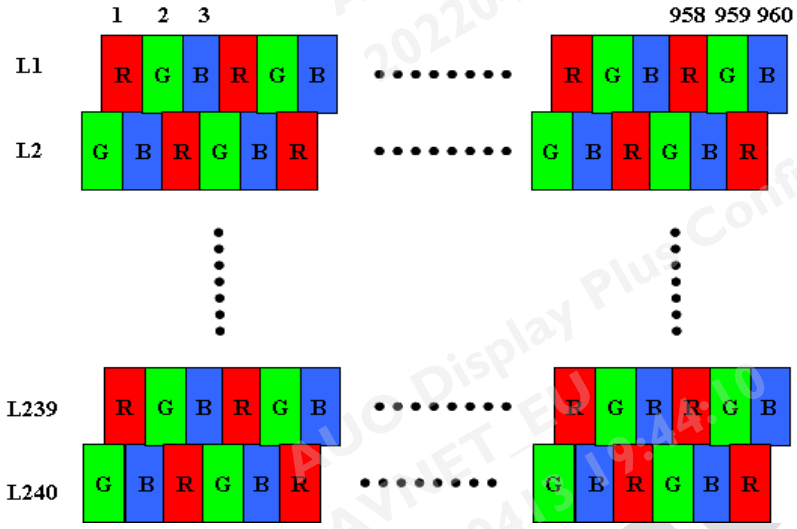
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. Definition of viewing angle, Φ, Refer to figure as below.

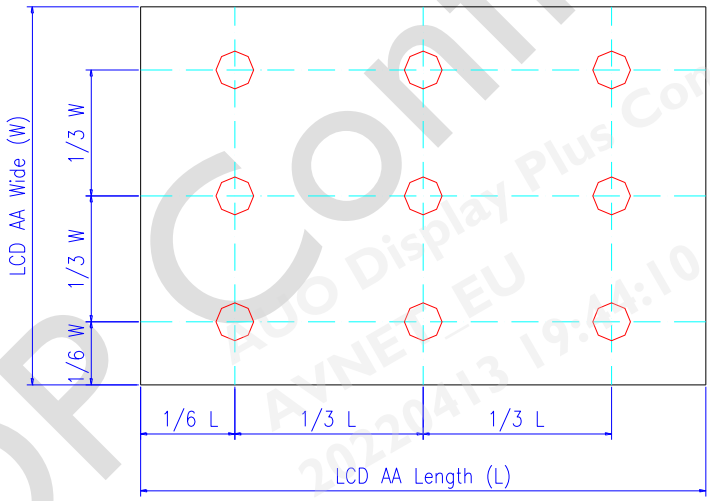


Note 7. Measured at the center area of the panel in white pattern based on 3,4 Backlight driving conditions to setup LED current.

Note 8. Color Filter Arrangement



Note 9. Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

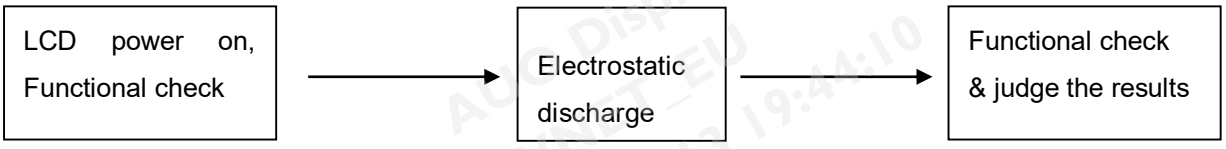
D. Reliability Test Items

No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70℃ 240Hrs	
2	Low Temperature Storage	Ta= -25℃ 240Hrs	
3	High Temperature Operation	Ta= 60℃ 240Hrs	
4	Low Temperature Operation	Ta= 0℃ 240Hrs	
5	High Temperature & High Humidity	Ta= 60℃ 90% RH 240Hrs	Operation
6	Heat Shock	Ta= -25℃~80℃/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	Note 3,4
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1. Ta: Ambient temperature.

Note 2. For item 1 through 6, the test method: check with recovery time 2hrs in the laboratory environment

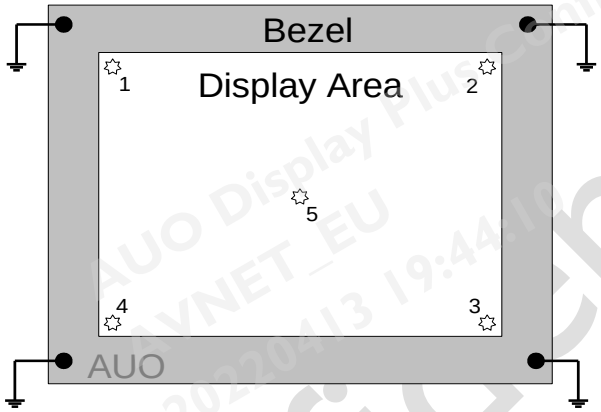
Note 3. ESD Testing Flow as the below,



Note 4. ESD testing method.

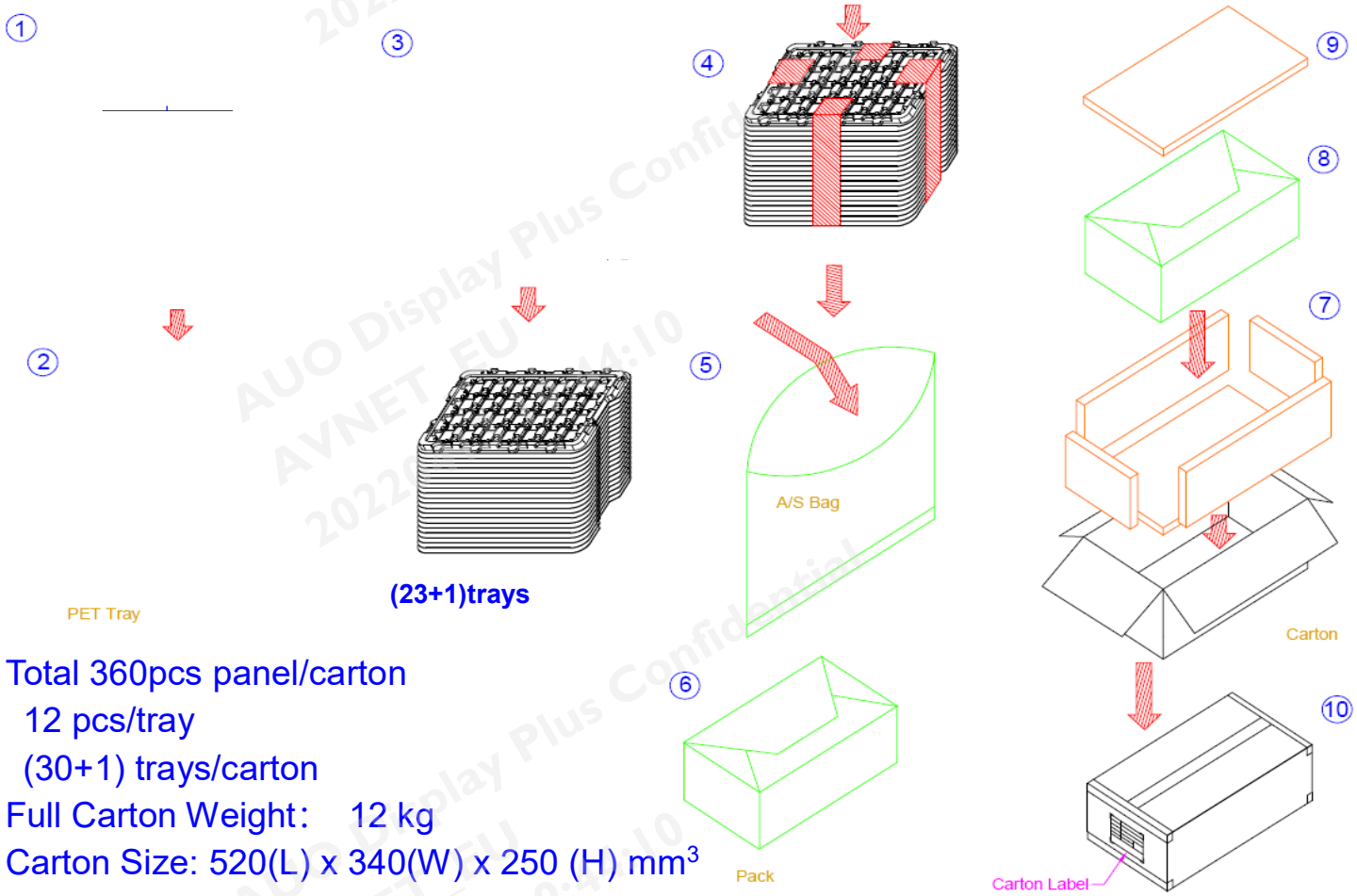
1. Ambient: 24~26℃, 56~65%RH

2. Instruments:NoisekenESS-2000,
3. Operation System: “CP-TEST” and adapter “A027DTN01.9 T2”
4. Test Mode: Operating mode, test pattern: colorbar+8Gray scale
5. Test Method:
    a. Contact Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
    b. Air Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
6. Test point:



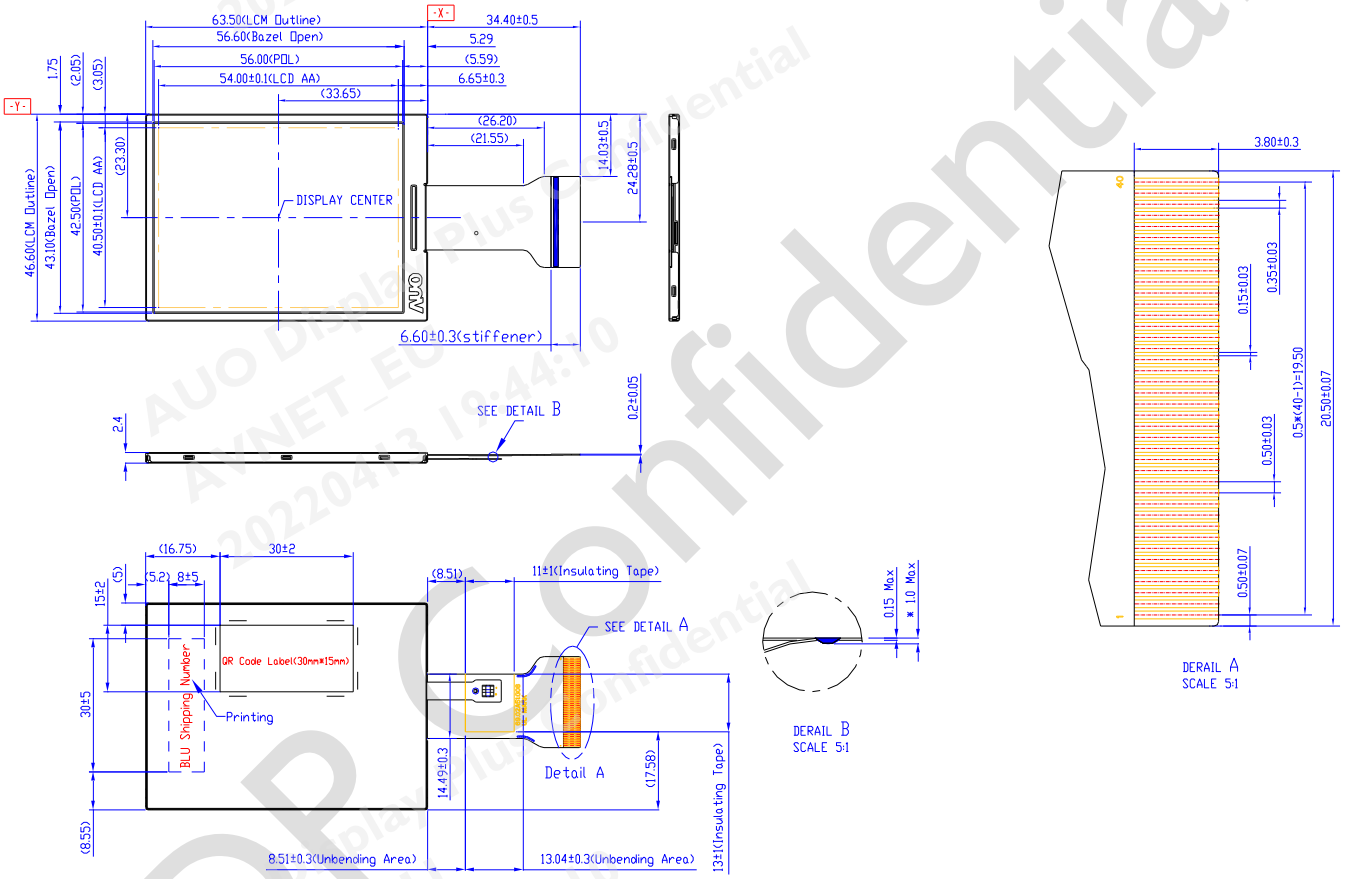
7. The metal casing is connected to power supply ground (0V) at four corners.
8. All register commands are repeating transfer.

E. Packing Form



Total 360pcs panel/carton
12 pcs/tray
(30+1) trays/carton
Full Carton Weight: 12 kg
Carton Size: 520(L) x 340(W) x 250 (H) mm^3

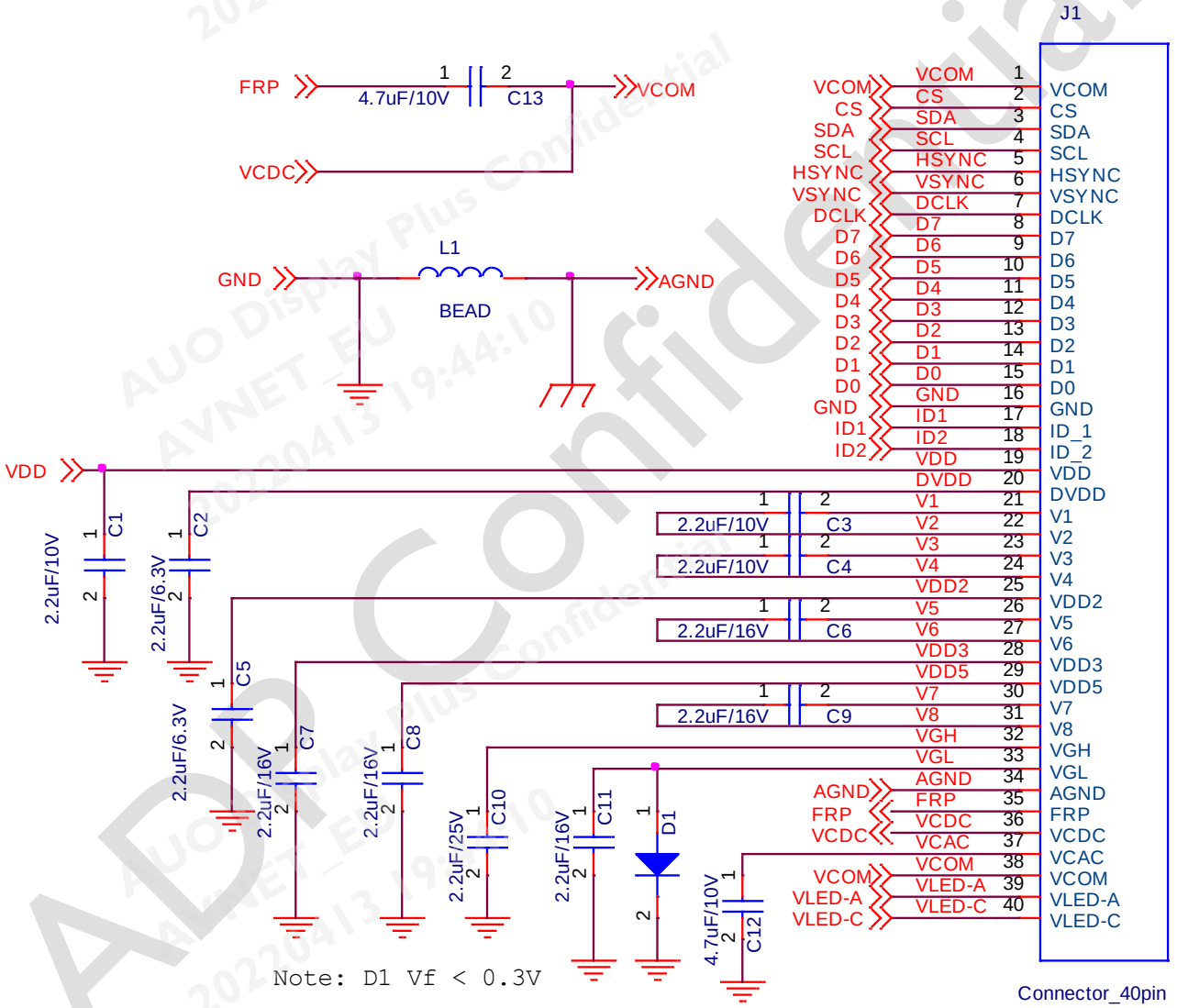
F. Outline dimension



1. Any stress or attachment on the back of the LCD module is forbidden.
2. The protection film in the back side of LCM should be torn off before assembly

QR Application note

1. Application circuit



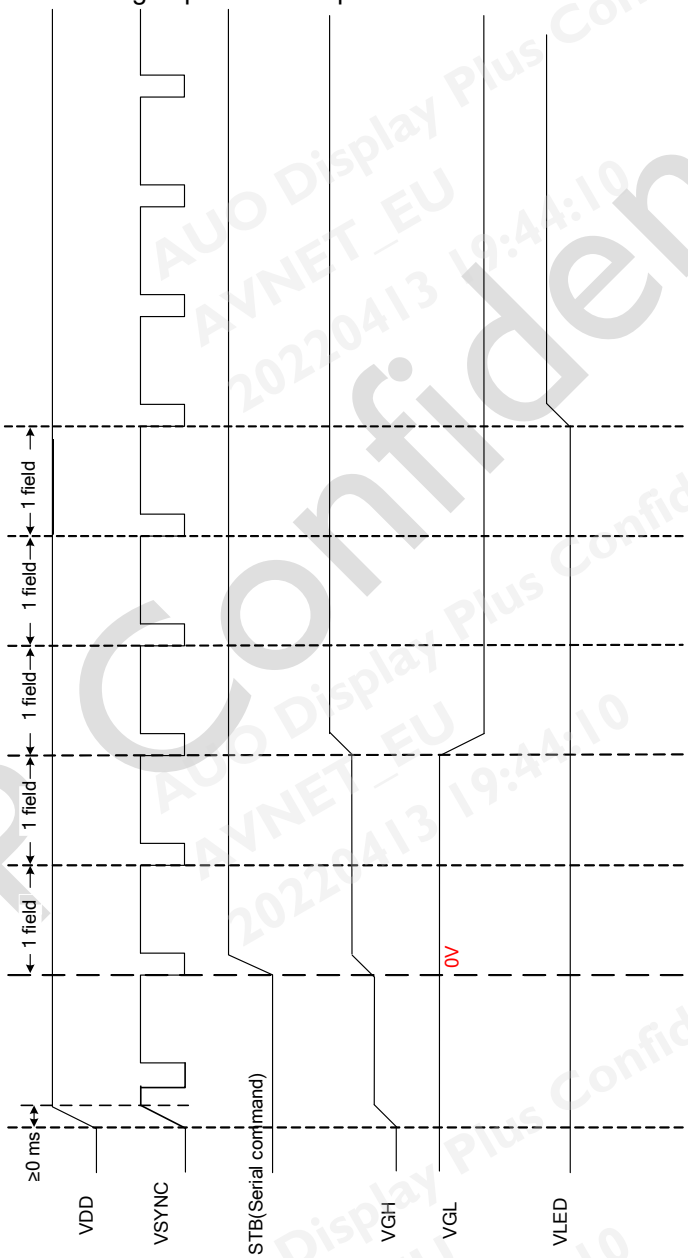
Note2: 1.Use external LED driver must set R5[1](SHDB1)= ”0”.
2.D1 forward voltage (Vf) is less than 0.3V (Condition 10 mA).

2. Power on/off sequence

The register setting of standby mode disabling / enabling is used to control the build-in power on / off sequence.

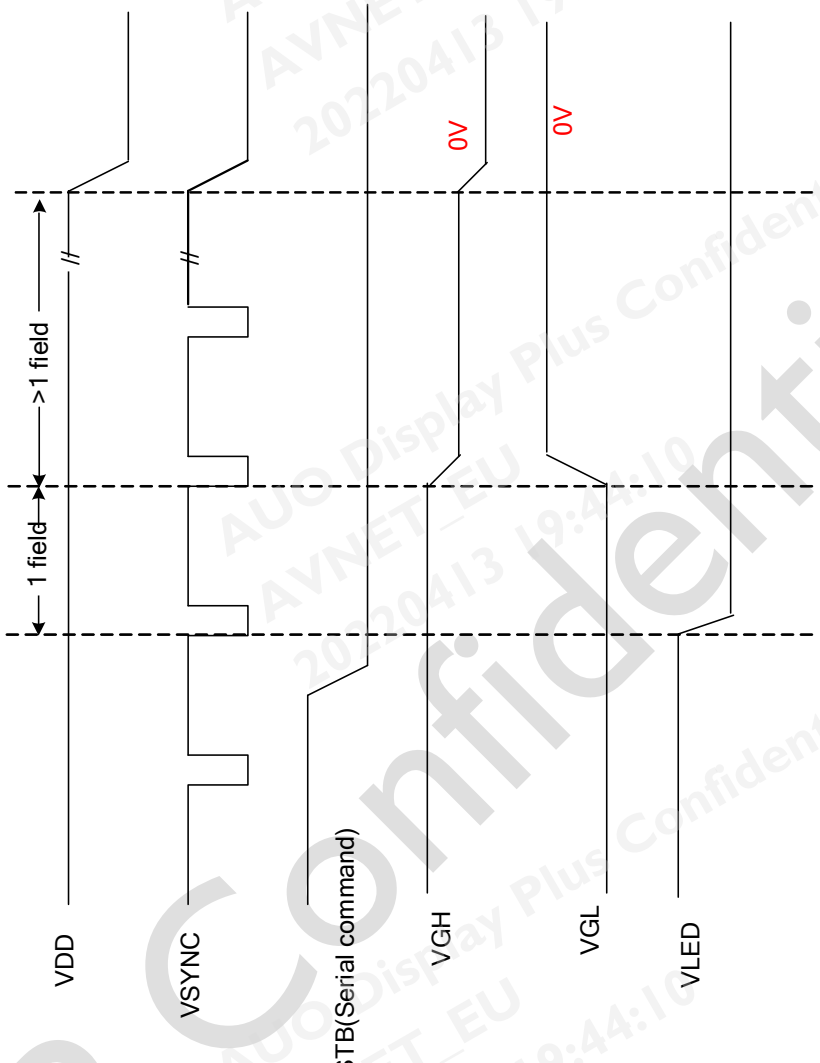
2.1 Power on (Standby Disabling)

Firstly, AUO recommaned a single VDD power-on voltage waveform slope which can refer to VDD waveform below; meantime, IC will perform a power-on reset function. Later, VSYNC/HSYNC/DCLK/DATA can be input. After the second VSYNC falling event, the serial control interface can be operative, too. The LCD driver is in default standby mode when power-on reset is functional. Set register R5: STB to '1' to disable the standby mode is required for normal operation. When the standby mode is disabled, a build-in power-on sequence is started. The LCD positive and negative power supplies VGH/VGL are pumped first, and followed by the LED power VLED. Please refer to the detail timing of power on sequence.



2.2 Power off (Standby Enabling)

When the register STB is set to '0' to enable standby mode, a build-in power off sequence is started. Please refer to Fig.11 for the detail timing of power off sequence.



3. Recommended power on/off serial command settings

3.1 UPS051

POWER ON

Recommended power on serial command settings				
Register	**Address**	**Data**	**Hex**	**Remark**
VDD ON				Rising time < 50 ms (Max)
		Delay 0 ms (Min.)		
		DCLK / HSYNC / VSYNC / DATA start		
		After two Vsync falling events(Min.)		
		Start command settings		
R5	00000101	01000100	0544	GRB='1'
R5	00000101	00000100	0504	GRB='0', Reset
R5	00000101	01000100	0544	GRB='1'
		Delay 40ms		
R5	00000101	01000100	0544	GRB='1'
R5	00000101	00000100	0504	GRB='0', Reset
R5	00000101	01000100	0544	GRB='1'
R1	00000001	10110100	01B4	VcomDC setting
R4	00000100	00001011	040B	UPS051 mode
R36-79	-	-	-	Gamma 2.2 Setting (P50-51)
RXX	-	-	-	Other Register Setting
R05	00000101	01000101	0545	Release standby

1 field : NTSC = 16.6 ms; PAL = 20 ms

POWER OFF

Recommended power off serial command settings				
Register	**Address**	**Data**	**Hex**	**Remark**
R5	00000101	01000100	0544	Set standby
		Delay 2 fields (min)		
		DCLK / HSYNC / VSYNC / DATA stop		
		Delay 0 ms (min)		
		VDD OFF		

1 field : NTSC = 16.6 ms; PAL = 20 ms

3.2 UPS052 320 mode

POWER ON

Recommended power on serial command settings				
Register	**Address**	**Data**	**Hex**	**Remark**
VDD ON				Rising time < 50 ms (Max)
Delay 0 ms (Min)				
DCLK / HSYNC / VSYNC / DATA start				
After two Vsync falling events(Min.)				
Start command settings				
R5	00000101	01000100	0544	GRB='1'
R5	00000101	00000100	0504	GRB='0', Reset
R5	00000101	01000100	0544	GRB='1'
Delay 40ms				
R5	00000101	01000100	0544	GRB='1'
R5	00000101	00000100	0504	GRB='0', Reset
R5	00000101	01000100	0544	GRB='1'
R1	00000001	10110100	01B4	VcomDC setting
R4	00000100	00011011	041B	UPS052 320 mode
RXX	-	-	-	Other Register Setting
R05	00000101	01000101	0545	Release standby

1 field : NTSC = 16.6 ms; PAL = 20 ms
Use internal LED driver setting (R5[1] = "1").

POWER OFF

Recommended power off serial command settings				
Register	**Address**	**Data**	**Hex**	**Remark**
R5	00000101	01000100	0544	Set standby
Delay 2 fields (min)				
DCLK / HSYNC / VSYNC / DATA stop				
Delay 0 ms (min)				
VDD OFF				

1 field : NTSC = 16.6 ms; PAL = 20 ms

3.3 UPS052 360 mode

POWER ON

Recommended power on serial command settings				
Register	**Address**	**Data**	**Hex**	**Remark**
VDD ON				Rising time < 50 ms (Max)
Delay 0 ms (Min)				
DCLK / HSYNC / VSYNC / DATA start				
After two Vsync falling events(Min.)				
Start command settings				
R5	00000101	01000100	0544	GRB='1'
R5	00000101	00000100	0504	GRB='0', Reset
R5	00000101	01000100	0544	GRB='1'
Delay 40ms				
R5	00000101	01000100	0544	GRB='1'
R5	00000101	00000100	0504	GRB='0', Reset
R5	00000101	01000100	0544	GRB='1'
R1	00000001	10110100	01B4	VcomDC setting
R4	00000100	00101011	042B	UPS052 360 mode
RXX	-	-	-	Other Register Setting
R05	00000101	01000101	0545	Release standby

1 field : NTSC = 16.6 ms; PAL = 20 ms
Use internal LED driver setting (R5[1] = "1").

POWER OFF

Recommended power off serial command settings				
Register	**Address**	**Data**	**Hex**	**Remark**
R5	00000101	01000100	0544	Set standby
Delay 2 fields (min)				
DCLK / HSYNC / VSYNC / DATA stop				
Delay 0 ms (min)				
VDD OFF				

1 field : NTSC = 16.6 ms; PAL = 20 ms

3.4 CCIR656

POWER ON

Recommended power on serial command settings				
Register	**Address**	**Data**	**Hex**	**Remark**
VDD ON				Rising time < 50 ms (Max)
Delay 0 ms (Min)				
DCLK / HSYNC / VSYNC / DATA start				
After two Vsync falling events(Min.)				
Start command settings				
R5	00000101	01000100	0544	GRB='1'
R5	00000101	00000100	0504	GRB='0', Reset
R5	00000101	01000100	0544	GRB='1'
Delay 40ms				
R5	00000101	01000100	0544	GRB='1'
R5	00000101	00000100	0504	GRB='0', Reset
R5	00000101	01000100	0544	GRB='1'
R1	00000001	10110100	01B4	VcomDC setting
R4	00000100	01101011	046B	CCIR656 mode
RXX	-	-	-	Other Register Setting
R05	00000101	01000101	0545	Release standby

1 field : NTSC = 16.6 ms; PAL = 20 ms
Use internal LED driver setting (R5[1] = "1").

POWER OFF

Recommended power off serial command settings				
Register	**Address**	**Data**	**Hex**	**Remark**
R5	00000101	01000100	0544	Set standby
Delay 2 fields (min)				
DCLK / HSYNC / VSYNC / DATA stop				
Delay 0 ms (min)				
VDD OFF				

1 field : NTSC = 16.6 ms; PAL = 20 ms

3.5 YUV 720

POWER ON

Recommended power on serial command settings				
Register	**Address**	**Data**	**Hex**	**Remark**
VDD ON				Rising time < 50 ms (Max)
Delay 0 ms (Min)				
DCLK / HSYNC / VSYNC / DATA start				
After two Vsync falling events(Min.)				
Start command settings				
R5	00000101	01000100	0544	GRB='1'
R5	00000101	00000100	0504	GRB='0', Reset
R5	00000101	01000100	0544	GRB='1'
Delay 40ms				
R5	00000101	01000100	0544	GRB='1'

R5	00000101	00000100	0504	GRB='0', Reset
R5	00000101	01000100	0544	GRB='1'
R1	00000001	10110100	01B4	VcomDC setting
R0	00000000	01000011	0043	Set CCIR601='1'
R4	00000100	01101011	046B	YUV 720 mode
RXX	-	-	-	Other Register Setting
R05	00000101	01000101	0545	Release standby

1 field : NTSC = 16.6 ms; PAL = 20 ms
Use internal LED driver setting (R5[1] = "1").

POWER OFF

Recommended power off serial command settings				
Register	**Address**	**Data**	**Hex**	**Remark**
R5	00000101	01000100	0544	Set standby
Delay 2 fields (min)				
DCLK / HSYNC / VSYNC / DATA stop				
Delay 0 ms (min)				
VDD OFF				

1 field : NTSC = 16.6 ms; PAL = 20 ms

3.6 YUV 640

POWER ON

Recommended power on serial command settings				
Register	**Address**	**Data**	**Hex**	**Remark**
VDD ON				Rising time < 50 ms (Max)
Delay 0 ms (Min)				
DCLK / HSYNC / VSYNC / DATA start				
After two Vsync falling events(Min.)				
Start command settings				
R5	00000101	01000100	0544	GRB='1'
R5	00000101	00000100	0504	GRB='0', Reset
R5	00000101	01000100	0544	GRB='1'
Delay 40ms				
R5	00000101	01000100	0544	GRB='1'
R5	00000101	00000100	0504	GRB='0', Reset
R5	00000101	01000100	0544	GRB='1'
R1	00000001	10110100	01B4	VcomDC setting
R0	00000000	01000011	0043	Set CCIR601='1'
R4	00000100	01001011	044B	YUV 640 mode
RXX	-	-	-	Other Register Setting
R05	00000101	01000101	0545	Release standby

1 field : NTSC = 16.6 ms; PAL = 20 ms
Use internal LED driver setting (R5[1] = "1").

POWER OFF

Recommended power off serial command settings				
Register	**Address**	**Data**	**Hex**	**Remark**
R5	00000101	01000100	0544	Set standby
Delay 2 fields (min)				
DCLK / HSYNC / VSYNC / DATA stop				
Delay 0 ms (min)				
VDD OFF				

1 field : NTSC = 16.6 ms; PAL = 20 ms