



晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR LCD MODULE

Customer	
Customer part no.	
Ampire part no.	AM-320240NMZQW-W0H-A(R)
Approved by	
Date	

☐ Preliminary Specification

☒ Formal Specification

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*This specification is subject to change without notice.

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2022/10/24	--	New Release	Tank

1 Features

5.7 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module. This module is composed of a 5.7" TFT-LCD panel, LCD controller, a driver circuit and backlight unit.

1.1 TFT Panel Feature :

- (1) Construction: 5.7" a-Si color TFT-LCD, White LED / CCFL Backlight and PCB.
- (2) Resolution (pixel): 320(R.G.B) X240
- (3) Number of the Colors : 262K colors (R , G , B 6 bit digital each)
- (4) LCD type : Transmissive Color TFT LCD (Normally Black)
- (5) Interface: 40 pin pitch 0.5 FFC
- (6) Power Supply Voltage: 3.3V single power input. Built-in power supply circuit.
- (7) Viewing Direction: All Direction.

1.2 LCD Controller Feature:

- (1) MCU interface 8/9/16/18 bit 80&68 series MCU interface.
- (2) Display RAM size : 640x240x3x6 bits. Ex:320x240 two frame buffer with 262K colors.
- (3) Arbitrary display memory start position selection.
- (4) MCU interface : 8 bit 80 MPU interface.
- (5) 8 bit / 16 bit interface support 65K (R5G6B5) /262K(R6G6B6) colors data format.
- (6) 9 bit / 18 bit interface support 262K(R6G6B6) colors data format only.

2 Physical specifications

Item	Specifications	Unit
Display Resolution(Dot)	320(RGB)(W) x 240(H)	dot
Pixel Size	0.36(W) x 0.36(H)	mm
Active Area	115.2(W) x 86.4(H)	mm
Screen Size	5.7(Diagonal)	mm
Color Configuration	R.G.B Stripe	
Overall Dimension	131.0(W) x 102.2(H) x 12.4(D)	mm
Backlight Unit	LED	
Contrast Ratio	1000:1 (Typ.)	

3 Default Setting & Option

- Interface:

The user can select the MCU interface by change the Jumper & Resister Array.

Setting Interface Type	JP1	RA1	RA2	RA3	RA4	Remark
80-18Bit interface	1,2 short 2,3 open	2K ohm	OPEN	OPEN	OPEN	
80-16Bit interface	1,2 short 2,3 open	OPEN	2K ohm	OPEN	OPEN	
80-9Bit interface	1,2 short 2,3 open	OPEN	OPEN	2K ohm	OPEN	
80-8Bit interface	1,2 short 2,3 open	OPEN	OPEN	OPEN	2K ohm	Default
68-18Bit interface	1,2 open 2,3 short	2K ohm	OPEN	OPEN	OPEN	
68-16Bit interface	1,2 open 2,3 short	OPEN	2K ohm	OPEN	OPEN	
68-9Bit interface	1,2 open 2,3 short	OPEN	OPEN	2K ohm	OPEN	
68-8Bit interface	1,2 open 2,3 short	OPEN	OPEN	OPEN	2K ohm	

- Touch panel and Touch panel controller:

The user can select the with TP controller or without TP controller.

Pin Define Option	SK/X1	DO/X2	DI/Y1	TPCS/Y2	IRQ	Remark
Without TP	NC	NC	NC	NC	NC	Default
With TP / Without TP controller	X1	X2	Y1	Y2	NC	
With TP / With TP controller	SK	DO	DI	TPCS	IRQ	

If user wants to change the default setting for mass production, please contact with Ampire. We'll apply a new P/N for you.

4 Electrical specification

4.1 Absolute max. ratings

4.1.1 Electrical Absolute max. ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power Voltage	V_{DD}	$V_{SS}=0$	-0.3	5.5	V	
Input Voltage	V_{IN}		-0.3	$V_{DD}+0.3$	V	Note 1

Note1: /CS,/WR,/RD,RS,DB0~DB7

4.1.2 Environmental Absolute max. ratings

Item	OPERATING		STORAGE		Remark
	MIN	MAX	MIN	MAX	
Temperature	-20	70	-30	80	Note2,3,4,5,6,7
Humidity	Note1		Note1		
Corrosive Gas	Not Acceptable		Not Acceptable		

Note1 : $T_a \leq 40^{\circ}\text{C}$: 85% RH max

$T_a > 40^{\circ}\text{C}$: Absolute humidity must be lower than the humidity of 85%RH at 40°C

Note2 : For storage condition T_a at $-30^{\circ}\text{C} < 240\text{h}$, at $80^{\circ}\text{C} < 240\text{h}$

For operating condition T_a at $-20^{\circ}\text{C} < 240\text{h}$, at $70^{\circ}\text{C} < 240\text{h}$

Note3 : Background color changes slightly depending on ambient temperature. This phenomenon is reversible.

Note4 : The response time will be slower at low temperature.

Note5 : Only operation is guaranteed at operating temperature. Contrast , response time, another display quality are evaluated at $+25^{\circ}\text{C}$

Note6 : When LCM is operated over 40°C ambient temperature, the I_{LED} of the LED back-light should be follow :

Note7 : This is panel surface temperature, not ambient temperature.

Note8 : When LCM be operated over than 40°C , the life time of the LED back-light will be reduced.

4.2 Electrical characteristics

4.2.1 DC Electrical characteristic of the LCD

Typical operating conditions (VSS=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		V _{DD}	3.1	3.3	5.0	V	
Input Voltage for logic	H Level	V _{IH}	2.0	-	V _{DD}	V	Note 1
	L Level	V _{IL}	V _{SS}	-	0.8	V	
Power Supply current		I _{DD}		T.B.D.		mA	Note 2

Note1: /CS, /WR, /RD, RS, DB0~DB17

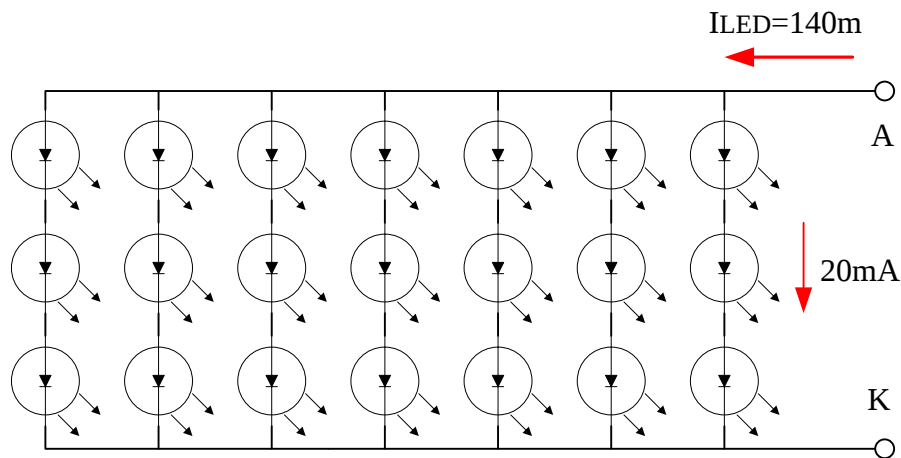
Note2: f_v =60Hz, VDD=3.3V, Ta=25°C, [Display Pattern: All White](#)

4.2.2 Electrical characteristic of LED Back-light

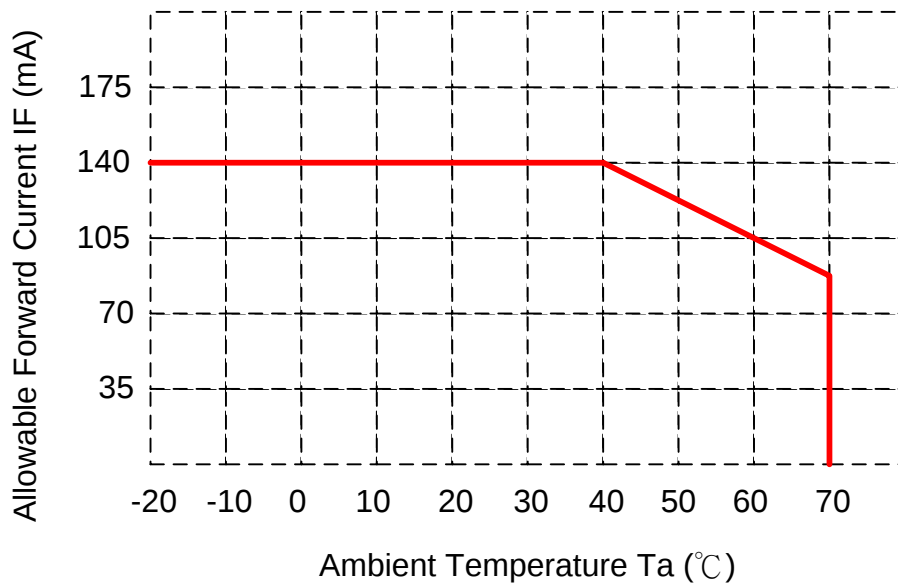
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LED Voltage	V_{AK}	8.4	9.6	10.8	V	$I_{LED} = 140mA$, $T_a = 25^{\circ}C$
LED Forward Current	I_{LED}	--	126	140	mA	$T_a = 25^{\circ}C$
	I_{LED}	--	84	105	mA	$T_a = 60^{\circ}C$
LED Life Time	--	--	30K	--	hours	Note 1

Note 1: End of Life shall be determined by the time when any of the following is satisfied under continuous lighting at $25^{\circ}C$ and $I_{LED} = 126mA$.

- Intensity drops to 50% of the Initial Value (Min. Luminance)
- Based on LED
- It is an estimative value

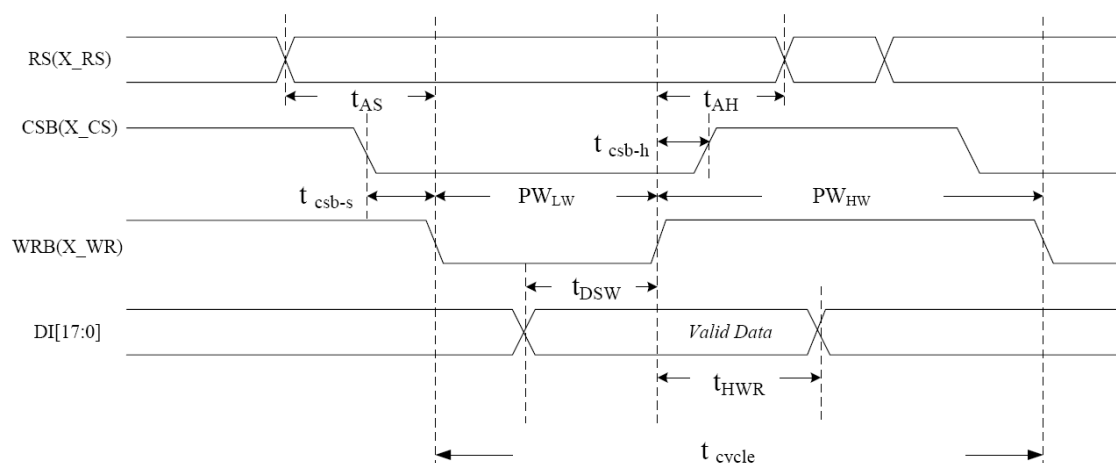


■ The constant current source is needed for white LED back-light driving. When LCM is operated over $60^{\circ}C$ ambient temperature, the I_{LED} of the LED back-light should be adjusted to 105mA max



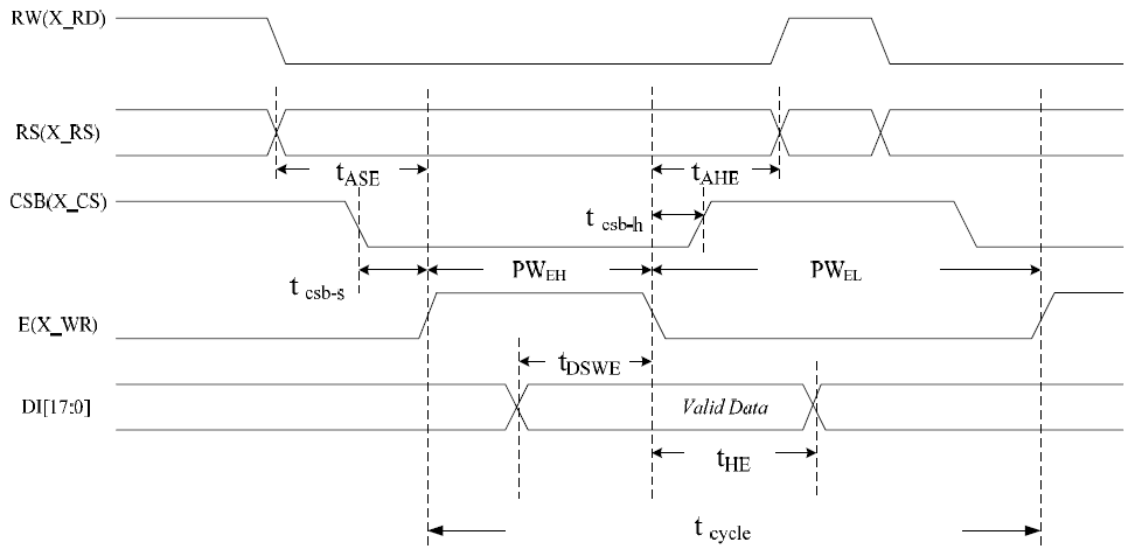
4.3 AC Timing characteristic of the Graphic TFT LCD controller

4.3.1 80 series Timing



Symbol	Parameter	Min	Typ.	Max	Unit	Remark
t_{cycle}	Enable cycle time	100	200		ns	
PW_{HW}	Enable high-level pulse width	66	70		ns	
PW_{LW}	Enable low-level pulse width	33	130		ns	
t_{AS}	RS setup time	16	25		ns	
t_{AH}	RS hold time	16	45		ns	
t_{DSW}	Write data setup time	50	50		ns	
t_{HWR}	Write data hold time	50	40		ns	
t_{csb-s}	CSB setup time	16	20		ns	
t_{csb-h}	CSB hold time	16	30		ns	

4.3.2 68series Timing



Symbol	Parameter	Min	Typ.	Max	Unit	Remark
t_{cycle}	Enable cycle time	100	200		ns	
PW_{EH}	Enable high-level pulse width	66	70		ns	
PW_{EL}	Enable low level pulse width	33	130		ns	
t_{ase}	RS setup time	16	25		ns	
t_{ah}	RS hold time	16	45		ns	
t_{DSWE}	Write data setup time	50	50		ns	
t_{HE}	Write data hold time	50	40		ns	
t_{csb-s}	CSB setup time	16	20		ns	
t_{csbh}	CSB hold time	16	30		ns	

5 Optical specification

5.1 Optical Characteristic:

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time	Rise Fall	T_r T_f	$\Theta=0^\circ$	- -	35	45	ms	Note 1,2,3,5
Contrast ratio		CR	At optimized viewing angle	700	1000	-		Note 1,2,4,5
Viewing Angle	Top Bottom Left Right		$CR \geq 10$	70 70 70 70	80 80 80 80	- - - -	deg.	Note1,2, 5,6
Brightness		Y_L	$I_{LED}=140mA$, $25^\circ C$	400	500	-	cd/m ²	
Red chromaticity		XR	$\Theta=0^\circ$ $\Theta=0^\circ$	Typ. -0.05	0.638	Typ. +0.05		Note 7 For reference only. These data should be update according the prototype.
		YR			0.312			
Green chromaticity		XG			0.278			
		YG			0.538			
Blue chromaticity		XB			0.147			
		YB			0.115			
White chromaticity		XW			0.312			
		YW			0.356			

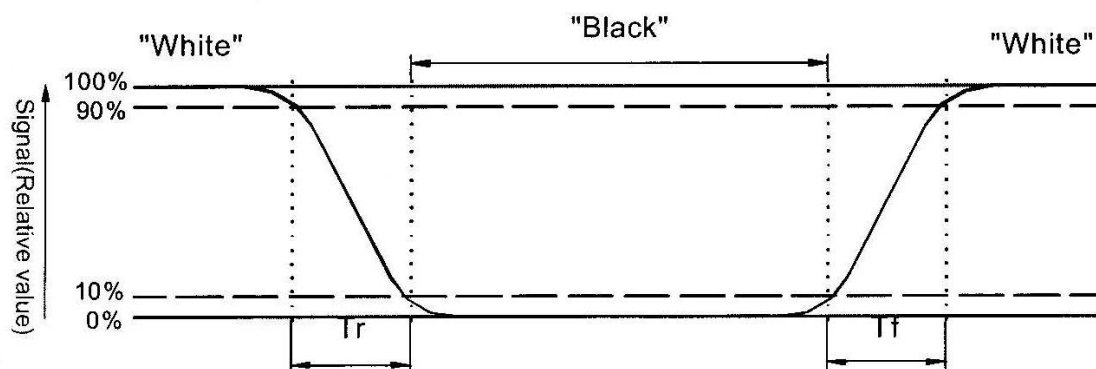
() For reference only. These data should be update according the prototype.

Note 1: LED BL :Ambient temperature= $25^\circ C$,and lamp current $I_{LED}=140mA$.To be measured in the dark room.

Note 2:To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-7,after 10 minutes operation.

Note 3.Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from"white" to "black" (rising time),respectively.The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector Output when LCD is at "Black" state}}$$

Note 5: White $V_i = V_{i50} + 1.5V$

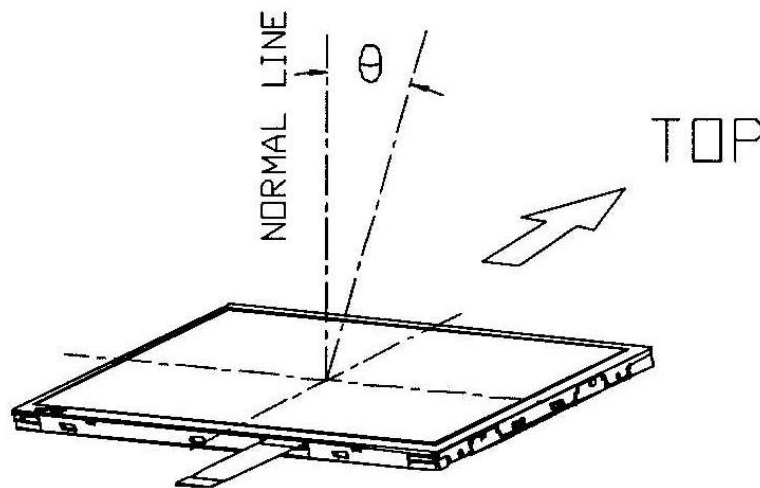
Black $V_i = V_{i50} + 2.0V$

“±” means that the analog input signal swings in phase with V_{COM} signal.

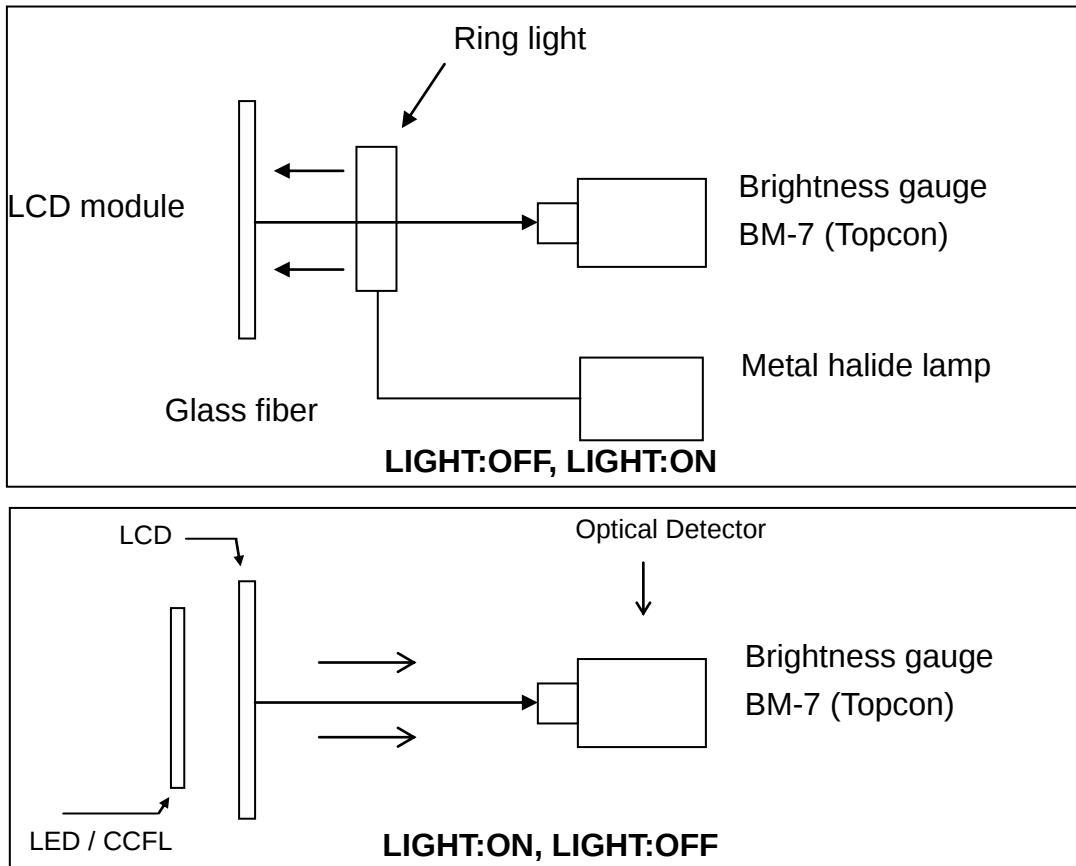
“ $\frac{-}{+}$ ” means that the analog input signal swings out of phase with V_{COM} signal.

V_{i50} : The analog input voltage when transmission is 50%. The 100% Transmission is defined as the transmission of LCD panel when all the Input terminals of module are electrically opened.

Note 6. Definition of viewing angle, Refer to figure as below.



Note 7.Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.



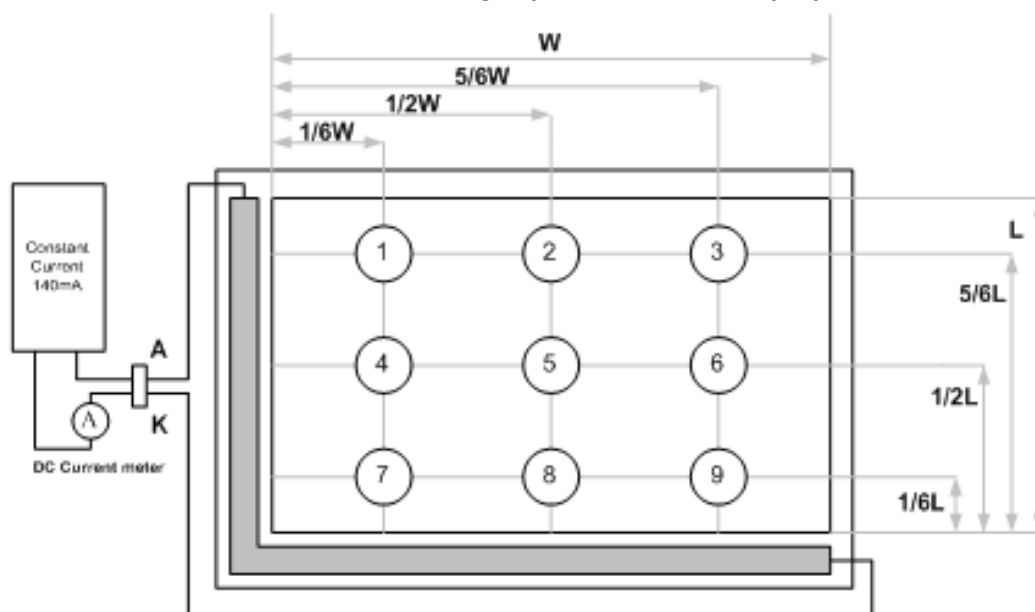
5.2 Optical characteristic of the Back-light

ITEM	MIN	TYP	MAX	UNIT	Condition
AVG. X of 1931 C.I.E.	0.28	0.31	0.34	--	$I_{LED} = 140mA, T_a = 25^{\circ}C$
AVG. Y of 1931 C.I.E.	0.28	0.31	0.34	--	$I_{LED} = 140mA, T_a = 25^{\circ}C$
Brightness Uniformity	80	--	--	%	$I_{LED} = 140mA, T_a = 25^{\circ}C$

() For reference only. These data should be update according the prototype.

Note1 : Measurement after 10 minutes from LED BL operating.

Note2 : Measurement of the following 9 places on the display.



Note3: The Uniformity definition

$(\text{Min Brightness} / \text{Max Brightness}) \times 100\%$

6 Interface specifications

6.1 Driving signals for the TFT panel

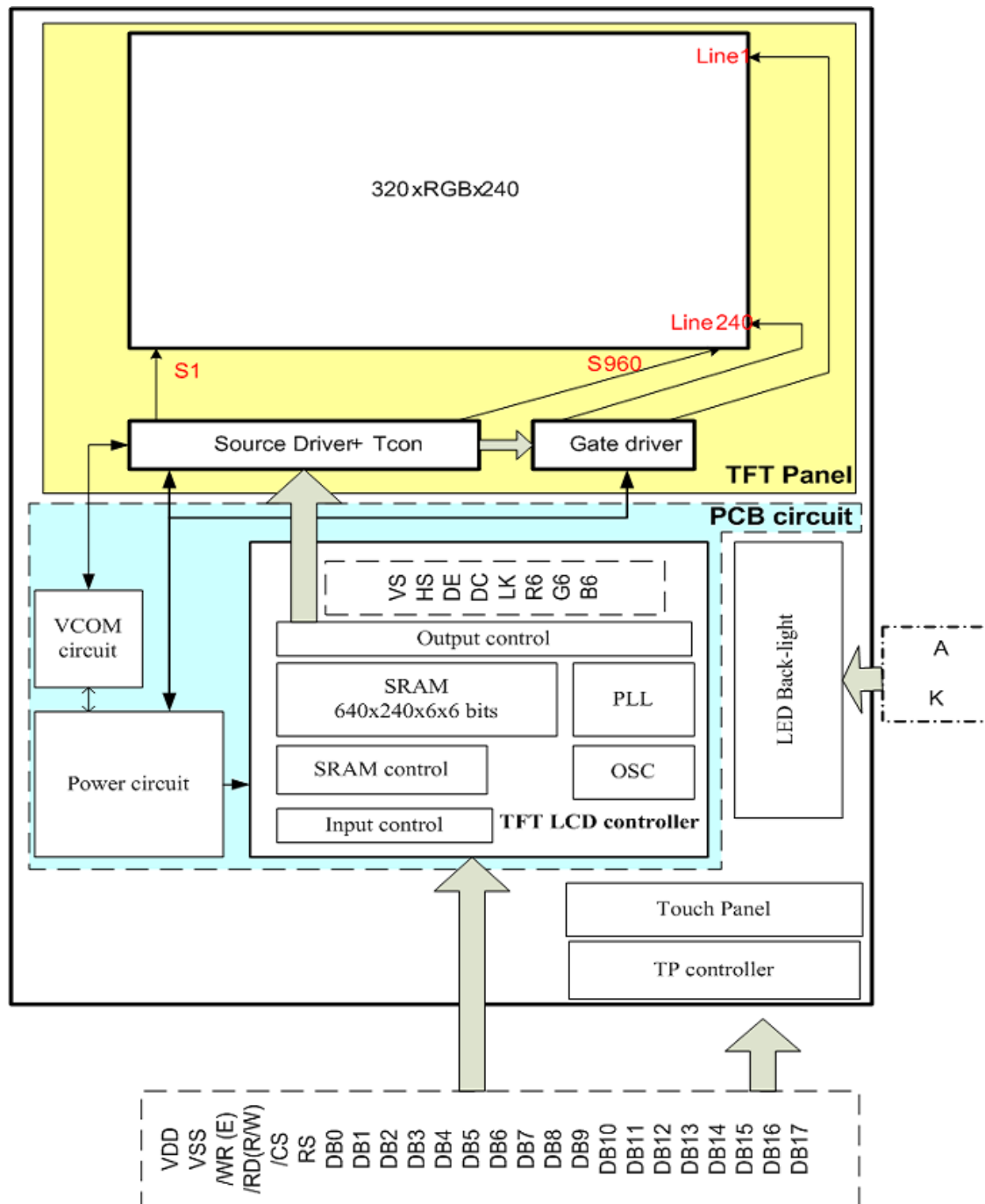
Pin no	Symbol	I/O	Description	Remark
1	DGND		GND	
2	DGND		GND	
3	NC		No connection	
4	NC		No connection	
5	/RESET	H/L	Reset signal for TFT LCD controller	
6	RS	H/L	Register and Data select for TFT LCD controller	
7	/CS	H/L	Chip select low active signal for TFT LCD controller	
8	/WR	H/L	80mode : /WR low active signal for TFT LCD controller 68mode : E signal latch on rising edge	
9	/RD	H/L	80mode : /RD low active signal for TFT LCD controller 68mode : R/W signal H: read L: Write	
10	DB0	I	Data Input	
11	DB1	I	Data Input	
12	DB2	I	Data Input	
13	DB3	I	Data Input	
14	DB4	I	Data Input	
15	DB5	I	Data Input	
16	DB6	I	Data Input	
17	DB7	I	Data Input	
18	DB8	I	Data Input	
19	DB9	I	Data Input	
20	DB10	I	Data Input	
21	DB11	I	Data Input	
22	DB12	I	Data Input	
23	DB13	I	Data Input	
24	DB14	I	Data Input	
25	DB15	I	Data Input	
26	DB16	I	Data Input	
27	DB17	I	Data Input	
28	65K/262K	H/L	Select color data form. H: 262K L: 65K	
29	DGND		GND	
30	NC		No connection	
31	NC		No connection	
32	NC		No connection	
33	NC		No connection	
34	NC		No connection	
35	VDD		Power supply for the logic	
36	VDD		Power supply for the logic	
37	VDD		Power supply for the logic	
38	DGND		GND	
39	DGND		GND	
40	DGND		GND	

6.2 Driving signals for the LED back-light

JST Housing: BHR-03VS-1

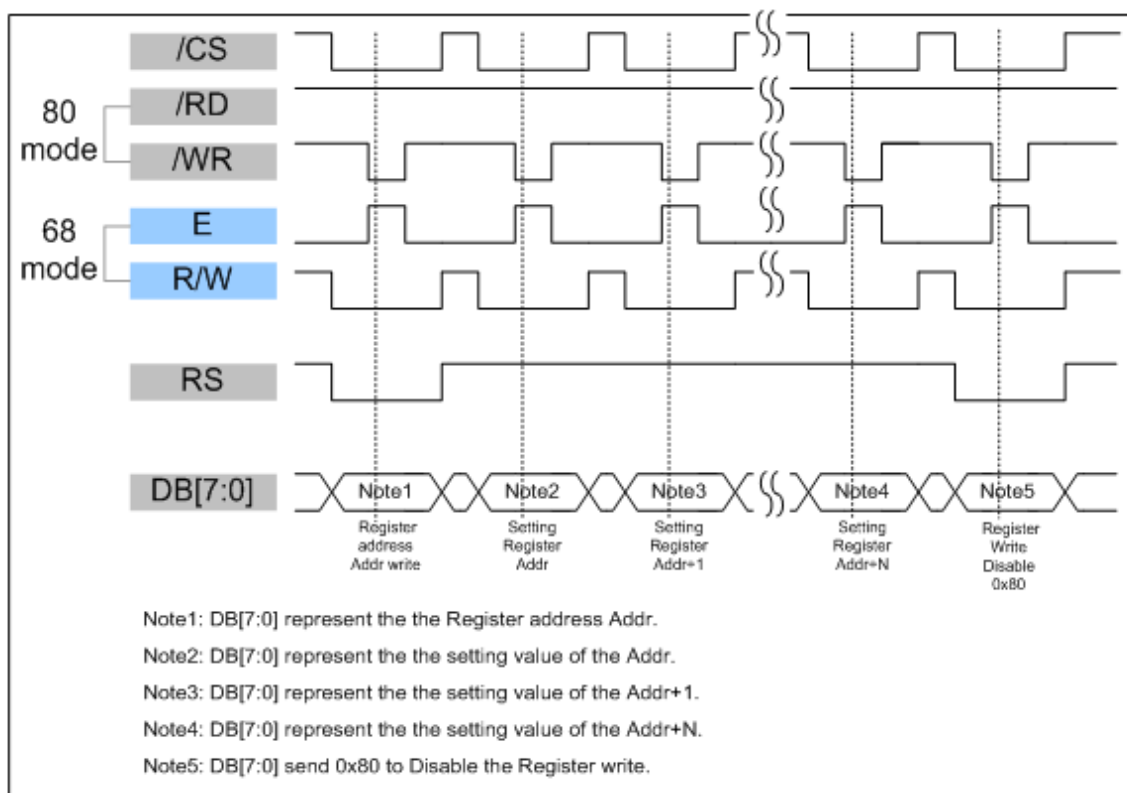
Pin no	Symbol	Level	Description	Remark
1	A	P	LED Anode	
2	NC	-	No connection	
3	K	P	LED Cathode	

7 BLOCK DIAGRAM

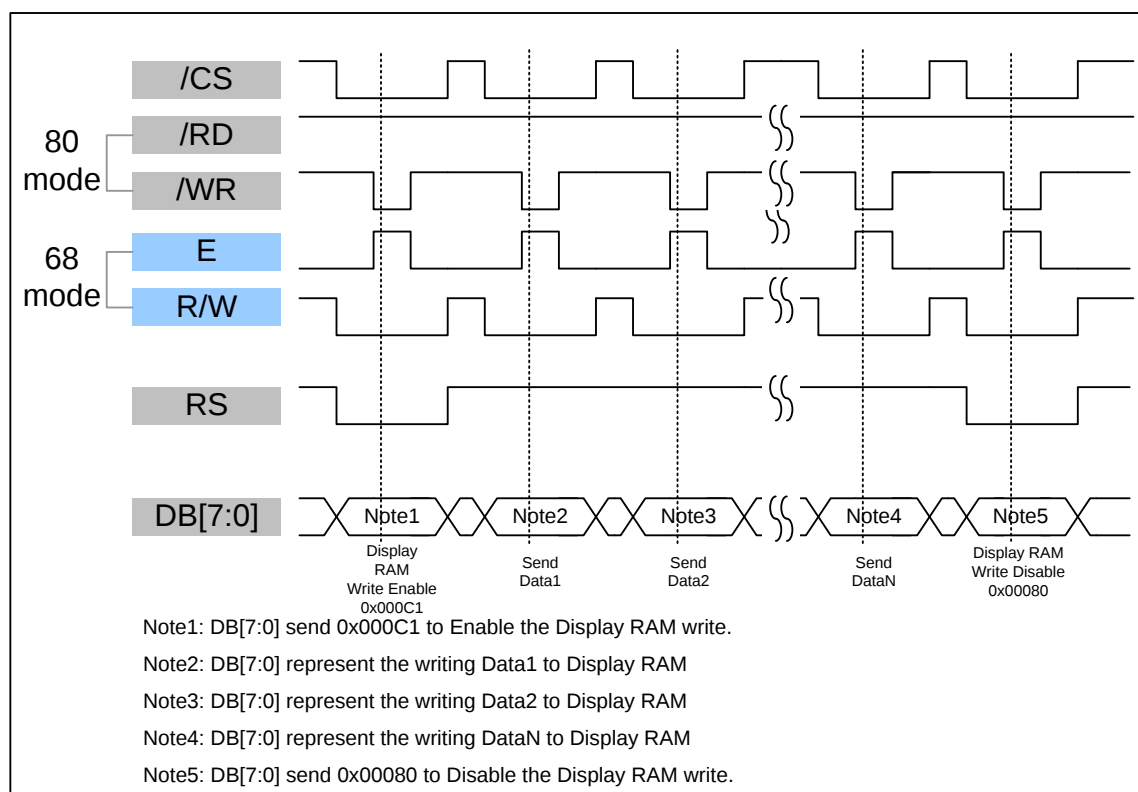


8 Interface Protocol

8.1 8Bit-80/68- Write to Command Register



8Bit-80/68-Write to Display RAM



8.2 Data transfer order Setting

8.2.A 8 bit interface 65K color (JP21,2 short 65K/262K =Low)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1 st data	X	X	X	X	X	X	X	X	R4	R3	R2	R1	R0	G5	G4	G3
2 nd data	X	X	X	X	X	X	X	X	G2	G1	G0	B4	B3	B2	B1	B0

8.2.B 8 bit interface 262K color (Pin2 2,3 short 65K/262K =High)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1 st data	X	X	X	X	X	X	X	X							R5	R4
2 nd data	X	X	X	X	X	X	X	X	R3	R2	R1	R0	G5	G4	G3	G2
3 rd data	X	X	X	X	X	X	X	X	G1	G0	B5	B4	B3	B2	B1	B0

9 Register Depiction

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
00	00	MSB of X-axis start position								
Description	set the horizontals start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
01	00	LSB of X-axis start position								
Description	set the horizontals start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
02	01	MSB of X-axis end position								
Description	set the horizontals end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
03	3F	LSB of X-axis end position								
Description	set the horizontals end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
04	00	MSB of Y-axis start position								
Description	set the vertical start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
05	00	LSB of Y-axis start position								
Description	Set the vertical start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
06	00	MSB of Y-axis end position								
Description	set the vertical end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
07	EF	LSB of Y-axis end position								
Description	Set the vertical end position of display active region									

To simplify the address control of display RAM access, the window area address function

allows for writing data only within a window area of display RAM specified by registers REG[00]~REG[07] .

After writing data to the display RAM, the Address counter will be increased within setting window address-range which is specified by

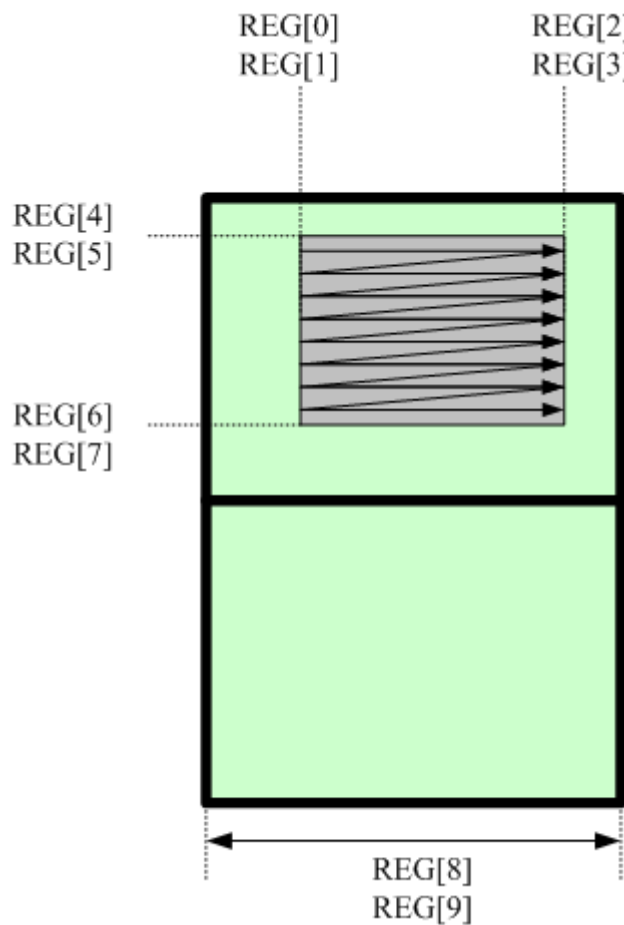
MIN X address (REG[0] & REG[1])

MAX X address (REG[2] & REG[3])

MIN Y address (REG[4] & REG[5])

MAX Y address (REG[6] & REG[7])

Therefore, data can be written consecutively without thinking the data address.



Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
08	01	X	X	X	X	X	X	_PanelXSize H_Byte[1:0]		
Description	Set the panel X size									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
09	40	_PanelXSize L_Byte[7:0]								
Description	Set the panel X size									

The register REG[08] and REG[09] is use to calculate the RAM address. If you want to use the TFT as Landscape mode (320x240), the REG[08] & RGE[09] must set to 320. If you want to use the TFT as Portrait mode (240x320), the REG[08] & RGE[09] must set to 240.

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0A	00	X	X	X	X	X	[17:16] bits of memory write start address			
Description	Memory write start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0B	00	[15:8] bits of memory write start address								
Description	Memory write start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0C	00	[7:0] bits of memory write start address								
Description	Memory write start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x10	0x0D	Bit_SWAP	OUT_TEST	BUS_SEL		Blanking	P/S_SEL	CLK_SEL		
Description	"0x10_Clk_sel[1:0]" : The TFT controller built-in 40Mhz PLL clock. These bits are for select the TFT panel dot clock frequency. 00 : 20Mhz 01: 10Mhz 02: 5 Mhz									
	"0x10_ps_sel[2]" : The TFT controller support parallel and serial RGB interface. These bits are for select the output timing. 0 : serial Panel 1: Parallel panel									
	"0x10_blanking_tmp[3]" 0 : OFF (blanking) 1: ON (normal operation)									
	"0x10_bus_sel[5:4]" : It only for serial Panel 00=R , 01=G , 10=B									
	"0x10_out_test[6]" : Self test 0 : normal operation 1: for test (don't use for normal operation) When set the bit to "1" , the Rout=(Reg 2a[6:0]) Gout=(Reg 2b[6:0]) Bout=(Reg 2c[6:0])									
	"0x10_bit_swap[7]" : 0-normal									
	The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x11	00	X	X	EVEN			_ODD			
Description	" Even line of serial panel data out sequence or data bus order of parallel panel 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR Others: reserved									
	Odd line of serial panel data out sequence 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR Others: reserved Must Set to 0x05 for AM320240N1									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x12	00					Hsync_stH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x13	00	Hsync_stL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x14	00					Hsync_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x15	10	Hsync_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x16	00					Hact_stH_Byte[3:0]				
Description	For TFT output timing adjust: DE pulse start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x17	38	Hact_stL_Byte[7:0]								
Description	For TFT output timing adjust: DE pulse start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x18	01					Hact_pwH_Byte[3:0]				
Description	For TFT output timing adjust: DE pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x19	40	Hact_pwL_Byte[7:0]								
Description	For TFT output timing adjust: DE pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1A	01					HtotalH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync total clocks H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1B	B8	HtotalL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync total clocks H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1C	00					Vsync_stH_Byte[3:0]				
Description	For TFT output timing adjust: Vsync start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1D	00	Vsync_stL_Byte[7:0]								
Description	For TFT output timing adjust: Vsync start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1E	00					Vsync_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Vsync pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1F	08	Vsync_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Vsync pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x20	00					Vact_stH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical DE pulse start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x21	12	Vact_stL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical DE pulse start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x22	00					Vact_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical Active width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x23	F0	Vact_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical Active width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x24	01					VtotalH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical total width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x25	09	VtotalL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical total width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
26	00	X	X	X	X	X	[17:16] bits of memory read start address			
Description	Memory read start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
27	00	[15:8] bits of memory write start address								
Description	Memory read start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
28	00	[7:0] bits of memory write start address								
Description	Memory read start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
29	00	[7:1] Reversed								
Description	[0] Load output timing related setting (H sync., V sync. and DE) to take effect									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2A	00	X	TestPatternRout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Rout data equal to TestPatternRout[6:0]									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2B	00	X	TestPatternGout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Gout data equal to TestPatternGout[6:0]									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2C	00	X	TestPatternBout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Bout data equal to TestPatternBout[6:0]									

If you set the " REG[0x10]_out_test[6]" : Self test =1 , the TFT controller will skip the connect of the display RAM. The Output port will send the REG[2A] ,REG[2B],REG[2C] data.

REG[2A]=0x3F
REG[2B]=0x00
REG[2C]=0x00

REG[2A]=0x00
REG[2B]=0x3F
REG[2C]=0x00

REG[2A]=0x00
REG[2B]=0x00
REG[2C]=0x3F

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2D	00	X	X	X	X	[3]	Rising/falling edge[2]	_rotate [1:0]		
Description	[3] Output pin X_DCON level control ; TFT Power ON/OFF control 0: TFT POWER circuit OFF 1: TFT POWER circuit ON									
	Rising/falling edge[2] : 0: The RGB out put data are on the Rising edge of the DCLK. 1: The RGB out put data are on the Falling edge of the DCLK.									
	_rotate [1:0]: 00 : rotate 0 degree 01 : rotate90 degree 10 : rotate 270 degree 11 : rotate 180 degree									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark	
30	00	X	X	X	X	X	_H byte H-Offset[3:0]				
Description	Set the Horizontal offset										
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark	
31	00	_L byte H-Offset[7:0]									
Description	Set the Horizontal offset										
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark	
32	00	X	X	X	X	X	_H byte V-Offset[3:0]				
Description	Set the Vertical offset										
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark	
33	00	_L byte V-Offset[7:0]									
Description	Set the Vertical offset										

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
34	00	[7:4] Reserved					_H byte H-def[3:0]			
Description	[3:0] MSB of image horizontal physical resolution in memory									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
35	40	_L byte H-def[7:0]								
Description	[7:0] LSB of image horizontal physical resolution in memory									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
36	01	[7:4] Reserved					_H byte V-def[3:0]			
Description	[3:0] MSB of image vertical physical resolution in memory									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
37	E0	_L byte V-def[7:0]								
Description	[7:0] LSB of image vertical physical resolution in memory									

The total RAM size is 640x240x18bit. The user can arrange the Horizontal ram size by REG[34],REG[35] and the Vertical ram size by REG[36],REG[37].

EX: 320x480x18bit REG[34]=0x01 , REG[35]=0x40 , REG[36]=0x01 , REG[37]=0xE0

EX: 640x240x18bit. REG[34]=0x02 , REG[35]=0x80 , REG[36]=0x00 , REG[37]=0xF0

10 Application Note:

```
void main(void)
```

```
{
    Initial_AMP506 ( );
    Full_386SCR(0xf800);
    Full_386SCR(0x07e0);
    Full_386SCR(0x001f);
}
```

```
void AMP506_80Mode_Command_SendAddress(BYTE Addr)
```

```
{
    SET_nRD;           // /RD=1
    CLR_RS;            // RS=0
    CLR_CS1;           // /CS=0
    CLR_nWRL;          // /WR=0
    DB16OUT(Addr);     // Data Bus OUT
    SET_nWRL;          // /WR=1
    SET_RS;            // RS=1
    SET_CS1;           // CS=1
}
```

```
void AMP506_80Mode_Command_SendData(BYTE Data)
```

```
{
    SET_nRD;
    SET_RS;
    CLR_CS1;
    CLR_nWRL;
    DB16OUT(Data);
    SET_nWRL;
    SET_RS;
    SET_CS1;
}
```

```
void AMP506_Command_Write(uint8 CMD_Address,uint8 CMD_Value)
```

```
{
    AMP506_80Mode_Command_SendAddress(CMD_Address);
    AMP506_80Mode_Command_SendData(CMD_Value);
}
```

```

void AMP506_80Mode_16Bit_Memory_SendData(uint16 Dat16bit)
{
    SET_nRD;
    SET_RS;
    CLR_CS1;
    CLR_nWRL;
    DB16OUT(Dat16bit>>8);
    SET_nWRL;           // Low to High Latch Data to AMP506 Buffer
    SET_CS1;

    SET_nRD;
    SET_RS;
    CLR_CS1;
    CLR_nWRL;
    DB16OUT(Dat16bit);
    SET_nWRL;           // Low to High Latch Data to AMP506 Buffer
    SET_CS1;

}

void Initial_AMP506(void)
{
    AMP506_Command_Write(0x40,0x12); /*[7:6] Reserved
                                     [5] PLL control pins to select out frequency range
                                     0: 20MHz ~ 100MHz 1: 100MHz ~ 300MHz
                                     [4] Reserved [3] Reserved
                                     [2:1] Output Driving Capability
                                     00: 4mA 01: 8mA 10: 12mA 11: 16mA
                                     [0] Output slew rate
                                     0: Fast 1: Slow
                                     */

    AMP506_Command_Write(0x41,0x01); //Set PLL=40Mhz * (0x42) / (0x41)
    AMP506_Command_Write(0x42,0x01); //0x41 [7:6] Reserved [5:0] PLL Programmable
                                     pre-divider, 6bit(1~63)
                                     //0x42 [7:6] Reserved [5:0] PLL Programmable loop
                                     divider, 6bit(1~63)

    AMP506_Command_Write(0x00,0x00); // MSB of horizontal start coordinate value
    AMP506_Command_Write(0x01,0x00); // LSB of horizontal start coordinate value

```

```

AMP506_Command_Write(0x02,0x01);    // MSB of horizontal end coordinate value
AMP506_Command_Write(0x03,0x3F);    // LSB of horizontal end coordinate value

AMP506_Command_Write(0x04,0x00);    // MSB of vertical start coordinate value
AMP506_Command_Write(0x05,0x00);    // LSB of vertical start coordinate value
AMP506_Command_Write(0x06,0x01);    // MSB of vertical end coordinate value
AMP506_Command_Write(0x07,0x3F);    // LSB of vertical end coordinate value


AMP506_Command_Write(0x08,0x01);    // MSB of input image horizontal resolution
AMP506_Command_Write(0x09,0x40);    // LSB of input image horizontal resolution
AMP506_Command_Write(0x0a,0x00);    //[17:16] bits of memory write start address
AMP506_Command_Write(0x0b,0x00);    //[15:8] bits of memory write start address
AMP506_Command_Write(0x0c,0x00);    //[7:0] bits of memory write start address


AMP506_Command_Write(0x10,0x0D);    /*[7] Output data bits swap      0: Normal 1:Swap
                                     [6] Output test mode enable 0: disable 1: enable
                                     [5:4] Serial mode data out bus selection
                                     00: X_ODATA17 ~ X_ODATA12 active , others are set to
zero
                                     01: X_ODATA11 ~ X_ODATA06 active , others are set to
zero
                                     10: X_ODATA05 ~ X_ODATA00 active , others are set to
zero
                                     11: reserved
                                     [3] Output data blanking
                                     0: set output data to 0    1: Normal display
                                     [2] Parallel or serial mode selection
                                     0: serial data out        1: parallel data output
                                     [1:0] Output clock selection
                                     00: system clock divided by 2
                                     01: system clock divided by 4
                                     10: system clock divided by 8
                                     11: reserved */

AMP506_Command_Write(0x11,0x05);
/*[7] Reserved
[6:4] Even line of serial panel data out sequence or data bus order of parallel panel
000: RGB   001: RBG   010: GRB   011: GBR   100: BRG   101: BGR   Others:
reserved
[3] Reversed
[2:0] Odd line of serial panel data out sequence
000: RGB   001: RBG   010: GRB   011: GBR   100: BRG   101: BGR   Others:

```

```

reserved */
AMP506_Command_Write(0x12,0x00); // [3:0] MSB of output H sync. pulse start
position
AMP506_Command_Write(0x13,0x00); //[7:0] LSB of output H sync. pulse start position
AMP506_Command_Write(0x14,0x00); // [3:0] MSB of output H sync. pulse width

AMP506_Command_Write(0x15,0x10);      //[7:0] LSB of output H sync. pulse width
AMP506_Command_Write(0x16,0x00);      //[3:0] MSB of output DE horizontal start
position
AMP506_Command_Write(0x17,0x38);      //[7:0] LSB of output DE horizontal start
position

AMP506_Command_Write(0x18,0x01); // [3:0] MSB of output DE horizontal active region in
pixel
AMP506_Command_Write(0x19,0x40);      //[7:0] LSB of output DE horizontal active region
in pixel
AMP506_Command_Write(0x1a,0x01);      //[7:4] Reserved [3:0] MSB of output H total in
pixel
AMP506_Command_Write(0x1b,0xb8);      //[7:0] LSB of output H total in pixel
AMP506_Command_Write(0x1c,0x00);      //[3:0] MSB of output V sync. pulse start
position
AMP506_Command_Write(0x1d,0x00);      //[7:0] of output V sync. pulse start position
AMP506_Command_Write(0x1e,0x00);      //[7:4] Reserved [3:0] MSB of output V sync.
pulse width
AMP506_Command_Write(0x1f,0x08);      //[7:0] LSB of output V sync. pulse width
AMP506_Command_Write(0x20,0x00);      // [3:0] MSB of output DE vertical start position
AMP506_Command_Write(0x21,0x12);      //[7:0] LSB of output DE vertical start position
AMP506_Command_Write(0x22,0x00);      // [3:0] MSB of output DE vertical active region
in line
AMP506_Command_Write(0x23,0xf0);      //[7:0] LSB of output DE vertical active region
in line
AMP506_Command_Write(0x24,0x01);      //[7:4] Reversed [3:0] MSB of output V total in
line
AMP506_Command_Write(0x25,0x09);      //[7:0] LSB of output V total in line
AMP506_Command_Write(0x26,0x00);      // [17:16] bits of memory read start address
AMP506_Command_Write(0x27,0x00);      //[7:0] [15:8] bits of memory read start address
AMP506_Command_Write(0x28,0x00);      //[7:0] [7:0] bits of memory read start address
AMP506_Command_Write(0x29,0x01);
//[7:1] Reversed [0] Load output timing related setting (H sync., V sync. and DE) to take effect
AMP506_Command_Write(0x2d,0x08); /* [7:4] Reserved

```

```

        [3] Output pin X_DCON level control
        [2] Output clock inversion      0: Normal 1: Inverse
        [1:0] Image rotate
            00: 0°  01: 90°  10: 270° 11: 180°
    */
    AMP506_Command_Write(0x30,0x00); // [7:4] Reserved [3:0] MSB of image horizontal shift
value
    AMP506_Command_Write(0x31,0x00); // [7:0] LSB of image horizontal shift value
    AMP506_Command_Write(0x32,0x00); // [7:4] Reserved [3:0] MSB of image vertical shift
value
    AMP506_Command_Write(0x33,0x00); // [7:0] LSB of image vertical shift value
    AMP506_Command_Write(0x34,0x01);
    // [3:0] MSB of image horizontal physical Resolution in memory
    AMP506_Command_Write(0x35,0x40);
    // [7:0] LSB of image horizontal physical resolution in memory

    AMP506_Command_Write(0x36,0x01);
    // [7:4] Reserved [3:0] MSB of image vertical physical resolution in memory
    AMP506_Command_Write(0x37,0xe0);
    // [7:0] LSB of image vertical physical resolution in memory
}

void AMP506_WindowSet(uint16 S_X,uint16 S_Y,uint16 E_X,uint16 E_Y)
{
    AMP506_80Mode_Command_SendAddress(0x00);
    AMP506_80Mode_Command_SendData((S_X)>>8);
    AMP506_80Mode_Command_SendData(S_X);
    AMP506_80Mode_Command_SendData((E_X-1)>>8);
    AMP506_80Mode_Command_SendData(E_X-1);
    AMP506_80Mode_Command_SendData(S_Y>>8);
    AMP506_80Mode_Command_SendData(S_Y);
    AMP506_80Mode_Command_SendData((E_Y-1)>>8);
    AMP506_80Mode_Command_SendData(E_Y-1);
}

void Full_386SCR(uint16 Dat16bit)
{
    int32 k,l;
    AMP506_WindowSet(0,0,Resolution_X,Resolution_Y);

```

```

AMP506_80Mode_Command_SendAddress(0xc1);  // _DisplayRAM_WriteEnable_
for(k=0;k<240*2;k++)
{
    for(l=0;l<320;l++)
    {
        AMP506_80Mode_16Bit_Memory_SendData(Dat16bit);
    }
}
AMP506_80Mode_Command_SendAddress(0x80);  // DisplayRAM_WriteDisable _
}

```

The TFT LCD controller default value is for AM320240N1 already. So we can start to write our data in a few steps:

Target: To write a 640x240 data to Display RAM and scroll the display data by change the Horizontal offset register.

10.1 Step 1: Make sure the interface Protocol.

10.2 Step 2: Define the Horizontal ram seize = 640 and Vertical ram size =240 640x240x18bit. REG[34]=0x02 , REG[35]=0x80 , REG[36]=0x00 ,

REG[37]=0xF0

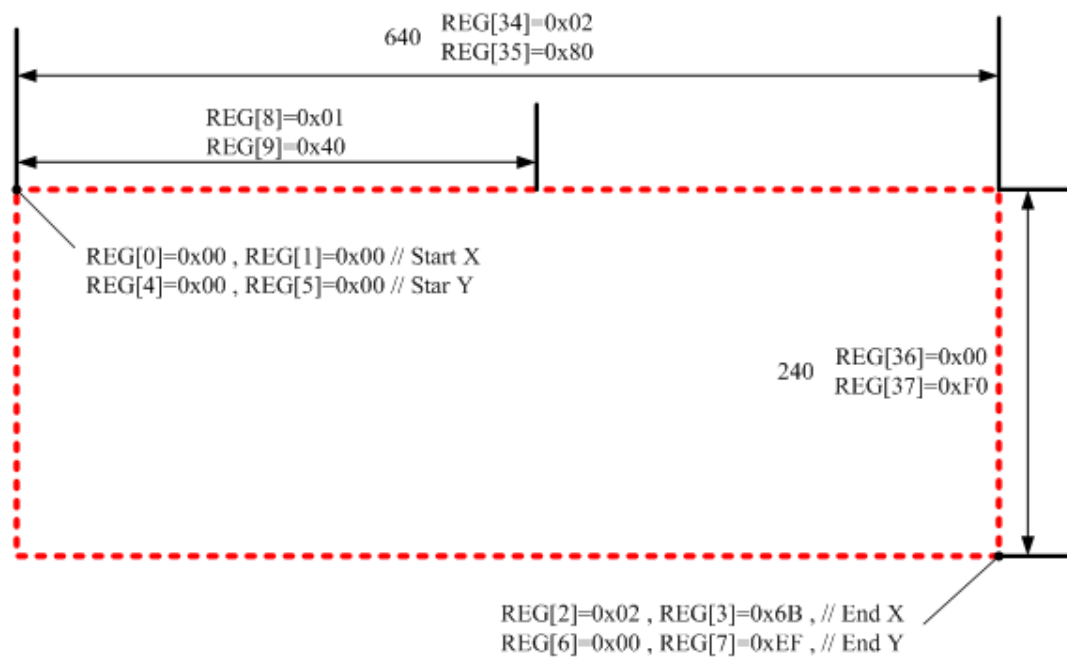
10.3 Step 3: Define the Panel X Size = 320

REG[8]=0x01 , REG[9]=0x40

10.4 Step4: Define the Write window. Start=(0,0) End=(619,239)

REG[0]=0x00 , REG[1]=0x00 , REG[2]=0x02 , REG[3]=0x6B , // Start X , End X

REG[4]=0x00 , REG[5]=0x00 , REG[6]=0x00 , REG[7]=0xEF , // Star Y ,End Y



10.5 Step5: Write the 640x240x18 bit data consecutively



10.6 Step6: The display will show the following image.



10.7 Step7: Change the Horizontal offset to switch or scroll the display data.

Set the Horizontal offset = 160 , REG[30]=00 REG[31]=A0 . You will see



10.8 Step8: Change the Horizontal offset to switch or scroll the display data.

Set the Horizontal offset = 320 , REG[30]=01 REG[31]=40 . You will see



DISPLAYED COLOR AND INPUT DATA

		Color & Gray Scale	DATA SIGNAL																	
			R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(61)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(31)	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(1)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(61)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(31)	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(1)	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(31)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	

11 Reliability test items

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=240 hrs	
Low Temperature Operation	-20±3°C , t=240 hrs	
High Temperature Storage	80±3°C , t=240 hrs	1,2
Low Temperature Storage	-30±3°C , t=240 hrs	1,2
Storage at High Temperature and Humidity	60°C, 90% RH , 240 hrs	1,2
Thermal Shock Test	-20°C (30min) ~ 70°C (30min) 100 cycles	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Note 3 : The module shouldn't be tested more than one condition, and all the test conditions are independent.

Note 4 : All the reliability tests should be done without protective film on the module.

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

12 USE PRECAUTIONS

12.1 Handling precautions

- 1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
- 2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
- 3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
- 4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

12.2 Installing precautions

- 1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. $1\text{M}\Omega$ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
- 2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
- 3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
- 4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

12.3 Storage precautions

- 1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
- 2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
- 3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

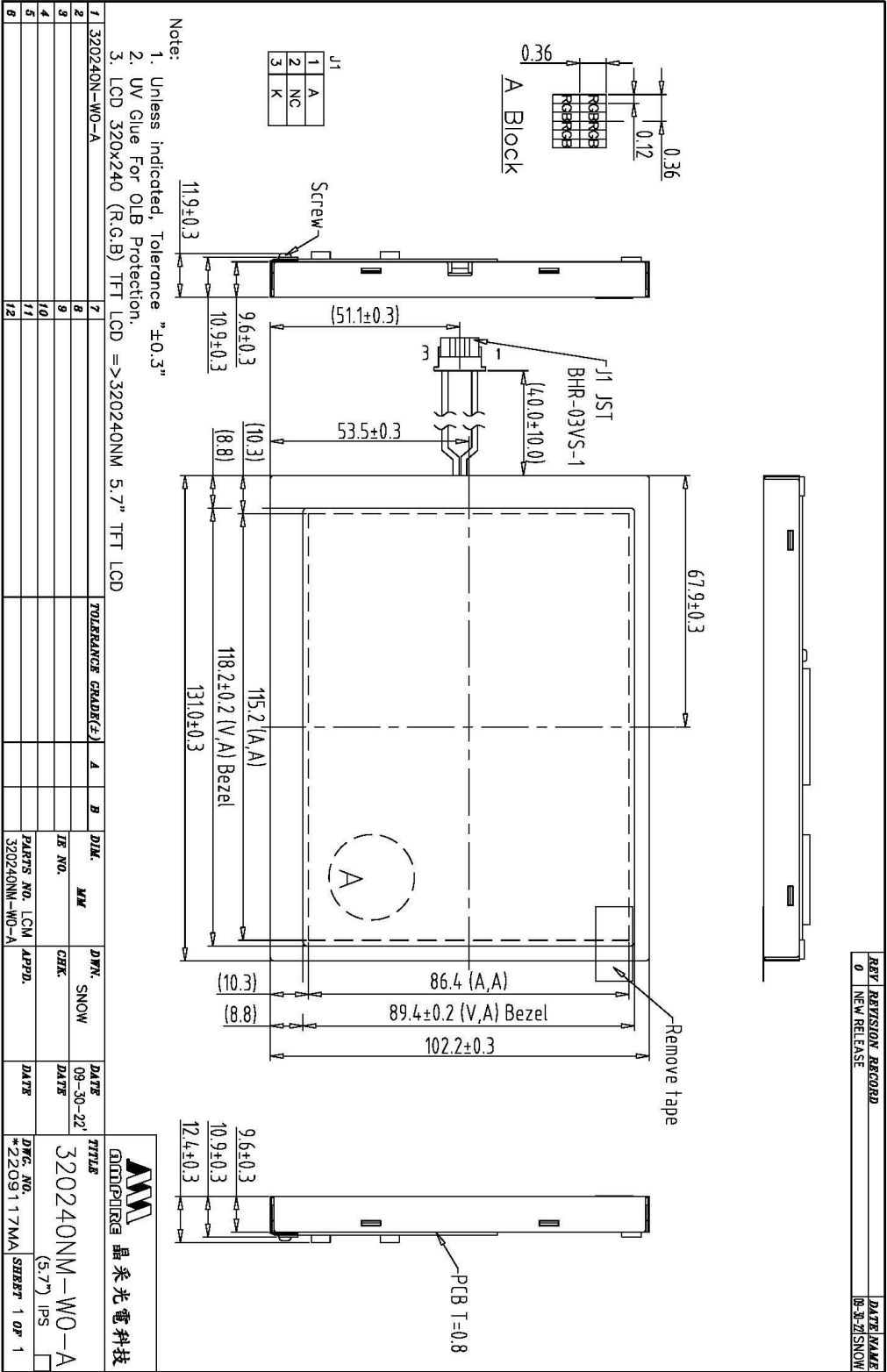
12.4 Operating precautions

- 1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
- 2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
- 3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC drive voltage.
- 4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
- 5) Make certain that each signal noise level is within the standard (L level: $0.2V_{dd}$ or less and H level: $0.8V_{dd}$ or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
- 6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
- 7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
- 8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

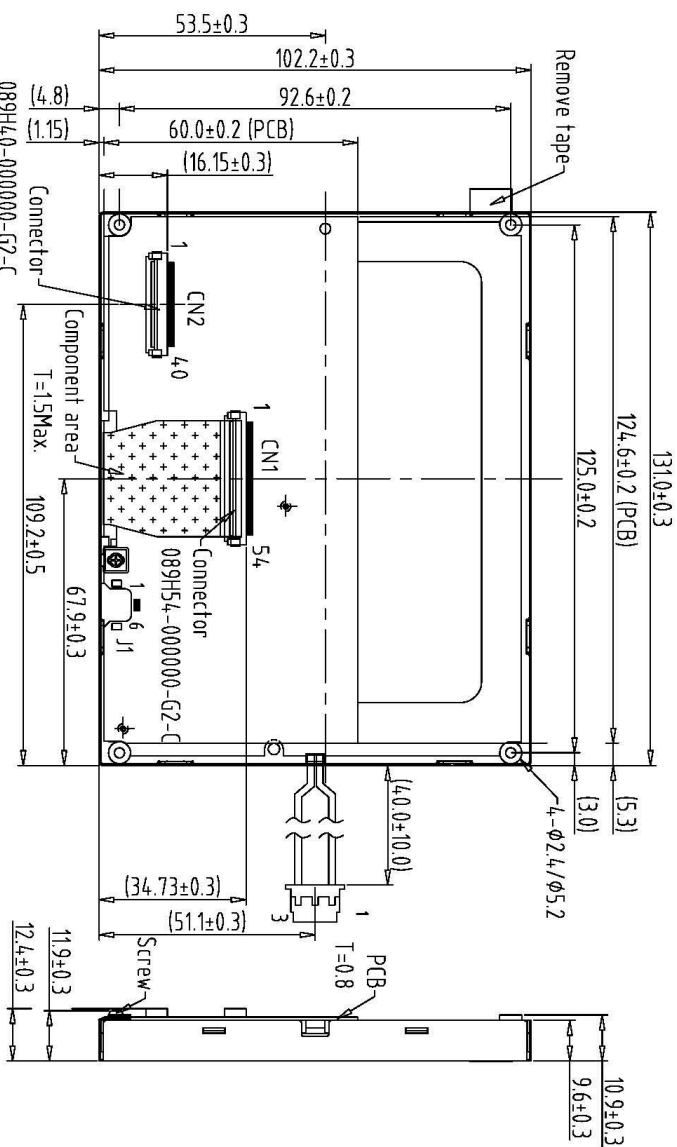
12.5 Other

- 1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
- 2) Do not keep the LCD at the same display pattern continually. The residual image will happen and it will damage the LCD. Please use screen saver.
- 3) AMIPRE will provide one year warranty for all products and three months warrantee for all repairing products.

13 OUTLINE DIMENSION



REV	REVISION RECORD	DATE	NAME
0	NEW RELEASE	09-30-21	SNOWM



CN2	2/1	DB11
1	DOGD	
2	DOGD	22 DB12
3	NC	23 DB13
4	NC	24 DB14
5	/RSEI	25 DB15
6	RS	26 DB16
7	/CS	27 DB17
8	/MR	28 65K/262K
9	/RD	29 DOGD
10	DB0	30 NC
11	DB1	31 NC
12	DB2	32 NC
13	DB3	33 NC
14	DB4	34 NC
15	DB5	35 YD
16	DB6	36 YD
17	DB7	37 YD
18	DB8	38 DOGD
19	DB9	39 DOGD
20	DB10	40 DOGD

Note: u07t4v-u00vvvv-u2-l

1. Unless indicated, Tolerance $\pm 0.3"$
2. UV Glue For OLB Protection.
3. Main LCD 320x240 (R.G.B) TFT LCD =>320240NM 5.7" TFT LCD

Back view

<i>I</i>	<i>J</i>	TOLERANCE GRADE(?)	A	B	DIM.	M/M	DIV.	SNOW	DATE	TITLE
1	320240N-WO-A								09-30-22	320240NM-WO-A
2		8							DATE	(5.7") IPS
3		9			IR NO.		CHEK.		DATE	
4		10								PARTS NO. ION-1 APPD.
5		11							DATE	DWG. NO.
6		12			320240NM-WO-A					*220911BMA SECRET 1 OF 1

14 Package

[illegible]