晶采光電科技股份有限公司
AMPIRE CO., LTD.

Specifications for LCD module

Customer	
Customer part no.	
Ampire part no.	**AM-8001280GTZQW-00H**
Approved by	
Date	

☐ **Preliminary Specification**
☑ **Formal Specification**

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Patrick	Simon	Jessica

This Specification is subject to change without notice.

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2022/08/31	--	New Release	Jessica

1 General Descriptions

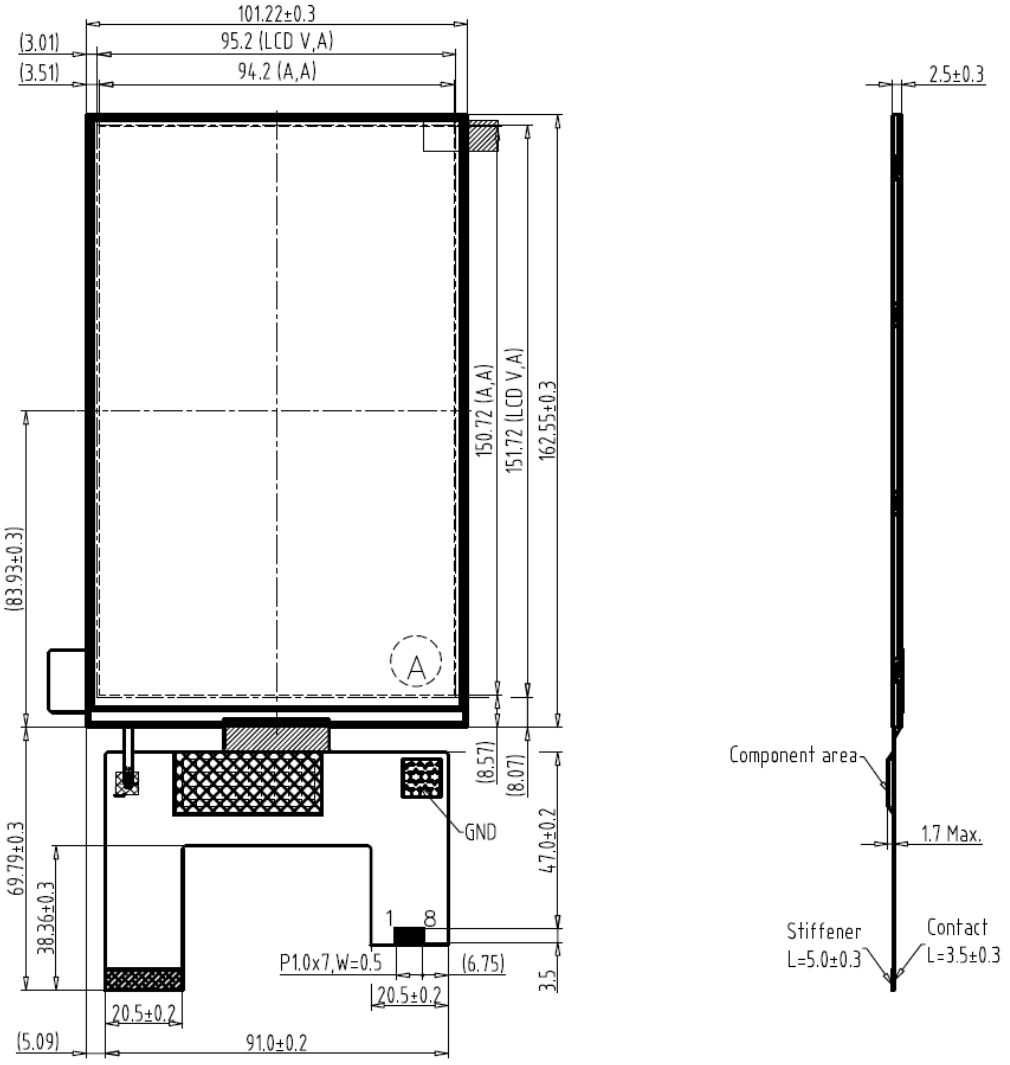
7 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module. This module is composed of a 7” TFT-LCD panel and backlight unit.

1.1 Features

(1) 7 inch configuration
(2) 4-wire mipi interface
(3) Driver IC : ILI9881C

1.2 Product Summary

Item	Specification	Remark
LCD Size	7.0 inch (Diagonal)	
Resolution	800 x 3 (RGB) x 1280	
Display Mode	Normally Black.	
Pixel pitch	0.11775 (W) x 0.11775(H) mm	
Interface	MIPI	
Color arrangement	RGB-stripe	
Luminance	**470**	cd/m2
Viewing Direction	All direction	



2 Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	3V3	-0.3	+3.6	V	-
IO Supply voltage	1V8	-0.3	+3.6	V	
Operating Temperature	TOP	-20	70	℃	Note 1
Storage Temperature	TST	-30	80	℃	Note 1

Note(1) The maximum rating is defined as above based on the chamber temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- ✧ Background color, contrast and response time would be different in temperatures other than 25℃.
- ✧ Operating under high temperature will decrease LED lifetime.

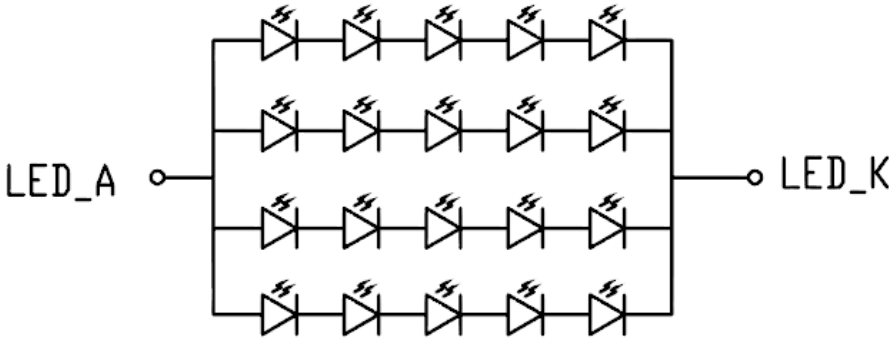
3 Electrical Characteristics

3.1 LCD Characteristics

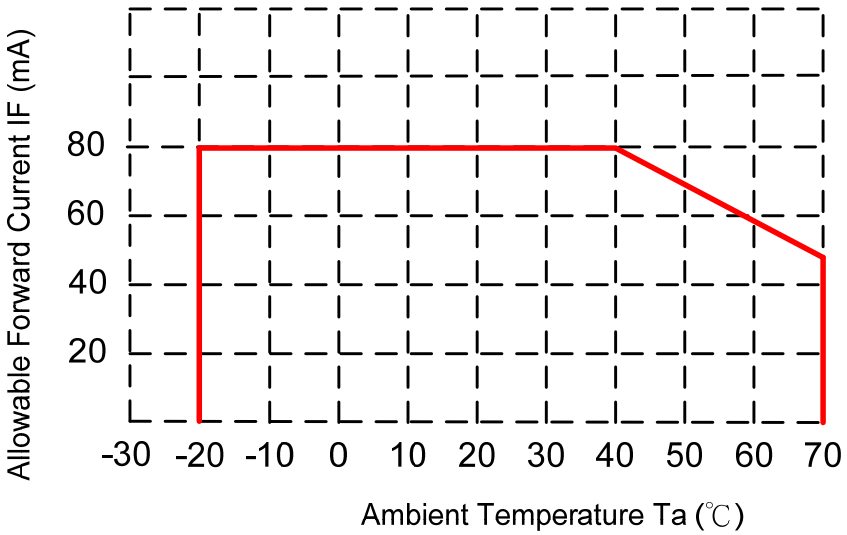
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	3V3	3.2	3.3	3.4	V	
IO Supply voltage	1V8	1.74	1.8	3.4	V	
Input Hi Logic Voltage	VIH	0.7*1V8	--	1V8	V	LCD_RESET
Input Low Logic Voltage	VIL	-0.3	--	0.3*1V8	V	LCD_RESET
Out Hi Logic Voltage	VOH	0.8*1V8	--	1V8	V	LCD_TE
Out Low Logic Voltage	VOL	-0.3	--	0.2*1V8	V	LCD_TE

3.2 Backlight Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED Forward Voltage	VF	--	15	--	V	IF=80mA, Ta=25℃
LED Forward Current	IF	--	80	--	mA	Ta=25℃
LED life time		30,000	50,000	-	Hr	IF=80mA, Ta=25℃



- ✧ The constant current source is needed for white LED back-light driving.
- ✧ Operating life means brightness goes down to 50% minimum brightness. LED life time is estimated data. Ta=25℃
- ✧ When LCM is operated over 40℃ ambient temperature, the IF should be follow :



4 AC Characteristics

DSI layer definitions

High Speed Mode – Clock Channel Timing

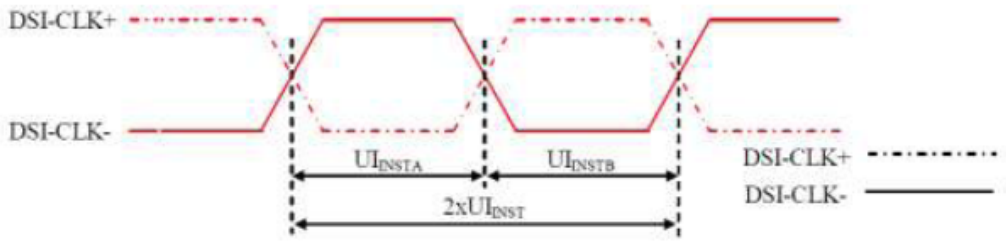


Figure 118 DSI Clock Channel Timing

Table 47 DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	2	5	ns
DSI-CLK+/-	UI_{INSTA},UI_{INSTB}	UI instantaneous Half	1	2.5	ns

Note: UI = UI_{INSTA} = UI_{INSTB}

High Speed Mode – Data Clock Channel Timing

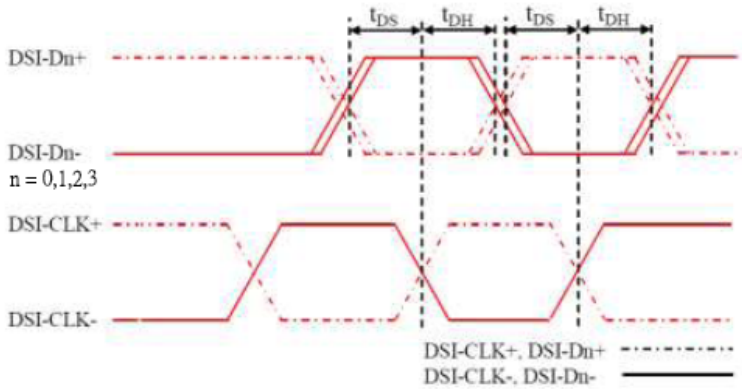


Figure 119 DSI Data to Clock Channel Timings

Table 48 DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0,1,2,3	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

High Speed Mode – Rise and Fall Timings

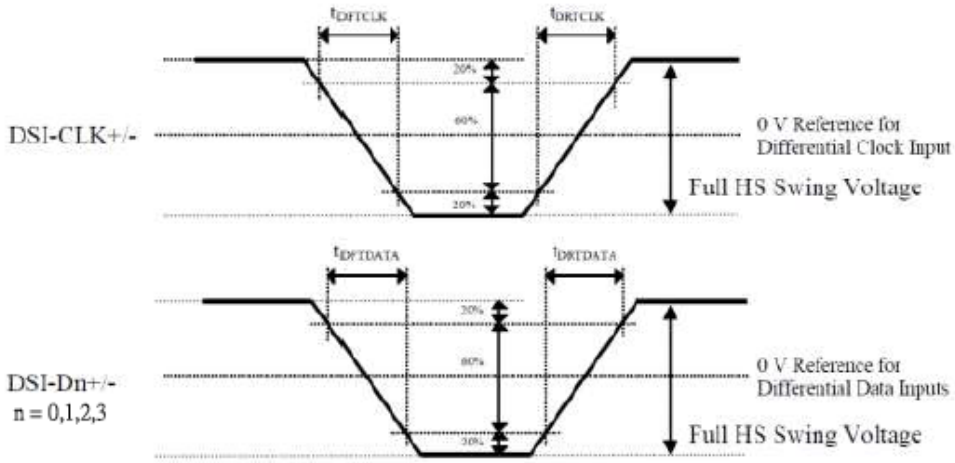


Figure 120 Rise and Fall Timings on Clock and Data Channels

Table 49 Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- n=0,1,2,3	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- n=0,1,2,3	150 ps	-	0.3UI (Note)

Note:

The display module has to meet timing requirements, what are defined for the transmitter(MPU) on MIPI D-Phy standard

Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (ILI7807D) sequence below.

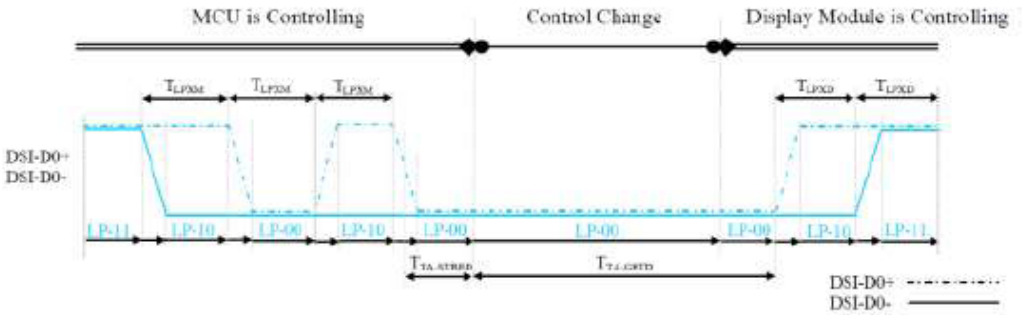


Figure 121 BTA from the MPU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module (ILI7807D) to the MPU sequence below.

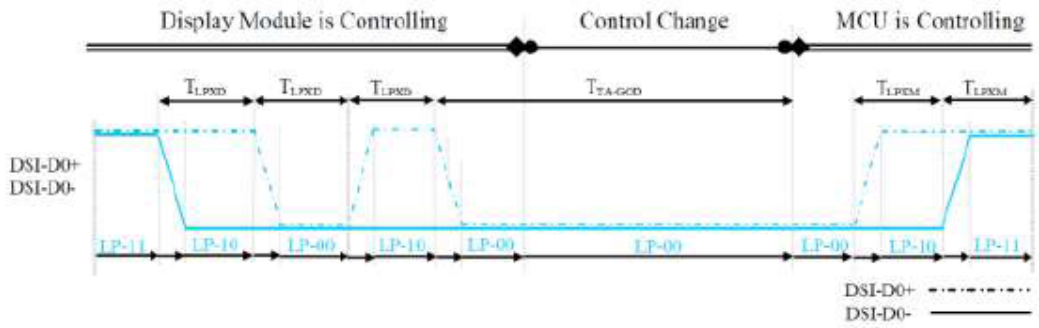


Figure 122 BTA from the Display Module to the MPU

Table 50 Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module (ILI7807D)	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI7807D) → MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (ILI7807D) starts driving	T_{LPXD}	$2\times T_{LPXD}$	ns

Table 51 Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI7807D)	$5\times T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MPU	$4\times T_{LPXD}$	ns

Data Lanes from Low Power Mode to High Speed Mode

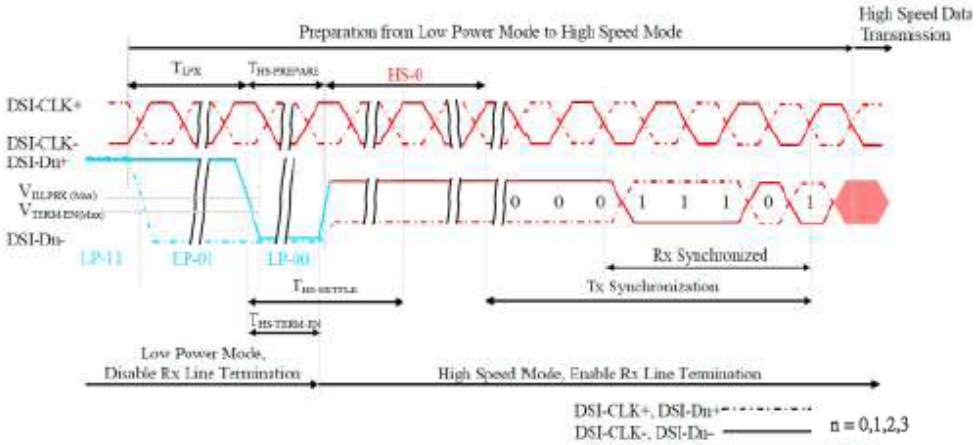


Figure 123 Data Lanes – Low Power Mode to High Speed Mode Timings

Table 52 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0,1,2,3	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0,1,2,3	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/-, n=0,1,2,3	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

Data Lanes from High Speed Mode to Low Power Mode

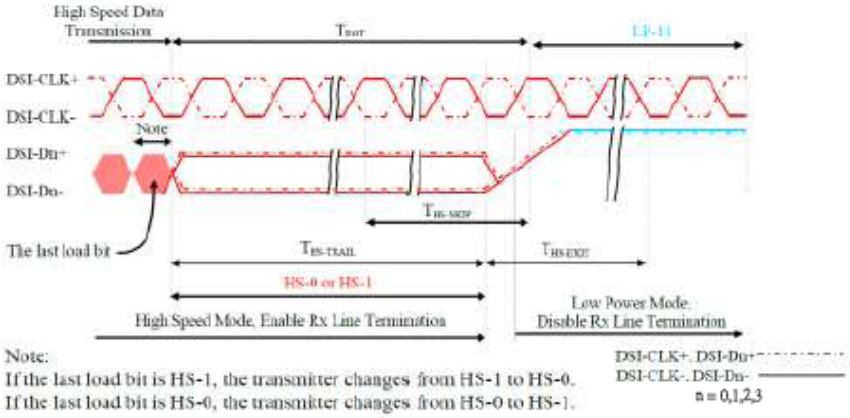


Figure 124 Data Lanes – High Speed Mode to Low Power Mode Timings

Table 53 Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0,1,2,3	$T_{HS-SKIP}$	Time-Out at Display Module (ILI7807D) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/-, n=0,1,2,3	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns
DSI-Dn+/-, n=0,1,2,3	$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(8*UI, 60ns+ 4*UI)	-	ns

DSI Clock Burst – High Speed Mode to/from Low Power Mode

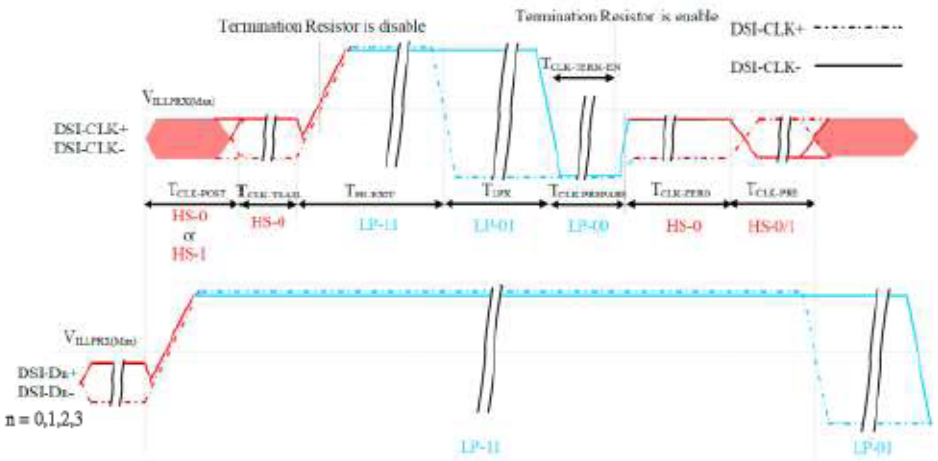
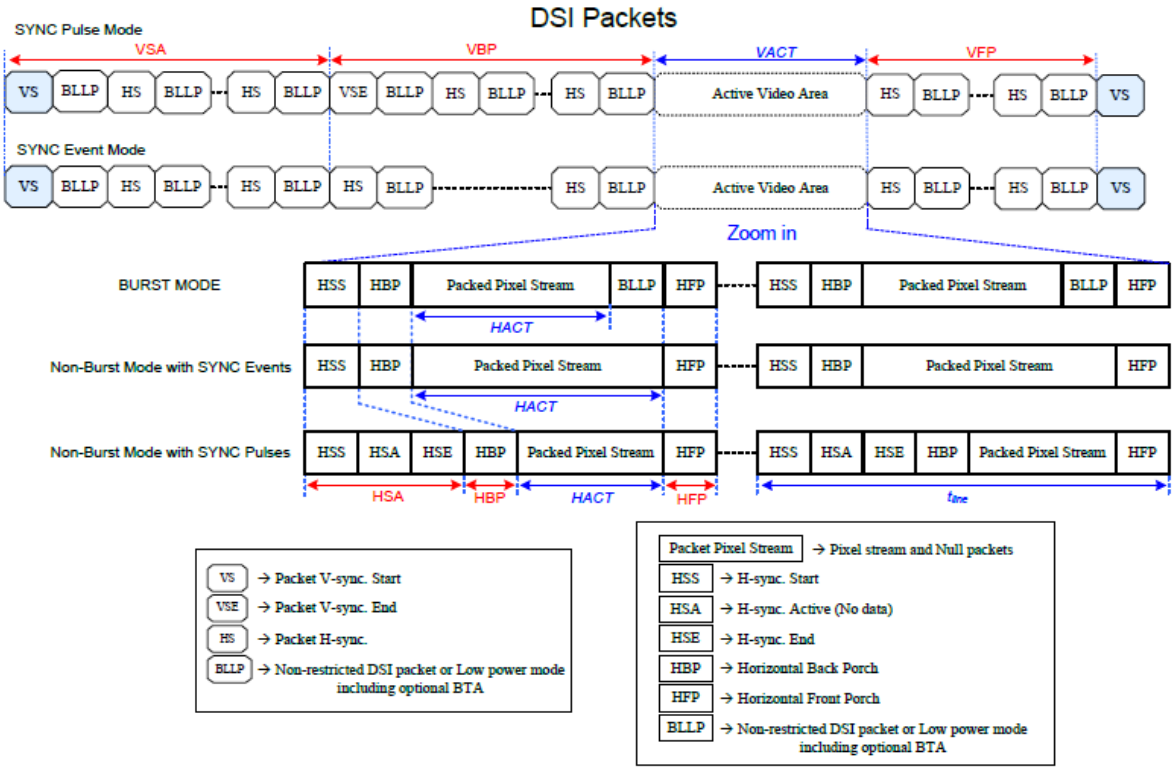


Figure 125 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 54 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

Timing for DSI video mode



5 Interface Timings

Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example : BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.

2. Pixel Format: Please reference to "DSI System Interface".

3. The formula exists slightly error because of the host-transmission way.

4. The best frame rate setting is from 50 to 60 Hz.

*5. Please reference to "*Table 55 Limited Clock Channel Speed*"*

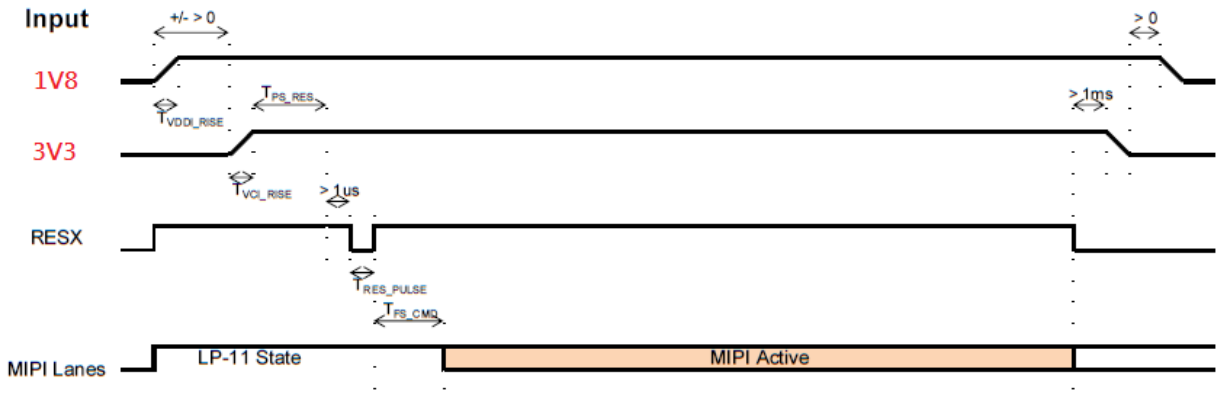
6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

Table 55 Limited Clock Channel Speed

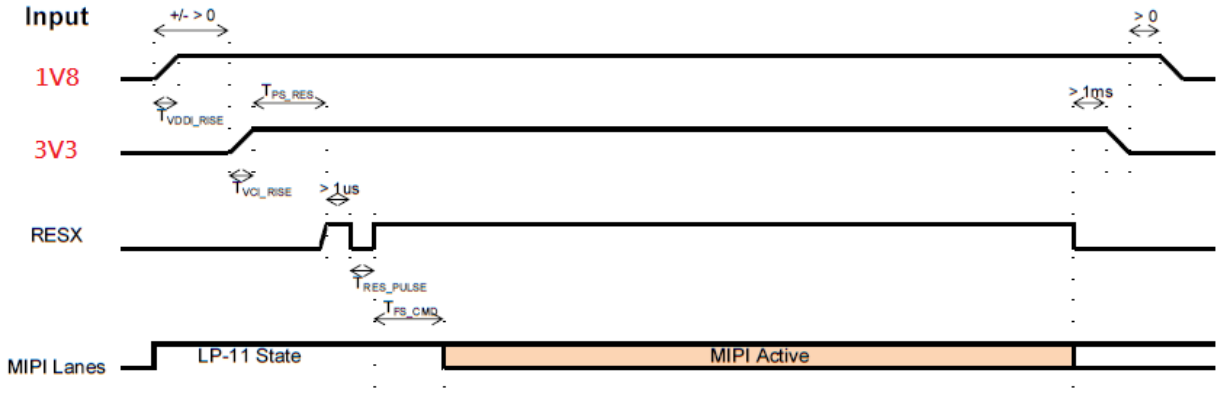
Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	1 Gbps	666 Mbps	666 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	1 Gbps	666 Mbps	666 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	1 Gbps	1 Gbps	1 Gbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	1 Gbps	1 Gbps	1 Gbps

6 Power ON/OFF Sequence

Case A:



Case B:



	Symbol	Characteristics	Min.	Typ.	Max.	Units
1V8	T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
3V3	T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
		Case B: VCI Rise time	40			
	T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
	T_{RES_PULSE}	Reset low pulse time	10	-	-	us
	T_{FS_CMD}	Reset to first command	10	-	-	ms

7 Timing

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Clock Frequency	fclk	40.8	51.2	67.2	MHz	Frame rate
Horizontal display area	thd		800		DCLK	
Horizontal Back Porch	HBP		20		DCLK	
Horizontal Pulse Width	HS		20		DCLK	
Horizontal Front Porch	HFP		32		DCLK	
HS Blanking	thb		72		DCLK	
HS period time	th		872		DCLK	
Vertical display area	tvd		1280		H	
Vertical Back Porch	VBP		6		H	
Vertical Pulse Width	VS		4		H	
Vertical Front Porch	HFP		8		H	
VS Blanking	thb		18		H	
VS period time	tv		1298		H	

8 Interface

Pin No.	Symbol	I/O	Description	Note
1	GND	P	Power Ground	
2	NC	-	No connection	
3	LED_A	P	Power for LED backlight anode	
4	LED_A	P	Power for LED backlight anode	
5	NC	-	No connection	
6	LED_K	P	Power for LED backlight negative	
7	LED_K	P	Power for LED backlight negative	
8	GND	P	Power Ground	
9	GND	P	Power Ground	
10	3V3	P	Power Supply voltage Analog	
11	3V3	P	Power Supply voltage Analog	
12	GND	P	Power Ground	
13	D3P	I	MIPI DSI differential data pair	
14	D3N	I	MIPI DSI differential data pair	
15	GND	P	Power Ground	
16	D2P	I	MIPI DSI differential data pair	
17	D2N	I	MIPI DSI differential data pair	
18	GND	P	Power Ground	
19	D1P	I	MIPI DSI differential data pair	
20	D1N	I	MIPI DSI differential data pair	
21	GND	P	Power Ground	
22	CLKP	I	MIPI DSI differential CLK pair	
23	CLKN	I	MIPI DSI differential CLK pair	
24	GND	P	Power Ground	
25	D0P	I	MIPI DSI differential data pair	
26	D0N	I	MIPI DSI differential data pair	

27	GND	P	Power Ground	
28	1V8	**P**	Power Supply voltage Digital	
29	1V8	**P**	Power Supply voltage Digital	
30	1V8	**P**	Power Supply voltage Digital	
31	LCD_TE	**O**	Tearing effect output pin. Leave the pin open when not in use.	
32	LCD_RESET	**I**	LCD reset signal, low active	
33	GND	P	Power Ground	
34	TOUCH_RESET	I	Touch reset signal, low active	
35	TOUCH_SCL	I	Touch IC I2C Bus serial clock	
36	TOUCH_SDA	I/O	Touch IC I2C Bus serial data	
37	TOUCH_VDD	P	Power Supply voltage touch IC	
38	TOUCH_VDD	P	Power Supply voltage touch IC	
39	TOUCH_INT#	O	Touch IC interrupt. Active Low.	
40	GND	P	Power Ground	

Note (1): Be sure to apply the power voltage as the power sequence spec.

9 Optical Specifications

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
View Angles		θT	CR≧10	70	85	-	Degree	Note(2)
		θB		70	85	-		
		θL		70	85	-		
		θR		70	85	-		
Contrast Ratio		CR	θ=0°	(700)	(1000)	-		Left/right 0° Top/bottom 5°
Response Time		TON+TOFF	25℃	-	25	35	ms	Note(1)(4)
Chromaticity	White	x		-0.05	(0.313)	+0.05		Note(1)(5)
		y			(0.329)			
	Red	x			T.B.D			
		y			T.B.D			
	Green	x			T.B.D			
		y			T.B.D			
	Blue	x			T.B.D			
		y			T.B.D			
Uniformity		U		75	80	-	%	Note(1)(6)
NTSC			CIE1931	45	50	-	%	
Luminance		L		**410**	**470**	-	cd/m^2	Note(7)

Test Conditions:

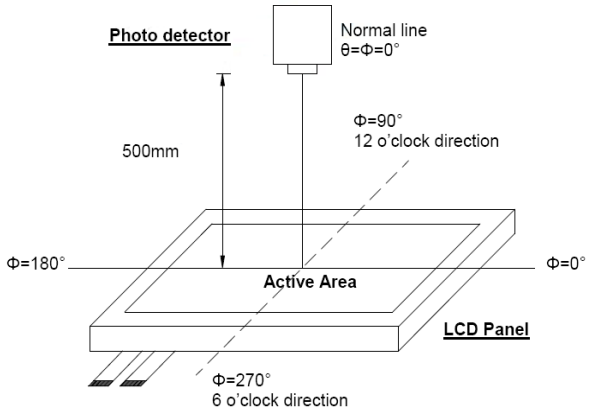
1. IF= 80mA, the ambient temperature is 25℃.
2. The test systems refer to Note (1) and Note (2).

Definition of optical measurement system

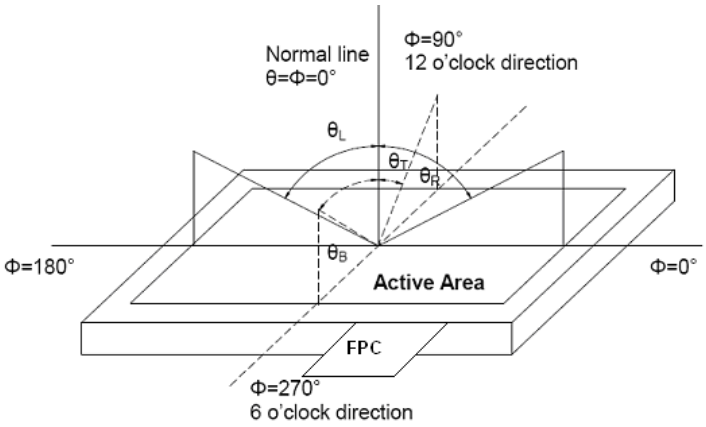
The optical characteristics should be measured in dark room. After 10 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.

Note(1) Definition of optical measurement system

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-7/Field of view: 1° / Height: 500mm.)

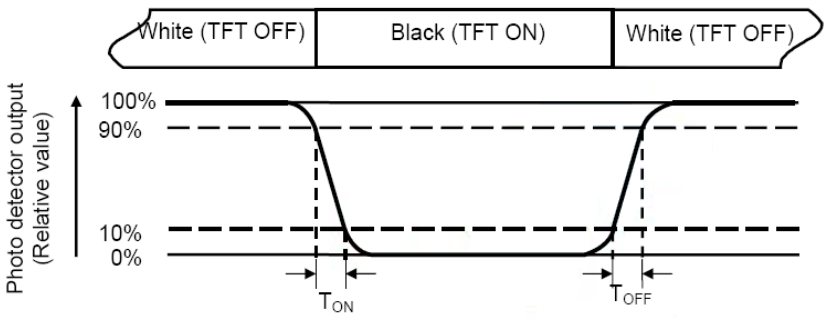


Note(2) Definition of viewing angle range



Note(3) Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note(4) Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

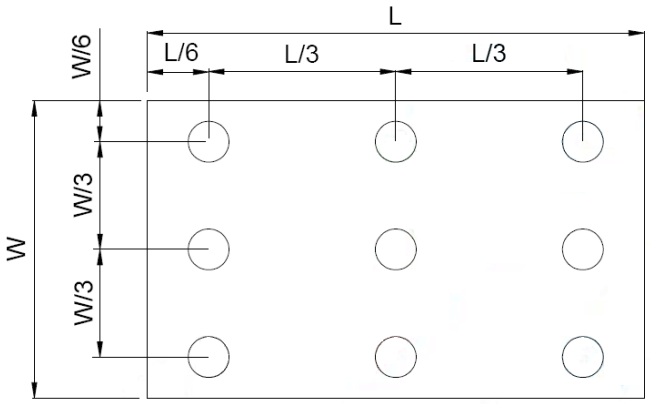
Note(5) Definition of color chromaticity (CIE1931)
Color coordinated measured at center point of LCD.

Note(6) All input terminals LCD panel must be ground when measuring the center area of the panel.

Note(7) Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (Refer to bellow figure). Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity (Yu)} = \frac{\text{Bmin}}{\text{Bmax}}$$

L ----- Active area length W ----- Active area width



Bmax: The measured maximum luminance of all measurement position.
Bmin: The measured minimum luminance of all measurement position.

10 Reliability Test Items

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=240 hrs	
Low Temperature Operation	-20±3°C , t=240 hrs	
High Temperature Storage	80±3°C , t=240 hrs	1,2
Low Temperature Storage	-30±3°C , t=240 hrs	1,2
Storage at High Temperature and Humidity	60°C, 90% RH , 240 hrs	1,2
Thermal Shock Test	-20°C (30min) ~ 70°C (30min) 100 cycles	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note(1) Condensation of water is not permitted on the module.

Note(2) The module should be inspected after 1 hour storage in normal conditions (15-35°C, 45-65%RH).

Note(3) The module shouldn't be tested over one condition, and all the tests are independent.

Note(4) All reliability tests should be done without the protective film.

Definitions of life end point:

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

11 General Precaution

11.1 Disassembling or Modification

(1) Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. AMPIRE does not warrant the module, if customers disassemble or modify the module.

11.2 Breakage of LCD Panel

(1) If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.
(2) If liquid crystal contacts mouth or eyes, rinse out with water immediately.
(3) If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.
(4) Handle carefully with chips of glass that may cause injury, when the glass is broken.

11.3 Electric Shock

(1) Disconnect power supply before handling LCD module.
(2) Do not pull or fold the LED cable.
(3) Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

11.4 Absolute Maximum Ratings and Power Protection Circuit

(1) Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.
(2) Please do not leave LCD module in the environment of high humidity and high temperature for a long time.
(3) It's recommended to employ protection circuit for power supply.

11.5 Operation

(1) Do not touch, push or rub the polarizer with anything harder than HB pencil lead.
(2) Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.
(3) When the surface is dusty, please wipe gently with absorbent cotton or other soft material.
(4) Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may cause deformation or color fading.

(5) When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzene or other adequate solvent.

11.6 Mechanism

(1) Please mount LCD module by using mounting holes arranged in four corners tightly.

11.7 Static Electricity

(1) Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

(2) Because LCD modules use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

11.8 Strong Light Exposure

(1) The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

11.9 Disposal

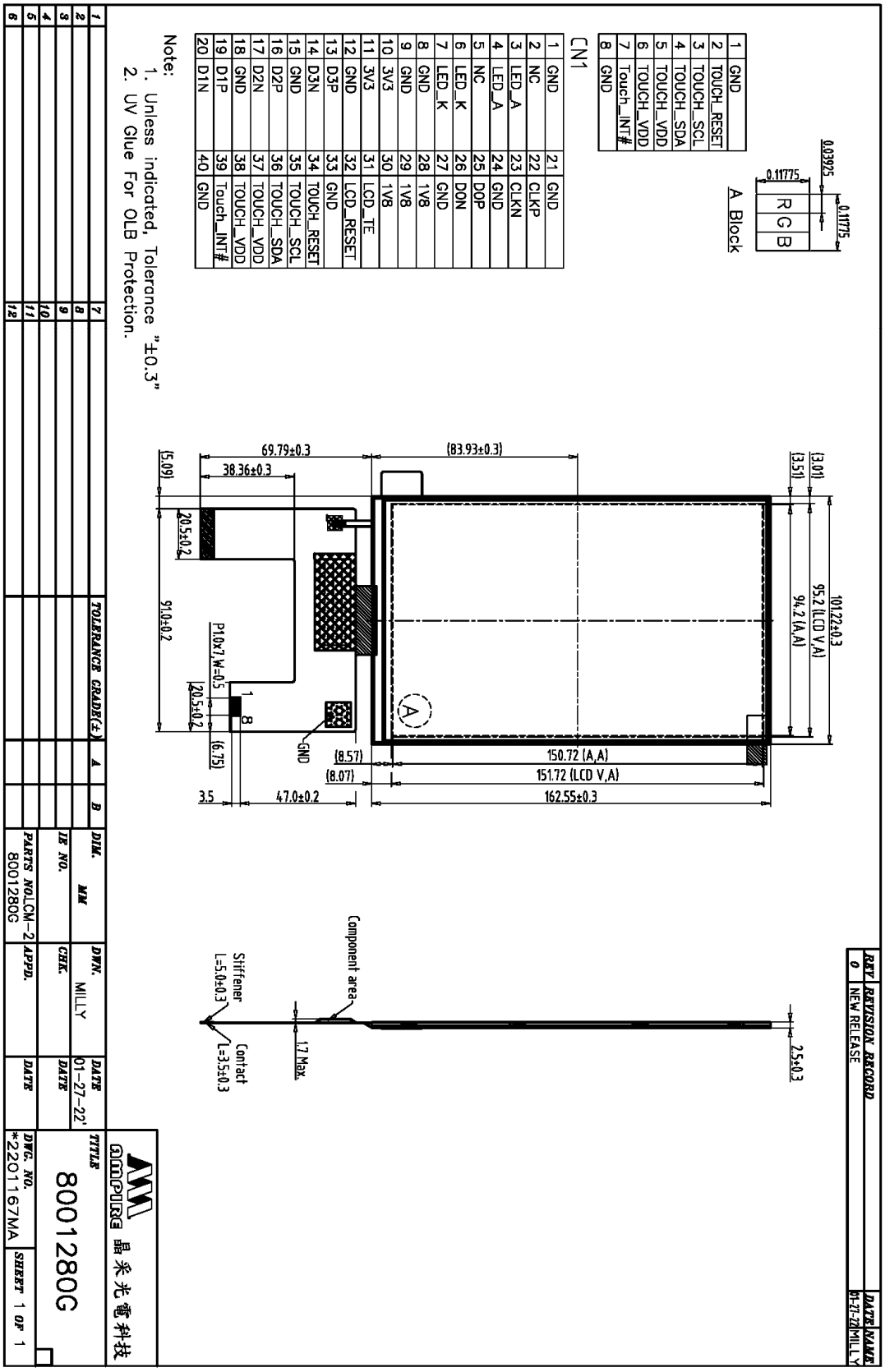
(1) When disposing LCD module, obey the local environmental regulations.

11.10 Others

(1) AMIPRE will provide one year warrantee for all products, and three months warrantee for all repairing products.

(2) Do not keep the LCD at the same display pattern continually. The residual image will happen and it will damage the LCD. Please use screen saver.

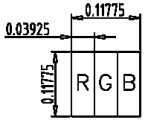
12 Outline Dimension



1	GND
2	TOUCH_RESET
3	TOUCH_SCL
4	TOUCH_SDA
5	TOUCH_VDD
6	TOUCH_VDD
7	Touch_INT#
8	GND

1	GND	21	GND
2	NC	22	CLKP
3	LED_A	23	CLKN
4	LED_A	24	GND
5	NC	25	DOP
6	LED_K	26	DON
7	LED_K	27	GND
8	GND	28	1V8
9	GND	29	1V8
10	3V3	30	1V8
11	3V3	31	LCD_TE
12	GND	32	LCD_RESET
13	D3P	33	GND
14	D3N	34	TOUCH_RESET
15	GND	35	TOUCH_SCL
16	D2P	36	TOUCH_SDA
17	D2N	37	TOUCH_VDD
18	GND	38	TOUCH_VDD
19	D1P	39	Touch_INT#
20	D1N	40	GND

REV	REVISION RECORD	DATE	NAME
0	NEW RELEASE	01-27-22	MILLY



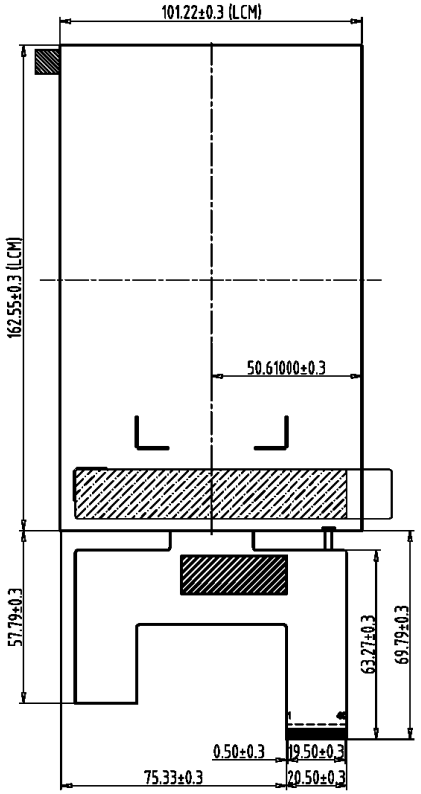
A Block

1	GND
2	TOUCH_RESET
3	TOUCH_SCL
4	TOUCH_SDA
5	TOUCH_VDD
6	TOUCH_VDD
7	Touch_INT#
8	GND

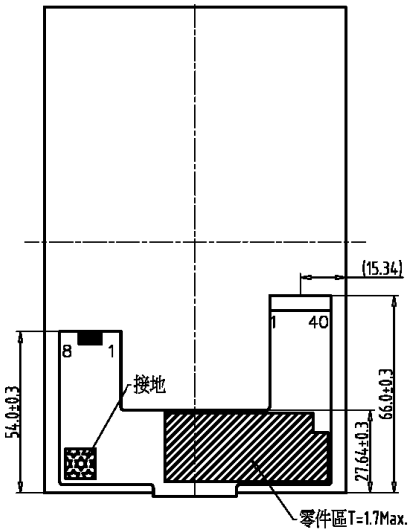
CN1

1	GND	21	GND
2	NC	22	CLKP
3	LED_A	23	CLKN
4	LED_A	24	GND
5	NC	25	D0P
6	LED_K	26	D0N
7	LED_K	27	GND
8	GND	28	1V8
9	GND	29	1V8
10	3V3	30	1V8
11	3V3	31	LCD_TE
12	GND	32	LCD_RESET
13	D3P	33	GND
14	D3N	34	TOUCH_RESET
15	GND	35	TOUCH_SCL
16	D2P	36	TOUCH_SDA
17	D2N	37	TOUCH_VDD
18	GND	38	TOUCH_VDD
19	D1P	39	Touch_INT#
20	D1N	40	GND

Note:
1. Unless indicated, Tolerance "±0.3"
2. UV Glue For OLB Protection.



Back View



Bending

1		7		TOLERANCE GRADE(±)	A	B	DIM. MM	DWN. MILLY	DATE 01-27-22'	TITLE 8001280G	
2		8					IE NO.	CHK.	DATE		
3		9									
4		10									
5		11					PARTS NO. LCM-3 8001280G	APPD.	DATE	DWG. NO. *2201168MA	SHEET 1 OF 1
6		12									

AMPIRE 晶采光電科技

13 Package

TBD