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SPECIFICATION
FOR
TFT MODULE

MODULE NO. : AVD-TT101WX-NW-228-S

CUSTOMER NO. :

Rev No. : O

AVD	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE	叶嘉峰		何鹏
DATE	2022.11.09	2022.11.09	2022.11.09

CUSTOMER APPROVAL	SIGNATURE	DATE

Notes :

1、Please contact AVD before assigning your product based on this module specification.

2、To improve the quality of product, this product specification is subject to being changed without any notice.

REVISION RECORD

Rev No.	Contents	Prepared	Rev date
O	First release	Ye Jiafeng	2022-11-09

CONTENTS

1. GENERAL INFORMATION

No.	Item	Contents	Unit
1	LCD size	10.1 inch (Diagonal)	/
2	Display mode	IPS/NORMALLY BLACK/Transmissive	/
3	Viewing direction(eye)	FREE	/
4	Gray scale inversion direction	-	/
5	Resolution(H*V)	1280*800 Pixels	/
6	Module size (L*W*H)	229.70*149.15*5.00	mm
7	Active area (L*W)	216.96*135.60	mm
8	Pixel pitch (L*W)	0.1695*0.1695	mm
9	Interface type	LVDS interface	/
10	Color Depth	16.7M	/
11	Module power consumption	4.19(Appr)	W
12	Back light type	EDGE&WHITE LED	/
13	Driver IC	EK79202B1 OR COMPATIBLE	/
14	Weight	273(Appr)	G

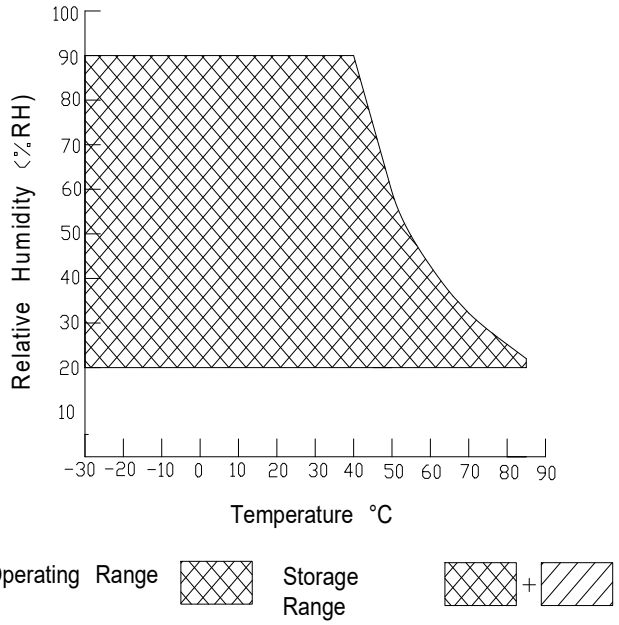
2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Power supply input voltage for TFT	VDD	2.3	3.6	V	
Backlight current (normal temp.)	ILED	-	350	mA	
Operation temperature	Top	-30	+85	℃	Note1
Storage temperature	Tst	-30	+85	℃	Note1
Humidity	RH	20%	90%	RH	Note1

Note1 :

1).The relative humidity and temperature range are as below sketch,90%RH Max.

2).The maximum wet bulb temperature ≤40℃ and without dewing.



3. ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS(at Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply input voltage(TFT Module)	VDD	3.1	3.3	3.5	V	
Power supply current	IVDD	-	250	-	mA	
LVDS Differential input high Threshold voltage	RxVTH	100	200	300	mV	RXVCM=1.2V
LVDS Differential input low Threshold voltage	RxVTL	-300	-200	-100	mV	
LVDS Differential input common mode voltage	RxVCM	1	1.2	1.4	V	
LVDS Differential voltage	|VID|	200	-	600	mV	
TFT gate on voltage	VGH	-	-	-	V	Note1
TFT gate off voltage	VGL	-	-	-	V	Note1
Analog power supply voltage	AVDD	-	-	-	V	Note1
Differential input common mode voltage	Vcom	-	-	-	V	Note1

Note1 : The value is just the reference value. VCOM must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..

4. BACKLIGHT CHARACTERISTICS

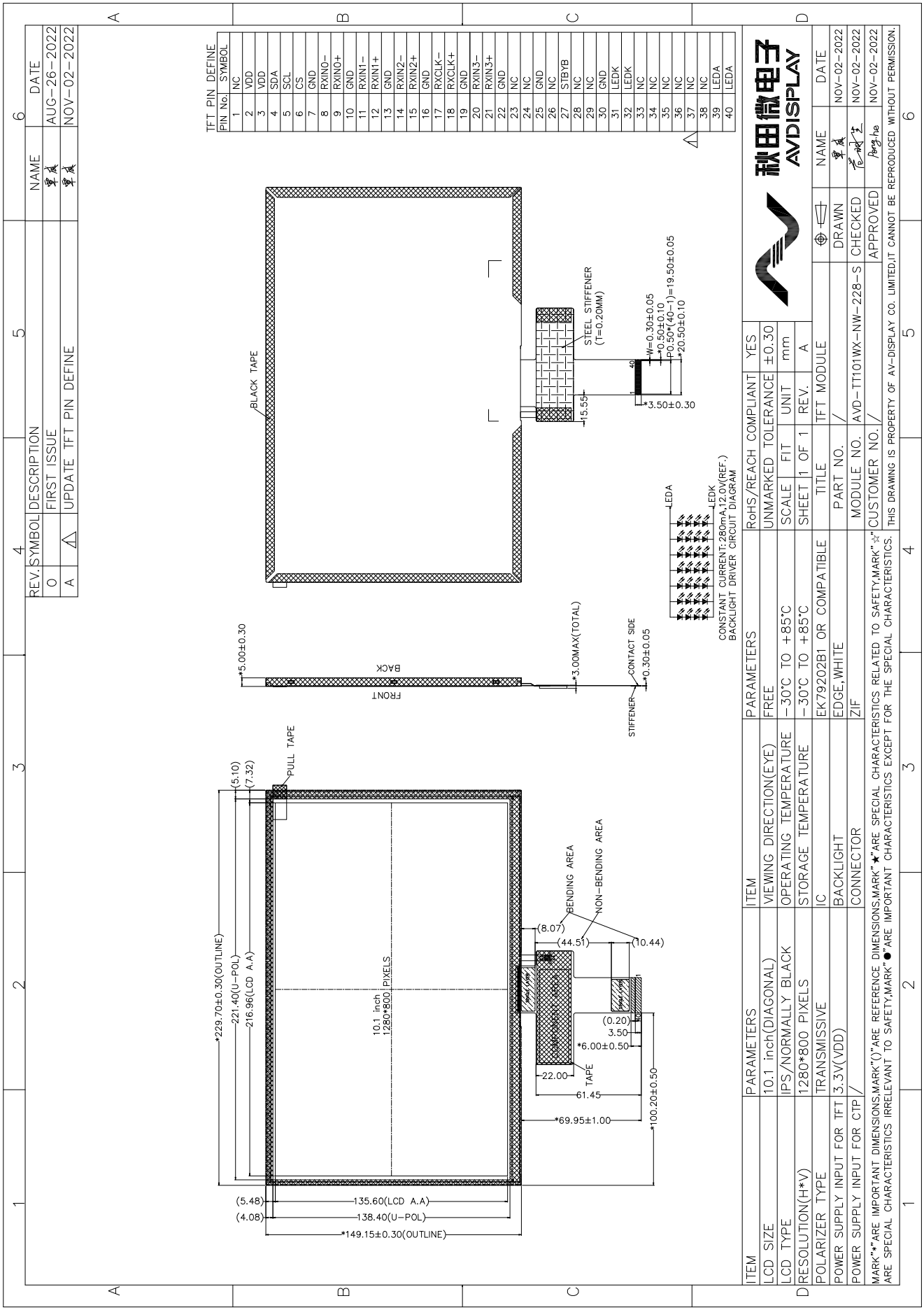
(at Ta=25℃,RH=60%)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED forward voltage	VF	10.8	12	13.2	V	
LED forward current	IF	-	280	-	mA	IF=40*7mA
LED power consumption	PLED	-	3.36	-	W	Note1
Number of LED	-		28		PCS	
Connection mode	-	4 in series 7 in parallel			/	
LED life-time	-	30000	-	-	Hrs	Note2

Note1 : Calculator value for reference : IF*VF = PLED

Note2 : The LED life-time define as the estimated time to 50% degradation of initial brightness at Ta=25℃ and IF =280mA. The LED lifetime could be decreased if operating IF is larger than 280mA.

5. EXTERNAL DIMENSIONS



6. ELECTRO - OPTICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time	Tr+ Tf	-	-	25	35	ms	FIG.1	Note 1
Contrast ratio	Cr		640	800	-	-	FIG.2	Note 2
Surface luminance	Lv	θ=0°	400	500	-	cd/m^2	FIG.2	Note 3
Luminance uniformity	Yu	θ=0°	75	80	-	%	FIG.2	Note 4
NTSC	-	θ=0°	45	50	-	%	FIG.2	Note 5
Viewing angle	θ	∅=90°	70	80	-	deg	FIG.3	Note 6
		∅=270°	70	80	-	deg	FIG.3	
		∅=0°	70	80	-	deg	FIG.3	
		∅=180°	70	80	-	deg	FIG.3	
CIE (x,y) chromaticity	Red x	θ=0° ∅=0° Ta=25℃	Typ -0.04	0.59	Typ +0.04	-	FIG.2 CIE1931	Note 5
	Red y			0.34		-		
	Green x			0.35		-		
	Green y			0.59		-		
	Blue x			0.15		-		
	Blue y			0.12		-		
	White x			0.31		-		
	White y			0.34		-		

The TFT module should be stabilized at a given temperature for 10 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 10 minutes in a windless room.

Note1. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state.

Normally white:Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

Normally black:Rise time (T_{ON}) is the time between photo detector output intensity changed from 10% to 90%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 90% to 10%.

For additional information see FIG1.

Note2.Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula.

For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

Measured at the center area of the LCD

Note3.Definition of surface luminance

Surface luminance is the luminance with all pixels displaying white.

For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note4.Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$Yu = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position.For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10 angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the display surface.

For more information see FIG.3.
For viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on CS-2000/BM-7 photo detector or compatible.

FIG.1. The definition of response Time

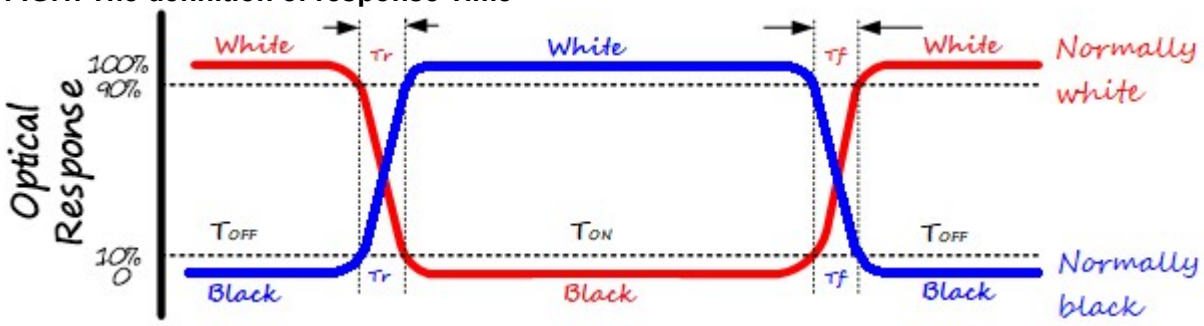


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

H,V : Active area
Light spot size ∅=1.5mm or ∅=7.7mm (CS-2000/BM-7)50cm distance or compatible distance from the LCM surface to detector lens.
Test spot position : see Figure a.
measurement instrument : Luminance meter CS-2000/BM-7 or compatible ,see Figure b.

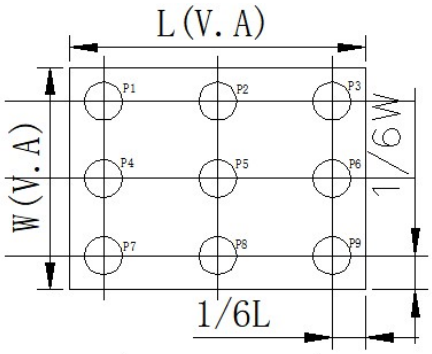


Figure a

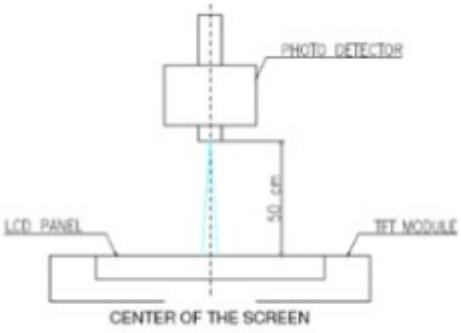
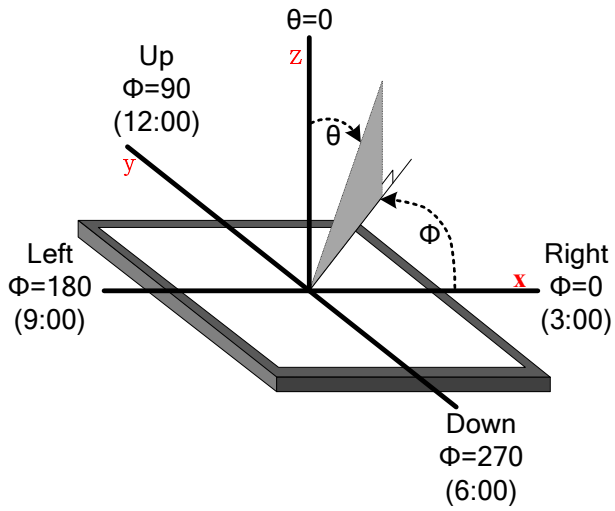


Figure b

FIG.3. The definition of viewing angle



7. INTERFACE DESCRIPTION

Interface No.	Name	I/O or connect to	Description
1	NC	/	No Connection
2-3	VDD	P	Power for LCD
4	SDA	I	Serial communication data input
5	SCL	I	Serial communication clock input
6	CS	I	Serial communication enables. Normally pull high
7	GND	P	Power ground
8	RXIN0-	I	LVDS data lane 0-
9	RXIN0+	I	LVDS data lane 0+
10	GND	P	Power ground
11	RXIN1-	I	LVDS data lane 1-
12	RXIN1+	I	LVDS data lane 1+
13	GND	P	Power ground
14	RXIN2-	I	LVDS data lane 2-
15	RXIN2+	I	LVDS data lane 2+
16	GND	P	Power ground
17	RXCLK -	I	LVDS clk lane -
18	RXCLK+	I	LVDS clk lane +
19	GND	P	Power ground
20	RXIN3-	I	LVDS data lane 3-
21	RXIN3+	I	LVDS data lane 3+
22	GND	P	Power ground
23-24	NC	/	/
25	GND	P	Power ground
26	NC	/	/
27	STBYB	I	Standby mode. Normally pull high. STBYB = L, timing controller, source driver will turn off, all output are High-Z. STBYB = H, normal operation.
28-29	NC	/	/
30	GND	P	Power ground
31-32	LEDK	P	LED Cathode for BL
33-38	NC	/	/
39-40	LEDA	P	LED ANODE for BL

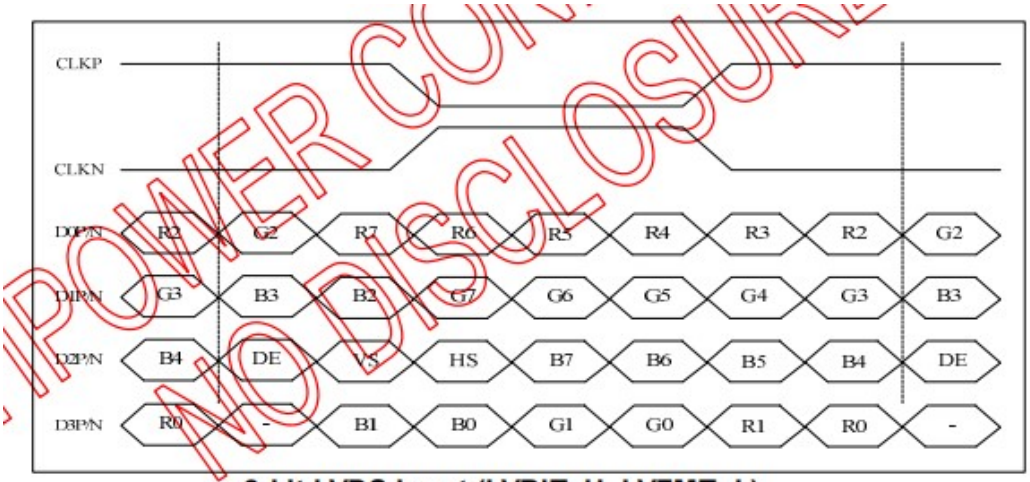
Module Interface description
I: input, O: output, P: Power,NC or / : No connection

8.AC CHARACTERISTICS

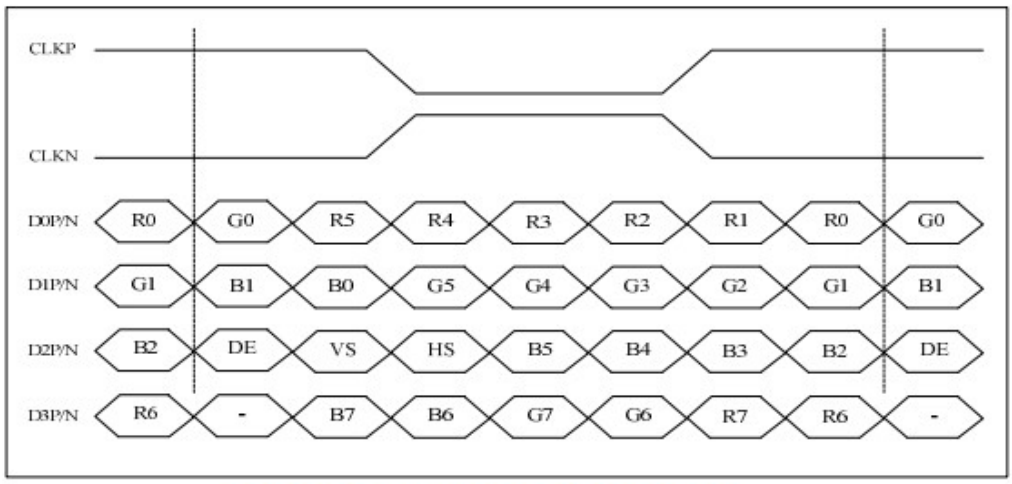
8.1 Video Interface and Timing Table

LVDS interface

Data input format for LVDS



8-bit LVDS input (LVBIT=H, LVFMT=L)



8-bit LVDS input(LVBIT=H, LVFMT=H)

8.2 LVDS/MIPI Input Timing Table

For 1280RGBx800

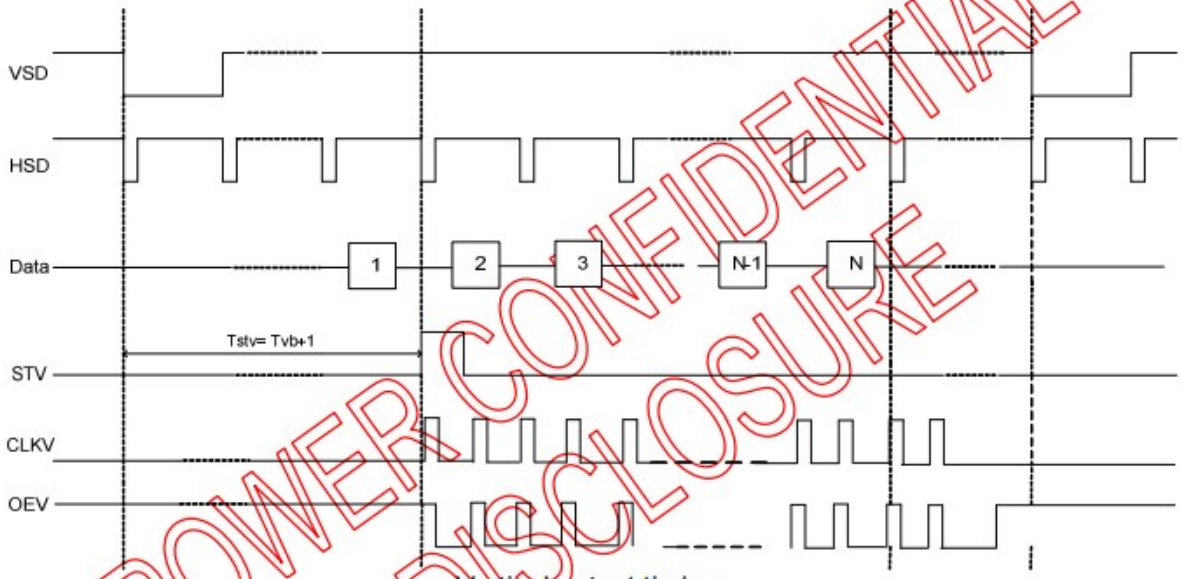
Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
DCLK frequency @Frame rate=60Hz (LVDS)		F_{DCLK}	66.3	72.4	78.9	MHz
HSYNC period time		T_H	1380	1440	1500	DCLK
Horizontal display area		T_{HD}		1280		DCLK
HSYNC pulse width	Min.	T_{HPW}		1		
	Typ.			-		
	Max.			40		
HSYNC back porch(with pulse width)		T_{HBP}	88	88	88	DCLK
HSYNC front porch		T_{HFP}	12	72	132	DCLK
VSYNC period time		T_V	824	838	872	H
Vertical display area		T_{VD}		800		H
VSYNC pulse width	Min.	T_{VPW}		1		H
	Typ.			-		
	Max.			20		
VSYNC back porch(with pulse width)		T_{VBP}	23	23	23	H
VSYNC front porch		T_{VFP}	1	15	49	H

MIPI Frequency = (Frame rate) x TH x TV x 24bits.
Mini-LVDS (3-pair) = DCLK rate x 3.

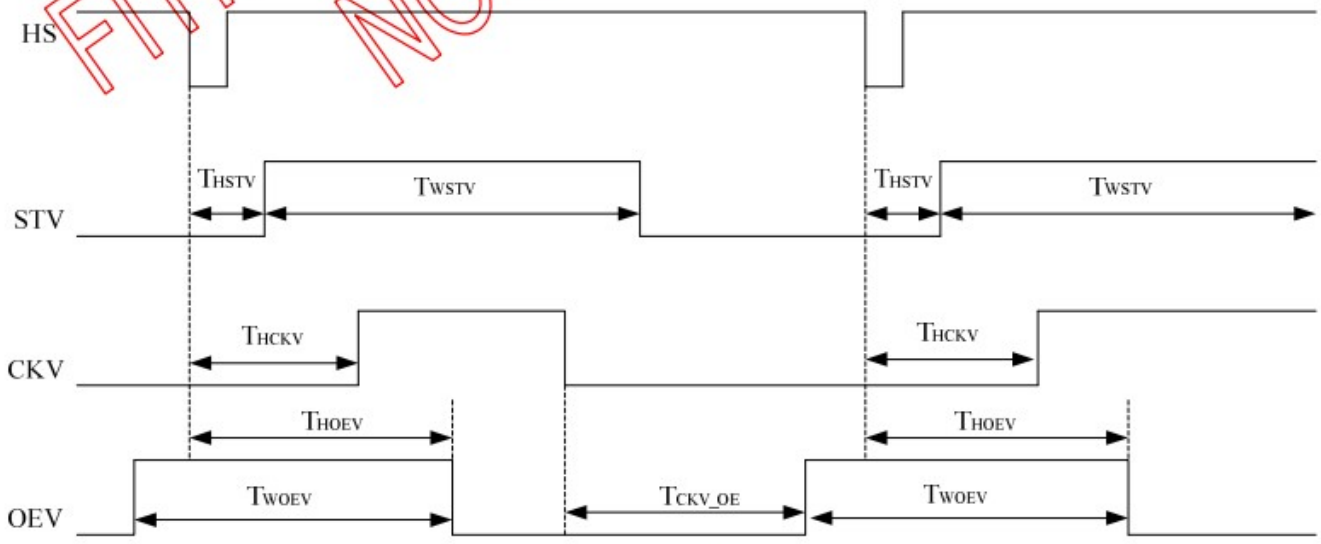
8.3 Gate Output Timing Table

(VDD=2.3 to 3.6V, VSS=VSSA=VSS_IF=0V, TA=-20 to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
STV Pulse Width	T_{WSTV}	-	1	-	H
Time from HSD to STV	T_{HSTV}	-	2	-	DCLK
Time from HSD to CKV	T_{HCKV}	-	25	-	DCLK
Time from HSD to OEV	T_{HOEV}	-	35	-	DCLK
Time from CKV to OEV	T_{CKV_OE}	-	168	-	DCLK
OEV Pulse Width	T_{WOEV}	-	188	-	DCLK



Vertical output timing

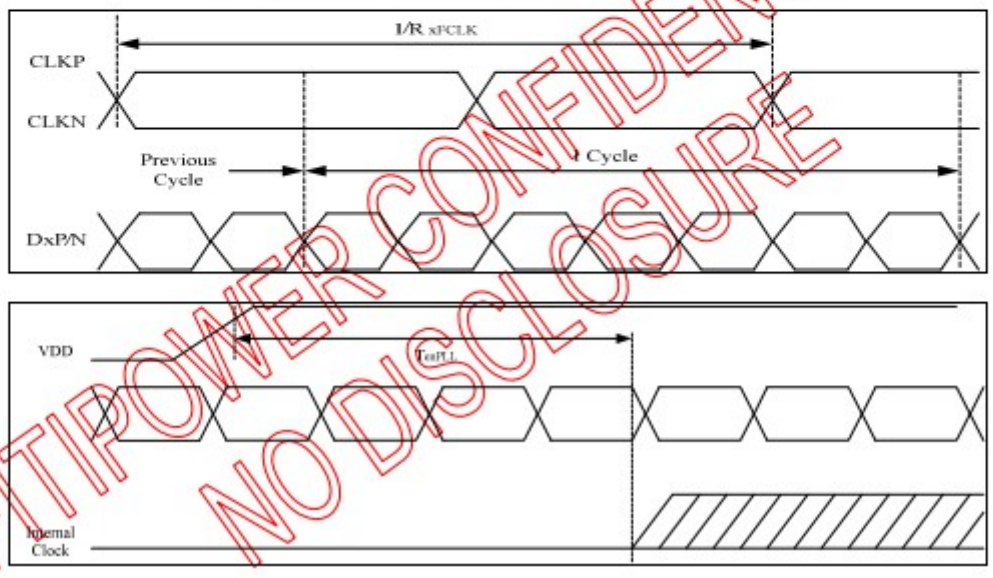


Gate output timing

8.4 LVDS mode AC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Clock frequency	R_{xFCLK}	30	-	TBD	MHz	Refer to input timing table for each display resolution
Input data skew margin	T_{RSKM}	500	-	-	ps	|VID| = 200mV RxVCM = 1.2V RxFCLK = 81MHz
Clock high time	T_{LVCH}	-	4/(7* R_{xFCLK})	-	ns	
Clock low time	T_{LVCL}	-	3/(7* R_{xFCLK})	-	ns	
PLL wake-up time	T_{enPLL}	-	-	150	us	

Table 13.1: LVDS mode AC electrical characteristics



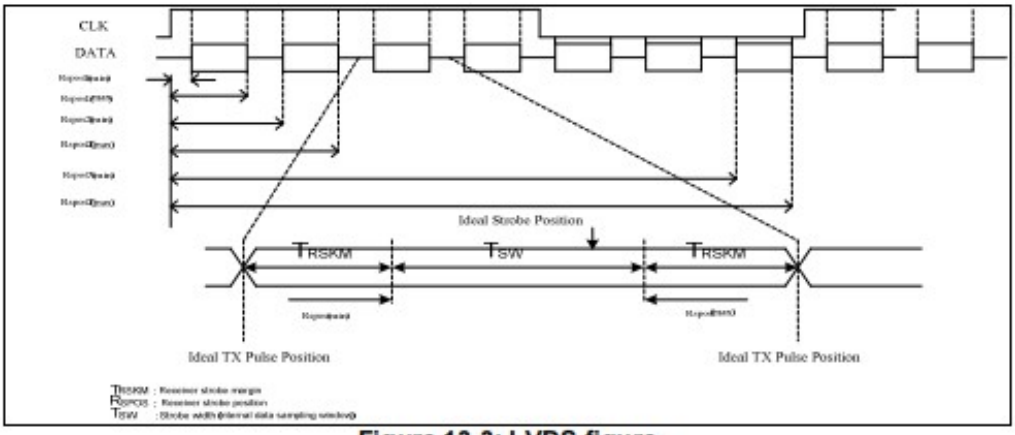
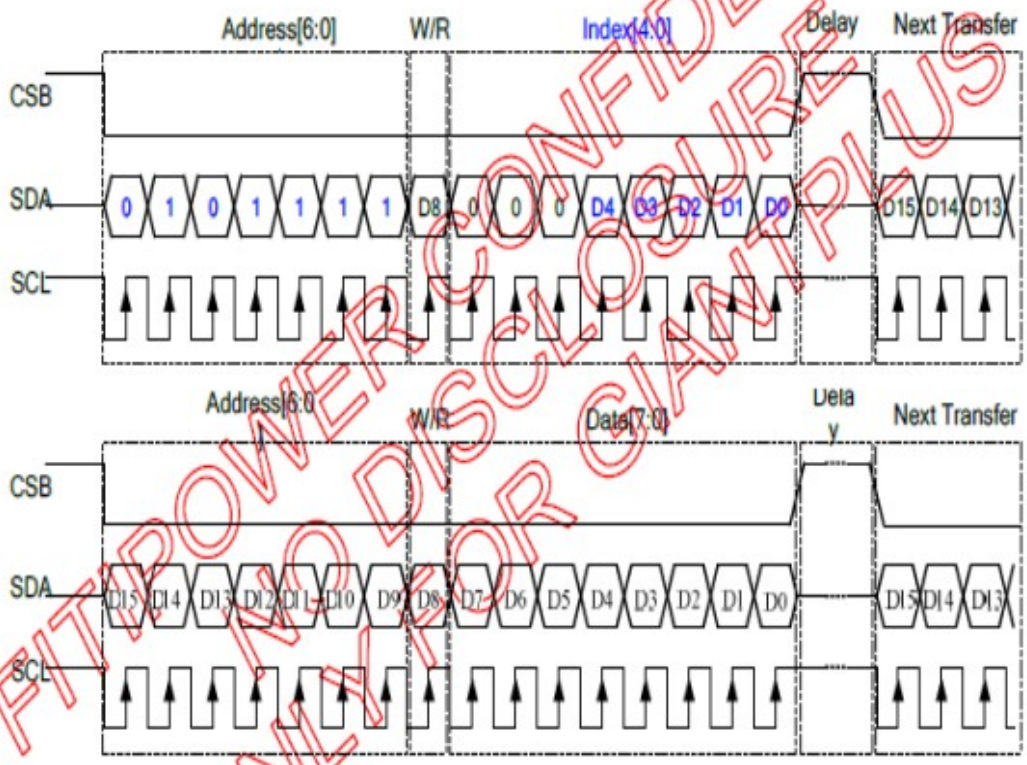


Figure 13.3: LVDS figure

Register Write by SPI

For prevent from incorrect setting of the internal register. Please refer to the section of "3-Wire Timing. Because the 3-wire only can read/write one address. So we put the "parameter index" at the address 0x2F. When 3-wire command sends, it will refer to the address 0x2F[4:0] as the parameter index value.



3-Wire Command Format:

Bit	Description
D15-D9	Register Address [6:0].
D8	W/R control bit. "0" for Write; "1" for Read
D7-D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [6:0]							0	Data (Issue by external controller)							

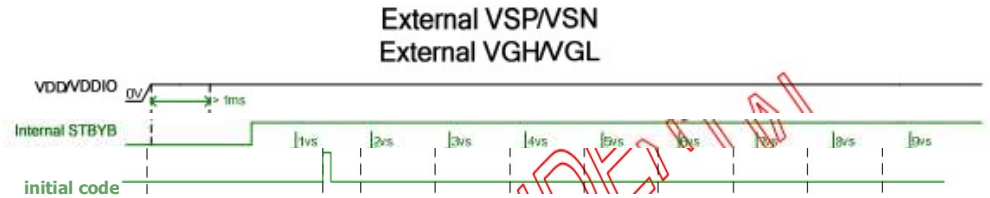
3-Wire Read Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [6:0]							1	Data (Issue by 3-Wire engine)							

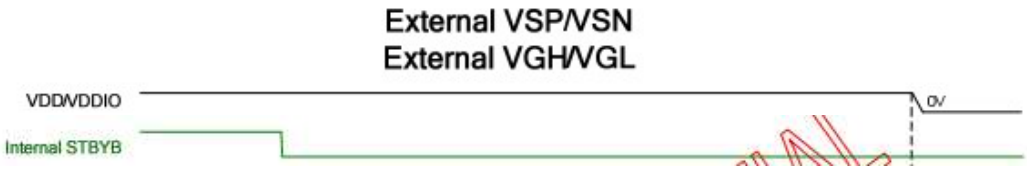
9. POWER SEQUENCE

To prevent the device damage from latch up and Improve subjective display effect,the power ON/OFF sequence shown below must be followed.

9.1 Power on sequence



9.2 Power off sequence



10. RELIABILITY TEST CONDITIONS

<table>
<tr><th>No.</th><th>Test item</th><th colspan="2">Test condition</th><th>Inspection after test</th></tr>
<tr><td>10.1</td><td>High temperature storage test</td><td colspan="2">+85℃/240 hours</td><td rowspan="12">Inspection after 2~4hours storage at room temperature, the sample should not have following defects:
1.Current changing value before test and after test is 50% larger;
2. Function defect : Non-display,abnormal-display,missing lines, Short lines,ITO corrosion;
3.Visual defect : Air bubble in the LCD,Seal leak,Glass crack.</td></tr>
<tr><td>10.2</td><td>Low temperature storage test</td><td colspan="2">-30℃/240 hours</td></tr>
<tr><td>10.3</td><td>High temperature operating test</td><td colspan="2">+85℃/240 hours</td></tr>
<tr><td>10.4</td><td>Low temperature operating test</td><td colspan="2">-30℃/240 hours</td></tr>
<tr><td>10.5</td><td>Thermal Shock
(non-operation)</td><td colspan="2">-30℃ ←→ +85℃/80cycles
(30min.)(<30sec.) (30min.)</td></tr>
<tr><td>10.6</td><td>High temperature high humidity test</td><td colspan="2">+60℃*90% RH/240 hours</td></tr>
<tr><td>10.7</td><td>Vibration test for Packaging</td><td colspan="2">Frequency : 250 r/min
Amplitude : 1 inch
Time: 45min</td></tr>
<tr><td rowspan="5">10.8</td><td rowspan="5">Drop test for Packaging</td><td colspan="2">Drop direction:
1 corner/3 edges/6 sides 10 times</td></tr>
<tr><td>Packing weight(kg)</td><td>Drop height(cm)</td></tr>
<tr><td>＜11</td><td>80±1.6</td></tr>
<tr><td>11≦G＜21</td><td>60±1.2</td></tr>
<tr><td>21≦G＜31</td><td>50±1.0</td></tr>
<tr><td>31≦G＜40</td><td>40±0.8</td></tr>
<tr><td>10.9</td><td>ESD test</td><td colspan="2">Air discharge: ±12KV, 10times
Contact discharge: ±6KV, 10times</td></tr>
</table>

Remark :
1.The test samples should be applied to only one test item.
2.Sample size for each test item is 3~5pcs.
3.For High temperature high humidity test, Pure water(Resistance>10MΩ) should be used.
4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5.Failure judgment criterion: Basic specification, Electrical characteristic, Mechanical characteristic, Optical characteristic.
6.After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

11.INSPECTION CRITERION

Refer to 《Inspection Criterion for TFT Products-To customer》，DOCUMENT NO.: AVD(WI)-00-QA-048

12. HANDLING PRECAUTIONS

12.1 Mounting method

The TFT module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.
Extreme care should be needed when handling the TFT modules.

12.2 Caution of TFT module handling and cleaning

When cleaning the display surface, Use soft cloth with solvent
[recommended below] and wipe lightly :
●.Isopropyl alcohol
●.Ethyl alcohol
Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.
Do not use the following solvent :
●.Water
●.Aromatics
Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns
Do not use the following solvent on the pad or prevent it from being contaminated :
●.Soldering flux
●.Chlorine (Cl) , Sulfur (S)
If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.
If ITO corrosion happen by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The TFT module use C-MOS LSI drivers, so we recommended that you :
Connect any unused input terminal to Vdd or Vss, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

12.4 Packing

Module employ TFT elements and must be treated as such.
●.Avoid intense shock and falls from a height.
●.To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

12.5 Caution for operation

●.It is an indispensable condition to drive TFT module within the specified voltage limit since the higher voltage then the limit cause the shorter TFT module life.
●.An electrochemical reaction due to direct current causes TFT module undesirable deterioration, so that the use of direct current drive should be avoided.
●.Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature TFT module how dark color in them. However those phenomena do not mean malfunction or out of order with TFT module, which will come back in the specified operation temperature.
●.If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
●.A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.
●.Usage under the maximum operating temperature, 50%Rh or less is required.
●.When fixed patterns are displayed for a long time,remnant image is likely to occur.

12.6 Storage

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.
●.Storing in an ambient temperature 10℃ to 30℃, and in a relative humidity of 45% to 75%. Don't expose to sunlight or fluorescent light.
●.Storing in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it . And with no desiccant.
●.Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.

●.Storing with no touch on polarizer surface by the anything else.
It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

12.7 Safety

●.It is recommendable to crash damaged or unnecessary TFT module into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
●.When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

13. PRECAUTION FOR USE

13.1 A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.
13.2 On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.
●.When a question is arisen in this specification.
●.When a new problem is arisen which is not specified in this specifications.
●.When an inspection specifications change or operating condition change in customer is reported to AVD, and some problem is arisen in this specification due to the change.
●.When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14. PACKING SPECIFICATION

Please consult our technical department for detail information.

15. INITIALIZATION CODE

```
ESET();

SPI3_9bit_WWR_CMD(0x4D,0x00);SPI3_9bit_WWR_DAT(0xAA);

SPI3_9bit_WWR_CMD(0x52,0x00);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x52,0x01);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x52,0x02);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x52,0x03);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x52,0x04);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x52,0x05);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x52,0x06);SPI3_9bit_WWR_DAT(0x12);
SPI3_9bit_WWR_CMD(0x52,0x07);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x52,0x08);SPI3_9bit_WWR_DAT(0x10);
SPI3_9bit_WWR_CMD(0x52,0x09);SPI3_9bit_WWR_DAT(0x11);
SPI3_9bit_WWR_CMD(0x52,0x0A);SPI3_9bit_WWR_DAT(0x04);
SPI3_9bit_WWR_CMD(0x52,0x0B);SPI3_9bit_WWR_DAT(0x05);
SPI3_9bit_WWR_CMD(0x52,0x0C);SPI3_9bit_WWR_DAT(0x06);
SPI3_9bit_WWR_CMD(0x52,0x0D);SPI3_9bit_WWR_DAT(0x07);
SPI3_9bit_WWR_CMD(0x52,0x0E);SPI3_9bit_WWR_DAT(0x08);
SPI3_9bit_WWR_CMD(0x52,0x0F);SPI3_9bit_WWR_DAT(0x09);
SPI3_9bit_WWR_CMD(0x52,0x10);SPI3_9bit_WWR_DAT(0x0A);
SPI3_9bit_WWR_CMD(0x52,0x11);SPI3_9bit_WWR_DAT(0x0B);
SPI3_9bit_WWR_CMD(0x52,0x12);SPI3_9bit_WWR_DAT(0x03);
SPI3_9bit_WWR_CMD(0x52,0x13);SPI3_9bit_WWR_DAT(0x0C);
SPI3_9bit_WWR_CMD(0x52,0x14);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x52,0x15);SPI3_9bit_WWR_DAT(0x13);

SPI3_9bit_WWR_CMD(0x59,0x00);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x59,0x01);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x59,0x02);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x59,0x03);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x59,0x04);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x59,0x05);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x59,0x06);SPI3_9bit_WWR_DAT(0x12);
SPI3_9bit_WWR_CMD(0x59,0x07);SPI3_9bit_WWR_DAT(0x13);
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SPI3_9bit_WWR_CMD(0x59,0x08);SPI3_9bit_WWR_DAT(0x10);
SPI3_9bit_WWR_CMD(0x59,0x09);SPI3_9bit_WWR_DAT(0x11);
SPI3_9bit_WWR_CMD(0x59,0x0A);SPI3_9bit_WWR_DAT(0x04);
SPI3_9bit_WWR_CMD(0x59,0x0B);SPI3_9bit_WWR_DAT(0x05);
SPI3_9bit_WWR_CMD(0x59,0x0C);SPI3_9bit_WWR_DAT(0x06);
SPI3_9bit_WWR_CMD(0x59,0x0D);SPI3_9bit_WWR_DAT(0x07);
SPI3_9bit_WWR_CMD(0x59,0x0E);SPI3_9bit_WWR_DAT(0x08);
SPI3_9bit_WWR_CMD(0x59,0x0F);SPI3_9bit_WWR_DAT(0x09);
SPI3_9bit_WWR_CMD(0x59,0x10);SPI3_9bit_WWR_DAT(0x0A);
SPI3_9bit_WWR_CMD(0x59,0x11);SPI3_9bit_WWR_DAT(0x0B);
SPI3_9bit_WWR_CMD(0x59,0x12);SPI3_9bit_WWR_DAT(0x03);
SPI3_9bit_WWR_CMD(0x59,0x13);SPI3_9bit_WWR_DAT(0x0C);
SPI3_9bit_WWR_CMD(0x59,0x14);SPI3_9bit_WWR_DAT(0x13);
SPI3_9bit_WWR_CMD(0x59,0x15);SPI3_9bit_WWR_DAT(0x13);

SPI3_9bit_WWR_CMD(0x32,0x00);
SPI3_9bit_WWR_DAT(0x03);

SPI3_9bit_WWR_CMD(0x34,0x00);
SPI3_9bit_WWR_DAT(0x7E);

SPI3_9bit_WWR_CMD(0x5F,0x00);
SPI3_9bit_WWR_DAT(0x38);

SPI3_9bit_WWR_CMD(0x2B,0x00);
SPI3_9bit_WWR_DAT(0x20);

SPI3_9bit_WWR_CMD(0x35,0x00);
SPI3_9bit_WWR_DAT(0x05);

SPI3_9bit_WWR_CMD(0x33,0x00);
SPI3_9bit_WWR_DAT(0x08);

SPI3_9bit_WWR_CMD(0x51,0x00);
SPI3_9bit_WWR_DAT(0x80);

SPI3_9bit_WWR_CMD(0x73,0x00);
SPI3_9bit_WWR_DAT(0xF0);

SPI3_9bit_WWR_CMD(0x74,0x00);
SPI3_9bit_WWR_DAT(0x91);

SPI3_9bit_WWR_CMD(0x75,0x00);
SPI3_9bit_WWR_DAT(0x03);

SPI3_9bit_WWR_CMD(0x71,0x00);
SPI3_9bit_WWR_DAT(0xC3);//

SPI3_9bit_WWR_CMD(0x7A,0x00);
SPI3_9bit_WWR_DAT(0x17);

SPI3_9bit_WWR_CMD(0x3C,0x00);
SPI3_9bit_WWR_DAT(0x40);

SPI3_9bit_WWR_CMD(0x4A,0x00);
SPI3_9bit_WWR_DAT(0x02);

SPI3_9bit_WWR_CMD(0x18,0x00);
SPI3_9bit_WWR_DAT(0xFF);

SPI3_9bit_WWR_CMD(0x19,0x00);
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SPI3_9bit_WWR_DAT(0x1F);

SPI3_9bit_WWR_CMD(0x1A,0x00);
SPI3_9bit_WWR_DAT(0xDC);

SPI3_9bit_WWR_CMD(0x4E,0x00);
SPI3_9bit_WWR_DAT(0x4A);

SPI3_9bit_WWR_CMD(0x4F,0x00);
SPI3_9bit_WWR_DAT(0x4C);

SPI3_9bit_WWR_CMD(0x53,0x00);SPI3_9bit_WWR_DAT(0x37);
SPI3_9bit_WWR_CMD(0x53,0x01);SPI3_9bit_WWR_DAT(0x2A);
SPI3_9bit_WWR_CMD(0x53,0x02);SPI3_9bit_WWR_DAT(0x29);
SPI3_9bit_WWR_CMD(0x53,0x03);SPI3_9bit_WWR_DAT(0x2A);
SPI3_9bit_WWR_CMD(0x53,0x04);SPI3_9bit_WWR_DAT(0x2E);
SPI3_9bit_WWR_CMD(0x53,0x05);SPI3_9bit_WWR_DAT(0x2F);
SPI3_9bit_WWR_CMD(0x53,0x06);SPI3_9bit_WWR_DAT(0x22);
SPI3_9bit_WWR_CMD(0x53,0x07);SPI3_9bit_WWR_DAT(0x0D);
SPI3_9bit_WWR_CMD(0x53,0x08);SPI3_9bit_WWR_DAT(0x0E);
SPI3_9bit_WWR_CMD(0x53,0x09);SPI3_9bit_WWR_DAT(0x0C);
SPI3_9bit_WWR_CMD(0x53,0x0A);SPI3_9bit_WWR_DAT(0x0E);
SPI3_9bit_WWR_CMD(0x53,0x0B);SPI3_9bit_WWR_DAT(0x0F);
SPI3_9bit_WWR_CMD(0x53,0x0C);SPI3_9bit_WWR_DAT(0x10);

SPI3_9bit_WWR_CMD(0x54,0x00);SPI3_9bit_WWR_DAT(0x37);
SPI3_9bit_WWR_CMD(0x54,0x01);SPI3_9bit_WWR_DAT(0x2A);
SPI3_9bit_WWR_CMD(0x54,0x02);SPI3_9bit_WWR_DAT(0x29);
SPI3_9bit_WWR_CMD(0x54,0x03);SPI3_9bit_WWR_DAT(0x2A);
SPI3_9bit_WWR_CMD(0x54,0x04);SPI3_9bit_WWR_DAT(0x2E);
SPI3_9bit_WWR_CMD(0x54,0x05);SPI3_9bit_WWR_DAT(0x2F);
SPI3_9bit_WWR_CMD(0x54,0x06);SPI3_9bit_WWR_DAT(0x22);
SPI3_9bit_WWR_CMD(0x54,0x07);SPI3_9bit_WWR_DAT(0x0D);
SPI3_9bit_WWR_CMD(0x54,0x08);SPI3_9bit_WWR_DAT(0x0E);
SPI3_9bit_WWR_CMD(0x54,0x09);SPI3_9bit_WWR_DAT(0x0C);
SPI3_9bit_WWR_CMD(0x54,0x0A);SPI3_9bit_WWR_DAT(0x0E);
SPI3_9bit_WWR_CMD(0x54,0x0B);SPI3_9bit_WWR_DAT(0x0F);
SPI3_9bit_WWR_CMD(0x54,0x0C);SPI3_9bit_WWR_DAT(0x10);

SPI3_9bit_WWR_CMD(0x55,0x00);SPI3_9bit_WWR_DAT(0x11);
SPI3_9bit_WWR_CMD(0x55,0x01);SPI3_9bit_WWR_DAT(0x11);
SPI3_9bit_WWR_CMD(0x55,0x02);SPI3_9bit_WWR_DAT(0x11);
SPI3_9bit_WWR_CMD(0x55,0x03);SPI3_9bit_WWR_DAT(0x11);
SPI3_9bit_WWR_CMD(0x55,0x04);SPI3_9bit_WWR_DAT(0x11);
SPI3_9bit_WWR_CMD(0x55,0x05);SPI3_9bit_WWR_DAT(0x11);
SPI3_9bit_WWR_CMD(0x55,0x06);SPI3_9bit_WWR_DAT(0x11);
SPI3_9bit_WWR_CMD(0x55,0x07);SPI3_9bit_WWR_DAT(0x11);

SPI3_9bit_WWR_CMD(0x56,0x00);
SPI3_9bit_WWR_DAT(0x08);

SPI3_9bit_WWR_CMD(0x67,0x00);
SPI3_9bit_WWR_DAT(0x22);

SPI3_9bit_WWR_CMD(0x6F,0x00);SPI3_9bit_WWR_DAT(0x01);
SPI3_9bit_WWR_CMD(0x6F,0x01);SPI3_9bit_WWR_DAT(0x01);
SPI3_9bit_WWR_CMD(0x6F,0x02);SPI3_9bit_WWR_DAT(0x01);
SPI3_9bit_WWR_CMD(0x6F,0x03);SPI3_9bit_WWR_DAT(0x0A);
SPI3_9bit_WWR_CMD(0x6F,0x04);SPI3_9bit_WWR_DAT(0x01);
SPI3_9bit_WWR_CMD(0x6F,0x05);SPI3_9bit_WWR_DAT(0x01);
SPI3_9bit_WWR_CMD(0x6F,0x06);SPI3_9bit_WWR_DAT(0x11);
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SPI3_9bit_WWR_CMD(0x6F,0x07);SPI3_9bit_WWR_DAT(0x11);
SPI3_9bit_WWR_CMD(0x6F,0x08);SPI3_9bit_WWR_DAT(0x0E);
SPI3_9bit_WWR_CMD(0x6F,0x09);SPI3_9bit_WWR_DAT(0x0C);
SPI3_9bit_WWR_CMD(0x6F,0x0A);SPI3_9bit_WWR_DAT(0x0E);
SPI3_9bit_WWR_CMD(0x6F,0x0B);SPI3_9bit_WWR_DAT(0x0F);
SPI3_9bit_WWR_CMD(0x6F,0x0C);SPI3_9bit_WWR_DAT(0x10);

SPI3_9bit_WWR_CMD(0x6D,0x00);
SPI3_9bit_WWR_DAT(0xA5);

SPI3_9bit_WWR_CMD(0x6C,0x00);
SPI3_9bit_WWR_DAT(0x08);

SPI3_9bit_WWR_CMD(0x0E,0x00);
SPI3_9bit_WWR_DAT(0x0A);

SPI3_9bit_WWR_CMD(0x3E,0x00);
SPI3_9bit_WWR_DAT(0x32);

SPI3_9bit_WWR_CMD(0x41,0x00);SPI3_9bit_WWR_DAT(0x72);
SPI3_9bit_WWR_CMD(0x41,0x01);SPI3_9bit_WWR_DAT(0x63);
SPI3_9bit_WWR_CMD(0x41,0x02);SPI3_9bit_WWR_DAT(0xD5);
SPI3_9bit_WWR_CMD(0x41,0x03);SPI3_9bit_WWR_DAT(0x43);
SPI3_9bit_WWR_CMD(0x41,0x04);SPI3_9bit_WWR_DAT(0x55);
SPI3_9bit_WWR_CMD(0x41,0x05);SPI3_9bit_WWR_DAT(0x04);
```

16. HSF COMPLIANCE

●.This products complies with ROHS 2011/65/EU and 2015/863/EU、REACH 1907/2006/EC requirements, and the packaging complies with 94-62-EC.

AVDISPLAY

Work Instruction

Inspection Criterion for TFT Products

Doc. No.	AVD（WI）-00-QA-048	Prepared by	
Version	V1.1	Checked by	
Pages	10	Customer approval	
Effective date		Released No.	
Controlled Document		Keeping Properly	

1. Objective

The TFT test criterion are set to formalize TFT quality standards for AVD with reference to those of the customer for inspection, release and acceptance of finished TFT products in order to guarantee the quality of TFT products required by the customer.

2. Scope

The criterion is applicable to all the TFT products manufactured by AVD.

3. Equipment for Inspection

Electrical tester, electrical testing machines, vernier calipers, microscopes, magnifiers, anti-static wrist straps, finger cots/gloves, labels, tri-phase cold and hot shock machine, constant temperature and humidity chamber, backlight table, ovens for high-low temperature experiments, refrigerators, constant voltage power supply (DC) , desk Lamps, etc.

4. Sampling Plan and Reference Standards

4.1 Sampling plan:

Refer to National Standard GB/T 2828.1---2012/ISO2859-1:1999，level II of normal levels:

Product Category	Non-Consumer Electronics	Industrial	Automobile
AQL	MA=0.4 MI=1.5	MA=0.25 MI=0.65	MA=0.15 MI=0.40

4.2 GB/T 2828.1---2012/ISO2859-1:1999 Sampling check procedure in count

4.3 GB/T 18910. Standard for LCM parts

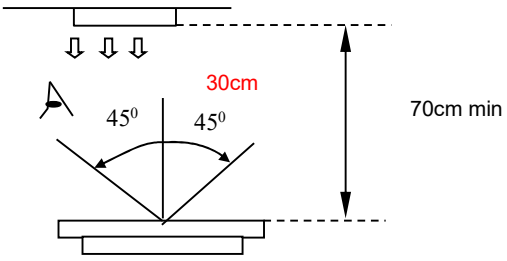
4.4 GB/T24213-2008 Basic Environmental Test Procedures for Electrical and Electronic Products

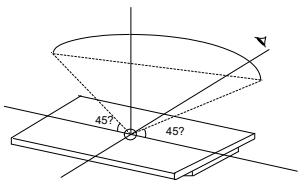
4.5 IPC-A-610E Acceptability of Electronic Assemblies

5. Inspection Conditions and Inspection Reference

5.1Cosmetic inspection: shall be done normally at 23±5℃ of the ambient temperature and45~75%RH of relative humidity, under the ambient luminance between 500lux~700lux and at the distance of 30cm apart between the inspector’s eyes and the LCD panel and normally in reflected light. For backlight LCM, cosmetic inspection shall be done under the ambient luminance between 200lux~500lux with the backlight on.

5.2 The TFT shall be tested at the angle of 45°left and right and 0-45° top and bottom as the following picture showing:





5.3 Definition of viewing area (VA)

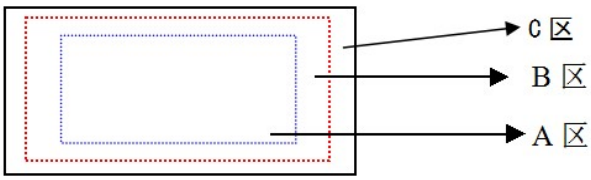
A area：Active area（AA area）

B area: Viewing area（VA area）

C area: Non-viewing area（not viewing after customer assembly）

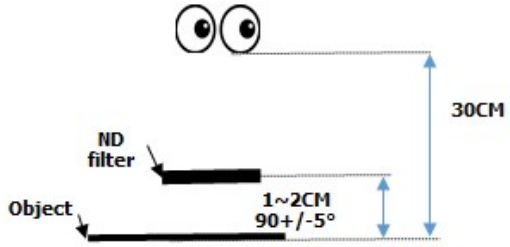
If there is any appearance viewing defect which do not affect product quality and customer assembly in C area, it's accepted in generally.

The criteria apply to A and B area except chipping and crack.



5.4 Inspection with naked eyes(exclusive of the inspection of the physical dimensions of defects carried out with magnifiers)

5.5 ND card use method(refer to below image) and scope: Multi-bright dot; Mura(Black/Gray pattern uneven); dark line and so on.



5.6 Undefined items or other special items, refer to mutual agreement and limited sample. If criterion does not match product specifications/ technical requirement, both should be subject to special inspection criterion agreed by customer.

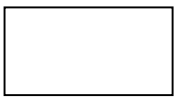
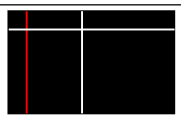
6. Defects and Acceptance Standards

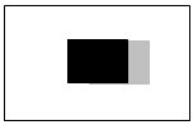
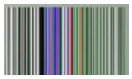
6.1 Electrical properties test

6.1.1 Test voltage(V)：Refer to the instruction of testers and the product specification or drawing and the display content and parameters and display effects shall conform to the product specification and drawing.

6.1.2 Current Consumption(I)：Refer to approved product specifications or drawings.

6.1.3 Function items(Defect category MA)

No.	Defects	Descriptions	Pictures	Inspection method/tools	Defect category
6.1.3.1	No display /reaction	shows no picture/display in normal connected situation.		Naked eyes/ testers	MA
6.1.3.2	Missing segment	Shows missing lines in normal display		Naked eyes/ testers	MA
6.1.3.3	Dark line	Only visible on gray pattern, 1 or more vertical/horizontal lines: 5%ND, not visible, OK	/	Naked eyes/ testers	MA

6.1.3.4	POL angle defect	Not accepted		Naked eyes/ testers	MA
6.1.3.5	Image retention (sticking)	Chess pattern stays for 2mins and change to 50% gray pattern, disappear in 30s, OK; if time>30s, NG		Naked eyes/ testers	MA
6.1.3.6	Display abnormal	Not accepted		Naked eyes/ testers	MA
6.1.3.7	Cross-talk	Refer to AVD specification	/	Naked eyes/ limited sample	MA
6.1.3.8	Display dim/bright	Refer to limited sample	/	Naked eyes/ limited sample	MA
6.1.3.9	Contrast	Refer to limited sample	/	Naked eyes/ limited sample	MA
6.1.3.10	Huge current	Out of spec, not accepted	/	Ammeter	MA
6.1.3.11	TP function defect	Not accepted	/	Naked eyes/ Touch/ test program	MA

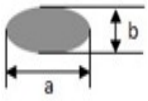
6.2 LCD dot/line defect

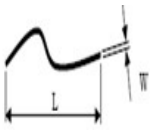
6.2.1 LCD pixel dot defect(defect category：MI)

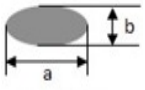
Item	**Inspection criterion**			
Size	S ＜5”	5≤S＜10”	10≤S＜15”	S≥15”
Single bright dot(RGB dot) quantity	1	2	2	3
2 connected bright dot quantity	0	1	1	1
3 connected bright dot or more quantity	0	0	0	0
Bright dot total quantity	1	2	3	4
Single dark dot quantity	2	3	4	5
2 connected dark dot quantity	1	1	2	2
3 connected dark dot or more quantity	0	0	0	0
Dark dot total quantity	3	4	5	6
Multi-bright dot quantity	ND 5％hidden, OK			

Item	**Inspection criterion**
Remark：2 bright dots distance DS≥15mm　2 dark dots distance DS≥5mm 1）Bright dot：Power on TFT and RGB dot in black display and size ≧1/2dot; or bright dot in RGB display 2）Dark dot：Power on TFT and gray or black dot in RGB display and size ≧1/2dot 3）Multi-bright dot：Power on TFT and fluorescent tiny dot in black display(only visible in black display) and single dot size<1/2dot	

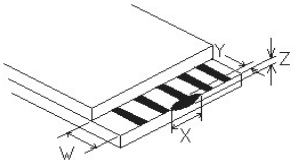
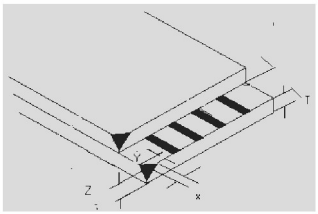
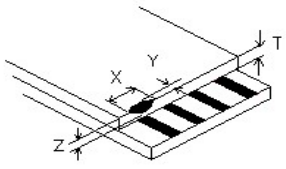
6.2.2 LCD appearance dot defect (defect category：MI)

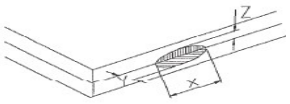
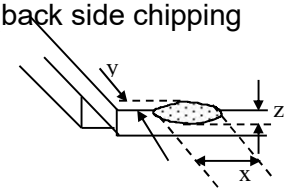
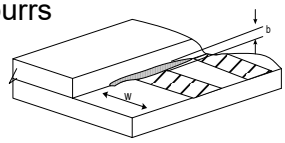
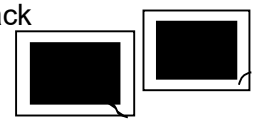
No.	**Item**	**Inspection criterion**					Picture	Inspection method/tools
		Size	S ＜5”	5≤S＜10”	10≤S＜15”	S≥15”		
6.2.2.1	Dot defect (black dot, white dot，particle)	D≤0.15	ignore	ignore	D≤0.2; Not count	D≤0.2; ignore	 D=(a+b)/2	Naked eyes /film card /magnifier
		0.15＜D≤0.25	3	3				
		0.25＜D≤0.30	1	2	0.2~0.35 Q’ty ≤4	0.2~0.35 Q’ty ≤ 5		
		0.30＜D≤0.35	0	1				
		0.35＜D≤0.50	0	0	1	2		
		D＞0.5	0	0	0	0		
		Remark: D≤0.15mm, not count. Multi-dot as bulk is not accepted. Count dot quantity≤ 5; 2 round dots or linear dots in 1 cm is judged as multi-dot.						

No.	**Item**	Length (mm)	Width (mm)	S ＜5”	5≤S＜10”	10≤S＜15”	S≥15”	Picture	Inspection method/tools
6.2.2.2	Line defect (visible when power on)	Not count	W≤0.03	Ignored	Ignored	Ignored	Ignored		Naked eyes /film card /magnifier
		L≤5	0.03≤W＜0.05	3	3	Ignored	Ignored		
		L≤5	0.05≤W＜0.08	0	1	3	3		
		L≤8	0.05≤W＜0.08	0	0	1	2		
		L＞8	W＞0.08	0	0	0	0		
		Remark：Invisible when power on, only visible in special angle against light, show as watermark/folding/scratch but can not be touched, no control or refer to keeping sample.							

6.2.2.3	Polarizer scratch/ Dent/ bubble defect, particle on polarizer	Size(mm)	S ＜5”	5≤S＜10”	10≤S＜15”	S≥15”		Naked eyes /film card /magnifier
		D≤0.20	Ignored	Ignored	Ignored	Ignored		
		0.20＜D≤0.5	2	2	3	5		
		0.50＜D≤0.8	0	1	2	3		
		0.8＜D≤1.5	0	0	1	2		
		D＞1.5mm	0	0	0	0		

6.3 Chipping defect

No.	Item	Accepted criterion(mm)				MAJ	MIN
6.3.1	ITO conductive side 	X	/	≤1/8L	/		√
		Y	Y≤1/6W	1/6W <Y≤1/4W	1/4W <Y		
		Accept	2	2	0		
6.3.2	Corner chipping (ITO pins position)	X	/	≤1/6L	/		√
		Y	Y≤1/2W	1/2W <Y≤W	W <Y		
		Accept	2	1	0		
		Corner chipping occurred in sealed edge position as per 6.3.3; at the same time it should not enter into black border of the frame and the corner chipping effect the electric connection position perform as per 6.3.1.					
6.3.3	Chipping in sealed area (outside chipping) 	X	/	≤1/8L	/		√
		Y (outside chipping)	Not enter into sealant	Enter Y≤H	H<Y		
		Y (inside chipping)		Enter Y≤1/2H	1/2H<Y		
		Z	≤T	≤1/2T	/		
		Accept	2	1	0		

	 Chipping in sealed area (inside chipping)	The standards of inner and outer chipping on edge sealing area are same. When the chipping occurred in the opposite of stage, Y as per the chipping on the non-conduction side standard in 6.3.1					
6.3.4	conductive side (back side chipping 	X	/	≤1/6L	/		√
		Y	Y≤1/3W	1/3W <Y≤2/3W	2/3W <Y		
		Accept	2	2	0		
		Chipping into ITO side ,refer to 6.3.1					
6.3.5	Protruding LCD poor cutting and LCD burrs 	X	/	≤1/8L	/		√
		Y	≤1/6W	1/6W <Y≤1/5W	1/5W <Y		
		Z	/	/	/		
		Accept	1	1	1		
		the outside protruding control as per the tolerance of drawing.					
6.3.6	Crack 	Not allow to occur cracks without direction; the crack expand to inside is NG, but to outside is OK (confirmed as per the damaged standard)					√
Remark:1)X means the length of chipping; Y means the width; Z means the thickness; W means the step width of the two glasses; H means the distance from the glass edge to the seal inner edge; t means glass thickness.							

6.4 Backlight components

No.	Item	Description	Accepted criterion	MAJ	MIN
6.4.1	No backlight wrong Color	/	Rejected	√	
6.4.2	Color deviation	When powered on, the LCD color differs from its sample and found that the color not conforming to the drawing after testing.	Refer to sample and drawing.		√
6.4.3	Brightness deviation	When powered on, the LCD brightness differs from its sample and is found after testing not conforming to the drawing; or if it conforms to the drawing but the brightness over ±40% than its typical	Refer to sample and drawing.		√

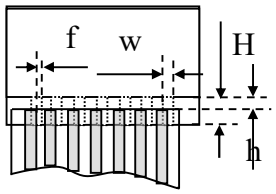
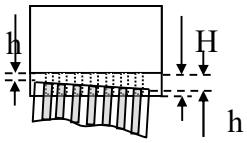
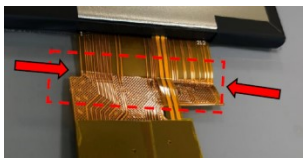
		value.			
6.4.4	Uneven brightness	Uneven on the same LCD and out of the specification of the drawing. The no specification evenness= (the max value-the min value)/ mean value< 70%.	Refer to sample and drawing.		√
6.4.5	Spot/line /scratch	When power on, it has dirty spot, scratches and so on spot and line defects.	Refer to 6.2.2		√

6.5 Metal frame (Metal Bezel)

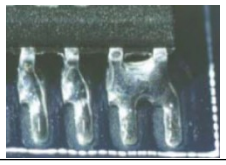
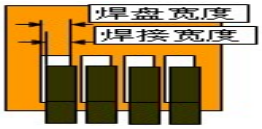
No.	Item	Description	Accepted criterion	MAJ	MIN
6.5.1	Material & surface treatment	Metal frame/surface treatment do not conform to the specifications.	Rejected	√	
6.5.2	Tab twist Unconformity/ Tab not twisted	Wrong twist method or direction and twist tabs are not twisted as required.	Rejected	√	
6.5.3	Bezel paint loss	1.Front surface: Paint peel off and scratch to the bottom Dot:D≤0.5mm, exceeds 3; Line:L≤3.0mm,W≤0.05mm exceeds 2; 2.Front dent, air bubble and side with paint peeling off scratch to the bottom Dot: D≤1.0mm, exceeds 3; Line:L≤10.0mm,W≤0.05mm, exceeds 2;	Rejected		√
6.5.4	Bezel scratch				√
6.5.5	Painting peel off, discoloration, dent, and scratch				√
6.5.6	Burr	Burr(s) on metal bezel is so long as to get into viewing area.	Rejected		√

6.6 FPC

No.	Item	Description	Accepted criterion	MAJ	MIN
6.6.1	Model & P/N	Material model & P/N	Keep the same with drawing and technical requirement	√	

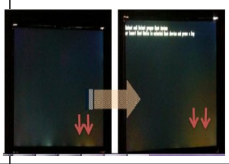
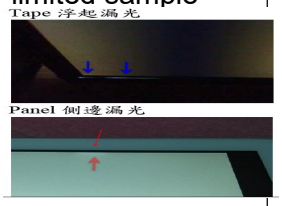
6.6.2	Dimension/ position	Dimension in drawing spec  Remark：H=ITO pin length f=FPC width W=ITO pin width	f≤1/3w，h ≤1/3H，dimension in drawing spec-> OK Conducive material and ITO/PDA connective area must over than 1/2. Entire dimension must be in spec tolerance. 		√
6.6.3	FPC appearance	Hot pressing material get broken, folding line open; FPC golden finger oxidate, broken ,scratch ,foreign material which cause line short	Broken length<2mm; FPC line is OK- > Accepted Crack and line broken-> Rejected		√
6.6.4	FPC burr	Burr near FPC edge area	When cover line and burr length ≤1.0mm->Accepted		√
6.6.5	FPC falling off	FPC bonding area falling off ; silica gel breaking	Rejected		√
6.6.6	Sealant missing ITO line	Sealant is not covered all ITO line	Rejected	√	
6.6.7	Missing sealant	No sealant	Rejected	√	
6.6.8	Sealant	Sealant height > product total height	Rejected	√	
6.6.9	FPC folding 	FPC folding as below photo and function is OK->Accept 	Accept		√
6.6.10	FPC connecting fingers dent/scratch/ stain	FPC connecting fingers dent/scratch/ stain as below photo and function is OK->Accept 	Accept		√

6.7 SMT

No.	Item	Description	Accepted criterion	MAJ	MIN
6.7.1	Soldering bridge	Solder between adjacent pads and components 	Rejected		√
6.7.2	Solder ball/splash	Solder ball/tin dross causing short circuit at the solder point. There are active solder ball and splash.	Rejected		√
6.7.3	Soldering excursion	Soldering slant > 1/3 soldering pad 	Rejected		√
6.7.4	Component wrong attaching	Component on PCB differs with drawing: wrong one, extra one, lack one, opposite polarity	Rejected	√	
		JUMP short circuit on PCB: extra soldering ,lack soldering.	Rejected	√	
6.7.5	Component falling off	Soldering but component is missing	Rejected	√	
6.7.6	Wrong component	Component model/spec differs from product specification	Rejected	√	

6.8 General Appearance

No.	Item	Description	Accepted criterion	MAJ	MIN
6.8.1	Protective film scratch/bubble	Protective film scratch/bubble is OK	Accepted	√	
6.8.2	Surface stain	Defect mark or label are not removed residual glue, and finger print,etc；	Accepted		√
6.8.3	Product label	Readable even unclear or misplaced part	Accepted		√
6.8.4	Component mark	Silk screen mark clear, resistance measured value in spec	Accepted		√
6.8.5	Newton’s rings	Area<1/6 screen area&quantity≤1	Accepted		√

6.8.6	Mura 	1.In black/gray display ND 3% invisible ->OK; visible->NG 2.Naked eyes inspection RGB display invisible Black display, area<1/4 screen area	Accepted		√
6.8.7	Light leak	1.LCD edge(near backlight) shadow by LCD lamps irregular illuminate 2.Judge in black/white/gray display (slight leaky is yellowish, greenish, bluefish ->NG）；	Refer to limited sample 		√
6.8.8	Polarizer	1.Polarizer slant.Cover AA and not over LCD edge 2.No unmovable stain or finger print in polarizer AA 3.Bubble/warped but not enter AA	Accepted		√
6.8.9	TP defect	TP stain(fogy&unremovable)	Accepted		√

Remark：Anything which is not clearly defined in 6.5~6.8 should refer to IPC-A-610. Non-consumer Electronics refer to class 1 and Industrial, Automobile refer to Class 2.

7. Others

Items not specified in this document or released on compromise should be inspected with reference to mutual agreement and limit samples.