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AVDISPLAY

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SPECIFICATION FOR TFT MODULE

MODULE NO. : AVD-TT24QV-NN-014-S

CUSTOMER NO. :

Rev No. : C

AVD	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE	沈翱翔		宋波玉
DATE	2024.10.30	2024.10.30	2024.10.30

CUSTOMER APPROVAL	SIGNATURE	DATE

Notes :

- 1、Please contact AVD before assigning your product based on this module specification.
- 2、To improve the quality of product, and this product specification is subject to change without any notice.



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1. GENERAL INFORMATION

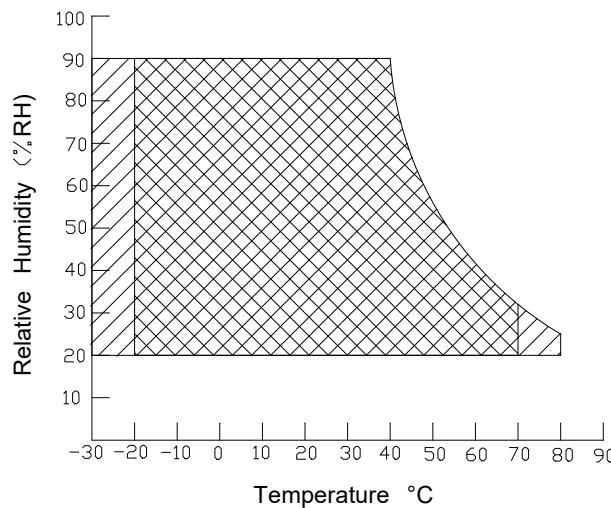
No.	Item	Contents	Unit
1	LCD size	2.4 inch (Diagonal)	/
2	Display mode	Normally black/Transmissive/Anti-glare	/
3	Viewing direction(eye)	FREE	/
4	Gray scale inversion direction	-	/
5	Resolution(H*V)	240*320 Pixels	/
6	Module size (L*W*H)	42.72*58.50*2.15	mm
7	Active area (L*W)	36.72*48.96	mm
8	Pixel pitch (L*W)	0.153*0.153	mm
9	Interface type	MCU 8bit interface	/
10	Color Depth	262K	/
11	Module power consumption	0.260(Appr)	W
12	Back light type	EDGE&WHITE	/
13	Driver IC	ST7789P3-G6 OR COMPATIBLE	/
14	Weight	25(Appr)	G

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Power supply input voltage for TFT	VDD	-0.3	4.6	V	
Backlight current (normal temp.)	ILED	-	100	mA	
Operation temperature	Top	-20	+70	°C	Note1
Storage temperature	Tst	-30	+80	°C	Note1
Humidity	RH	-	90%	RH	Note1

Note1 :

- 1).The relative humidity and temperature range are as below sketch,90%RH Max.
- 2).The maximum wet bulb temperature $\leq 40^{\circ}\text{C}$ and without dewing.



Operating Range  Storage Range  + 

3. ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS(at Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply input voltage	VDD	2.6	2.8	3.0	V	
I/O logic voltage	VDDIO	-	1.8	-	V	
Input voltage 'H' level	VIH	0.7VDDIO	-	VDDIO	V	
Input voltage 'L' level	VIL	VSS	-	0.3VDDIO	V	
Power supply current	IVDD	-	7	-	mA	
TFT gate on voltage	VGH	-	-	-	V	
TFT gate off voltage	VGL	-	-	-	V	
Analog power supply voltage	AVDD	-	-	-	V	
TFT common electrode voltage	VCOM	-	-	-	V	Note1

Note1 : The value is just the reference value. The customer can optimize the setting value by the different D-IC
 VCOM must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..

4. BACKLIGHT CHARACTERISTICS

(at Ta=25°C, RH=60%)

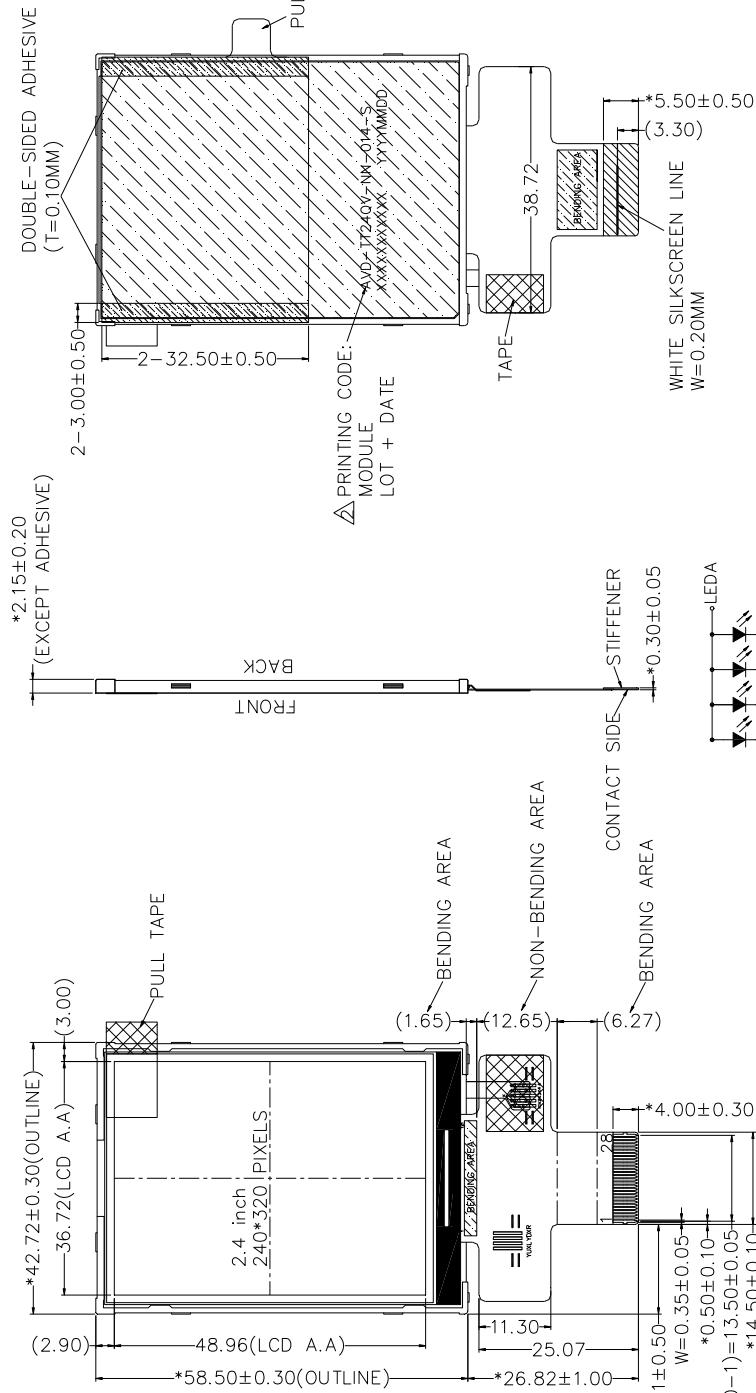
Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED forward voltage	VF	2.7	3.0	3.3	V	
LED forward current	IF	-	80	-	mA	IF=20*4mA
LED power consumption	PLED	-	0.24	-	W	Note1
Number of LED	-		4		PCS	
Connection mode	-	1 in series	4 in parallel		/	
LED life-time	-	20000	-	-	Hrs	Note2

Note1 : Calculator value for reference : IF*VF = PLED

Note2 : The LED life-time define as the estimated time to 50% degradation of initial brightness at Ta=25°C and IF =80mA. The LED lifetime could be decreased if operating IF is larger than 80mA.

5. EXTERNAL DIMENSIONS

REV.	SYMBOL	DESCRIPTION	5	NAME	6	DATE
O		FIRST ISSUE		桂 雷		DEC-31-2021
A	△	UPDATE BACKLIGHT		桂 雷		APR-19-2022
B	△△	CHANGE IC; ADD INK-JET PRINTING CODE		覃 威		DEC-09-2022



6. ELECTRO - OPTICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time	Tr+ Tf	-	-	35	45	ms	FIG.1	Note 1
Contrast ratio	Cr		900	1100	-	-	FIG.2	Note 2
Surface luminance	Lv	$\theta=0^\circ$	320	400	-	cd/m ²	FIG.2	Note 3
Luminance uniformity	Yu	$\theta=0^\circ$	75	80	-	%	FIG.2	Note 4
NTSC	-	$\theta=0^\circ$	-	70	-	%	FIG.2	Note 5
Viewing angle	θ	$\emptyset=90^\circ$	70	80	-	deg	FIG.3	Note 6
		$\emptyset=270^\circ$	70	80	-	deg	FIG.3	
		$\emptyset=0^\circ$	70	80	-	deg	FIG.3	
		$\emptyset=180^\circ$	70	80	-	deg	FIG.3	
CIE (x,y) chromaticity	Red x	$\theta=0^\circ$ $\emptyset=0^\circ$ $Ta=25^\circ C$	Typ -0.04	0.64	Typ +0.04	-	FIG.2 CIE1931	Note 5
	Red y			0.34		-		
	Green x			0.32		-		
	Green y			0.61		-		
	Blue x			0.15		-		
	Blue y			0.06		-		
	White x			0.30		-		
	White y			0.33		-		

Note1. Definition of response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%. For additional information see FIG1.

Note2. Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula.

For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Measured at the center area of the LCD

Note3. Definition of surface luminance

Surface luminance is the luminance with all pixels displaying white.

For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ……,Pn)

Note4. Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

$$Yu = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,……,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,……,Pn)}}$$

Note5. Definition of color chromaticity (CIE1931)

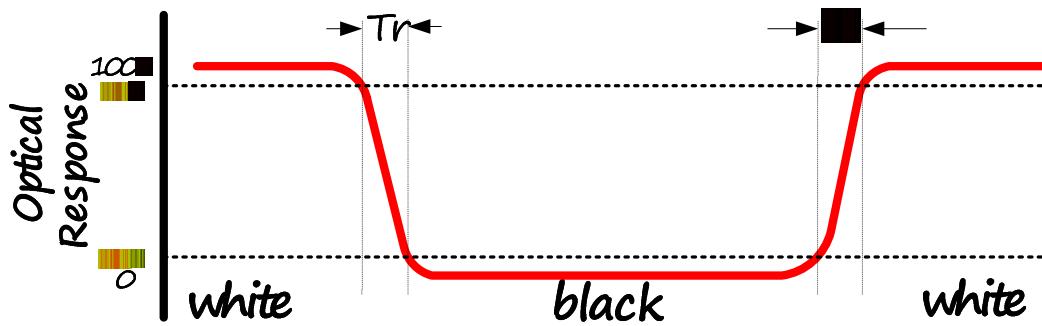
CIE (x,y) chromaticity, The x,y value is determined by screen active area center position P5. For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.

For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE, the testing data is base on TOPCON's BM-5or BM-7 photo detector or compatible.

FIG.1. The definition of response Time

FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

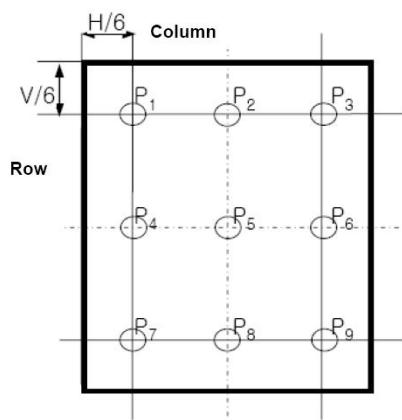
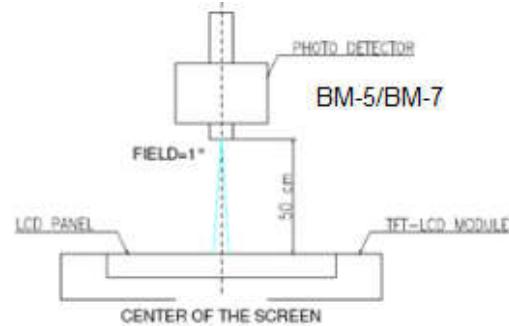
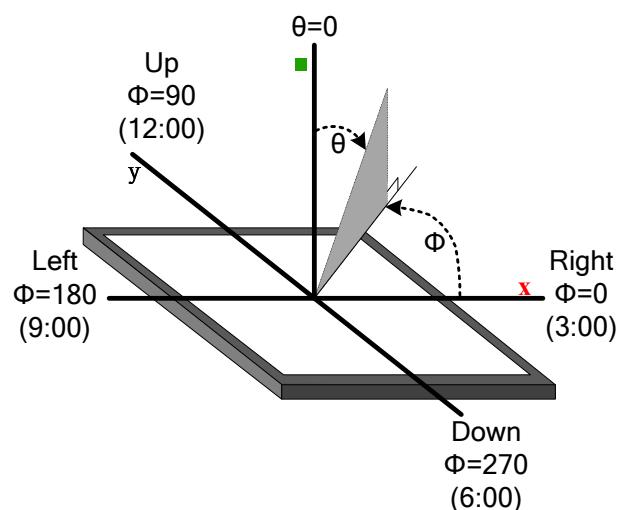
Note : The TFT module should be stabilized at a given temperature for 10 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 10 minutes in a windless room.

H,V : Active area

Light spot size $\varnothing=1.5\text{mm}$ (BM-7)50cm distance or compatible distance from the LCM surface to detector lens.

Test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-7 or compatible ,see Figure b.


Figure a

Figure b
FIG.3. The definition of viewing angle


7. INTERFACE DESCRIPTION

Module Interface description

Interface No.	Name	I/O or connect to	Description																																													
1	YU	I/O	Y-Up																																													
2	XL	I/O	X-Left																																													
3	YD	I/O	Y-Bottom																																													
4	XR	I/O	X-Right																																													
5	IM3	I	<table border="1" style="margin-left: 20px;"> <tr> <th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>80-8bit parallel I/F</td><td>DB[7:0]</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>0</td><td>80-9bit parallel I/F</td><td>DB[8:0]</td></tr> <tr> <td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-line 9bit serial I/F</td><td>SDA: in/out</td></tr> <tr> <td>2 data lane serial I/F</td><td>SDA: in/out WRX: in</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>0</td><td>4-line 8bit serial I/F</td><td>SDA: in/out</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>1</td><td>3-line 9bit serial I/F II</td><td>SDA: in SDO: out</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>0</td><td>4-line 8bit serial I/F II</td><td>SDA: in SDO: out</td></tr> </table>	IM3	IM2	IM1	IM0	MPU Interface Mode	Data pin	0	0	0	0	80-8bit parallel I/F	DB[7:0]	0	0	1	0	80-9bit parallel I/F	DB[8:0]	0	1	0	1	3-line 9bit serial I/F	SDA: in/out	2 data lane serial I/F	SDA: in/out WRX: in	0	1	1	0	4-line 8bit serial I/F	SDA: in/out	1	1	0	1	3-line 9bit serial I/F II	SDA: in SDO: out	1	1	1	0	4-line 8bit serial I/F II	SDA: in SDO: out	
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1	1	1	0	4-line 8bit serial I/F II	SDA: in SDO: out																																											
6	IM2	I																																														
7	IM1	I																																														
8	IM0	I																																														
9	VDDI	P	Power for LCD																																													
10	RESET	I	Chip reset pin																																													
11	CS	I	Chip selection pin																																													
12	SCL	I	Display data/command selection pin in parallel interface.																																													
13	DCX	I	Write enable in MCU parallel interface																																													
14	RD	I	Read enable in 8080 MCU parallel interface																																													
15	SDA	I/O	When IM3: Low, SPI interface input/output pin. When IM3: High, SPI interface input pin																																													
16-23	DB0~DB7	I/O	Data bus																																													
24	VDD	P	Power for LCD																																													
25	GND	P	Power Ground																																													
26	LEDA	P	Power for LED backlight(Anode)																																													
27	LEDK	P	Power for LED backlight(Cathode)																																													
28	NC	/	/																																													

I: input, O: output, P: Power, NC: No connection

8.AC CHARACTERISTICS

8080 Series MCU Parallel Interface Characteristics: 9/8-bit Bus

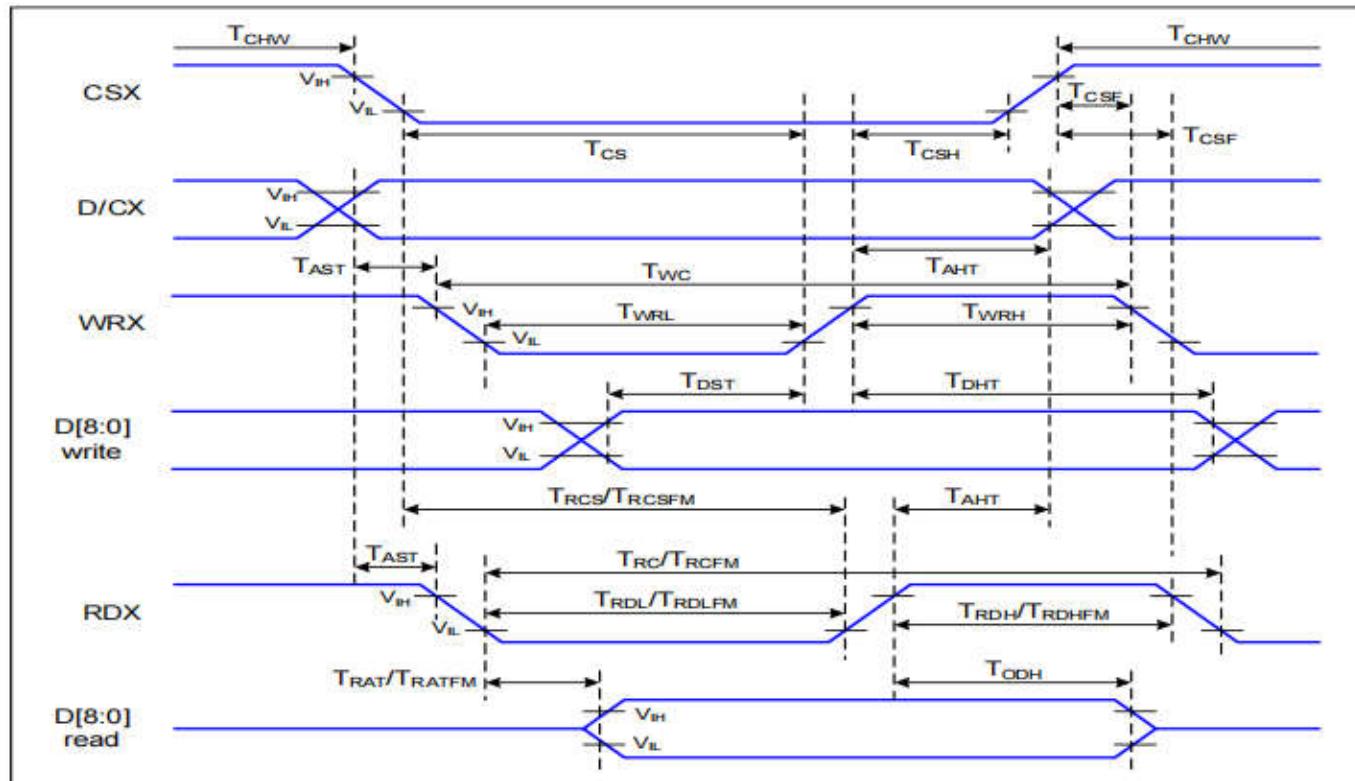
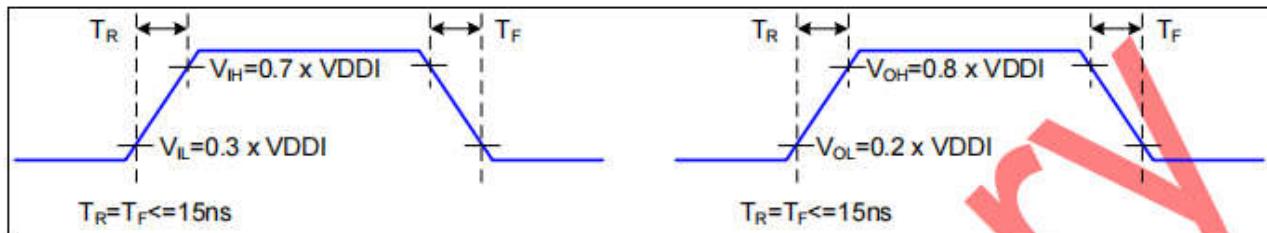
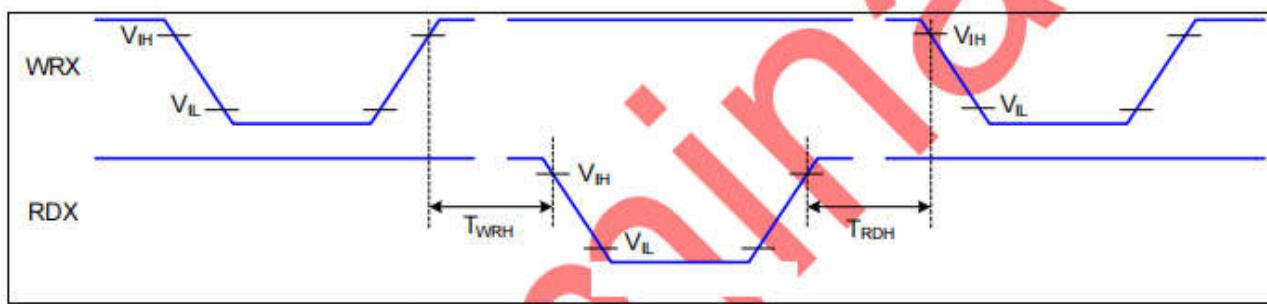


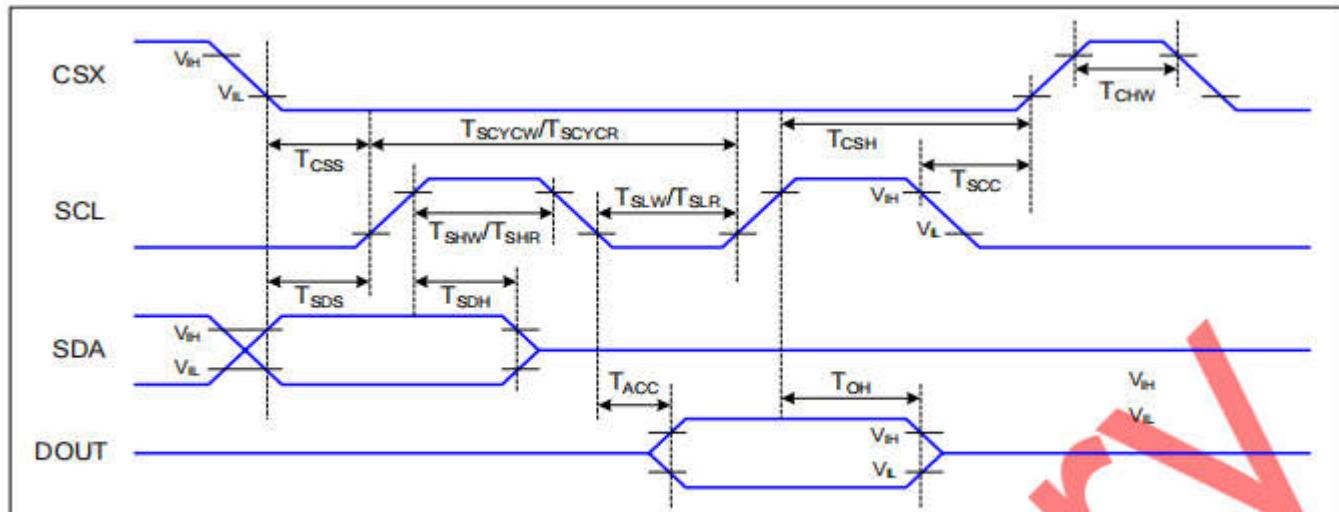
Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T _{AST}	Address setup time	0	-	ns	-
	T _{AHT}	Address hold time (Write/Read)	10	-	ns	
CSX	T _{CHW}	Chip select "H" pulse width	0	-	ns	-
	T _{CS}	Chip select setup time (Write)	15	-	ns	
	T _{TRCS}	Chip select setup time (Read ID)	45	-	ns	
	T _{TRCSFM}	Chip select setup time (Read FM)	355	-	ns	
	T _{CSE}	Chip select wait time (Write/Read)	10	-	ns	
WRX	T _{CSH}	Chip select hold time	10	-	ns	-
	T _{WC}	Write cycle	66	-	ns	
	T _{WRH}	Control pulse "H" duration	15	-	ns	
RDX (ID)	T _{WRH}	Control pulse "L" duration	15	-	ns	When read ID data
	T _{RC}	Read cycle (ID)	160	-	ns	
	T _{RDH}	Control pulse "H" duration (ID)	90	-	ns	
RDX (FM)	T _{RDH}	Control pulse "L" duration (ID)	45	-	ns	When read from frame memory
	T _{RCFM}	Read cycle (FM)	450	-	ns	
	T _{RDHFM}	Control pulse "H" duration (FM)	90	-	ns	
	T _{RDHFM}	Control pulse "L" duration (FM)	350	-	ns	
D[8:0]	T _{DST}	Data setup time	10	-	ns	For CL=30pF

	T_{DHT}	Data hold time	10	-	ns	
	T_{RAT}	Read access time (ID)	-	40	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Table 4 8080 Parallel Interface Characteristics

Figure 2 Rising and Falling Timing for I/O Signal

Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (T_r, T_f) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Serial Interface Characteristics (3-line serial):

Figure 4 3-line serial Interface Timing Characteristics



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T _{css}	Chip select setup time (write)	15	-	ns	-
	T _{csh}	Chip select hold time (write)	15	-	ns	
	T _{css}	Chip select setup time (read)	60	-	ns	
	T _{scc}	Chip select hold time (read)	65	-	ns	
	T _{chw}	Chip select "H" pulse width	40	-	ns	
SCL	T _{scycw}	Serial clock cycle (Write)	16	-	ns	-
	T _{shw}	SCL "H" pulse width (Write)	7	-	ns	
	T _{slw}	SCL "L" pulse width (Write)	7	-	ns	
	T _{scycr}	Serial clock cycle (Read)	150	-	ns	
	T _{shr}	SCL "H" pulse width (Read)	60	-	ns	
	T _{slr}	SCL "L" pulse width (Read)	60	-	ns	
SDA (DIN)	T _{sds}	Data setup time	7	-	ns	-
	T _{sdh}	Data hold time	7	-	ns	
DOUT	T _{acc}	Access time	10	50	ns	For maximum CL=30pF
	T _{oh}	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note1 : The rising time and falling time (T_r , T_f) of input signal are specified at 15ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Note2 : In the read sequence of Serial interface, the 500nsec delay time is needed between read command and first read clock.

Serial Interface Characteristics (4-line serial):

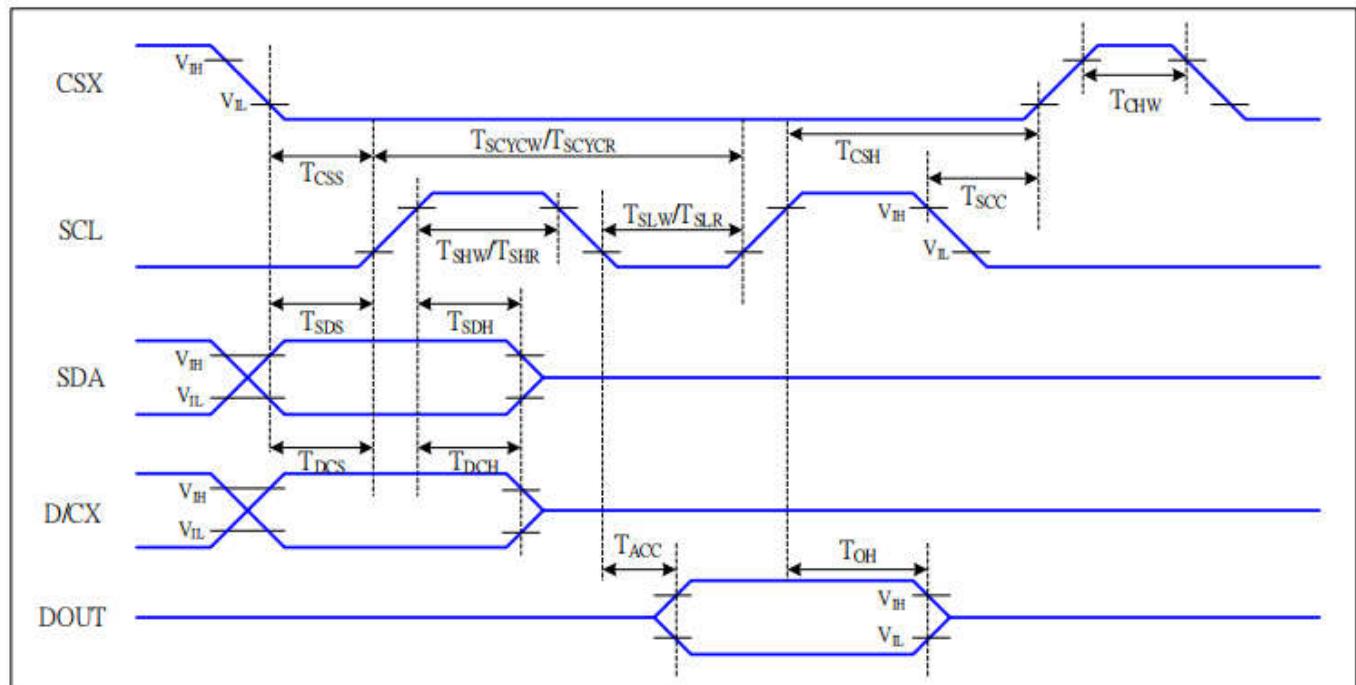


Figure 5 4-line serial Interface Timing Characteristics



$VDDI=1.65$ to $3.3V$, $VDD=2.4$ to $3.3V$, $AGND=DGND=0V$, $Ta=25^\circ C$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T _{css}	Chip select setup time (write)	15	-	ns	
	T _{csh}	Chip select hold time (write)	15	-	ns	
	T _{css}	Chip select setup time (read)	60	-	ns	
	T _{scs}	Chip select hold time (read)	65	-	ns	
	T _{ch}	Chip select "H" pulse width	40	-	ns	
SCL	T _{scycw}	Serial clock cycle (Write)	16	-	ns	-write command & data ram
	T _{shw}	SCL "H" pulse width (Write)	7	-	ns	
	T _{slw}	SCL "L" pulse width (Write)	7	-	ns	
	T _{scyrc}	Serial clock cycle (Read)	150	-	ns	-read command & data ram
	T _{shr}	SCL "H" pulse width (Read)	60	-	ns	
	T _{slr}	SCL "L" pulse width (Read)	60	-	ns	
D/CX	T _{dcs}	D/CX setup time	10	-	ns	
	T _{dch}	D/CX hold time	10	-	ns	
SDA (DIN)	T _{sds}	Data setup time	7	-	ns	
	T _{sdh}	Data hold time	7	-	ns	
DOUT	T _{acc}	Access time	10	50	ns	For maximum CL=30pF
	T _{oh}	Output disable time	15	50	ns	For minimum CL=8pF

Table 6 4-line serial Interface Characteristics

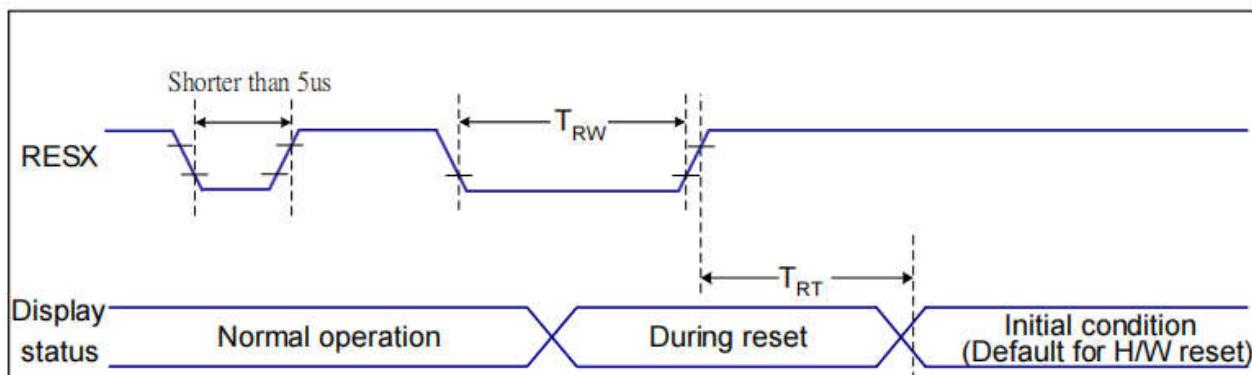


Figure 7 Reset Timing

$VDDI=1.65$ to $3.6V$, $VDD=2.4$ to $3.6V$, $AGND=DGND=0V$, $Ta=25^\circ C$

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 8 Reset Timing



9. POWER SEQUENCE

To prevent the device damage from latch up and Improve subjective display effect, the power ON/OFF sequence shown below must be followed.

VDDI and VDD can be applied in any order.

In CABC function application, VDDI power on need delay 5ms after VDD has been supplied.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec

after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after

RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

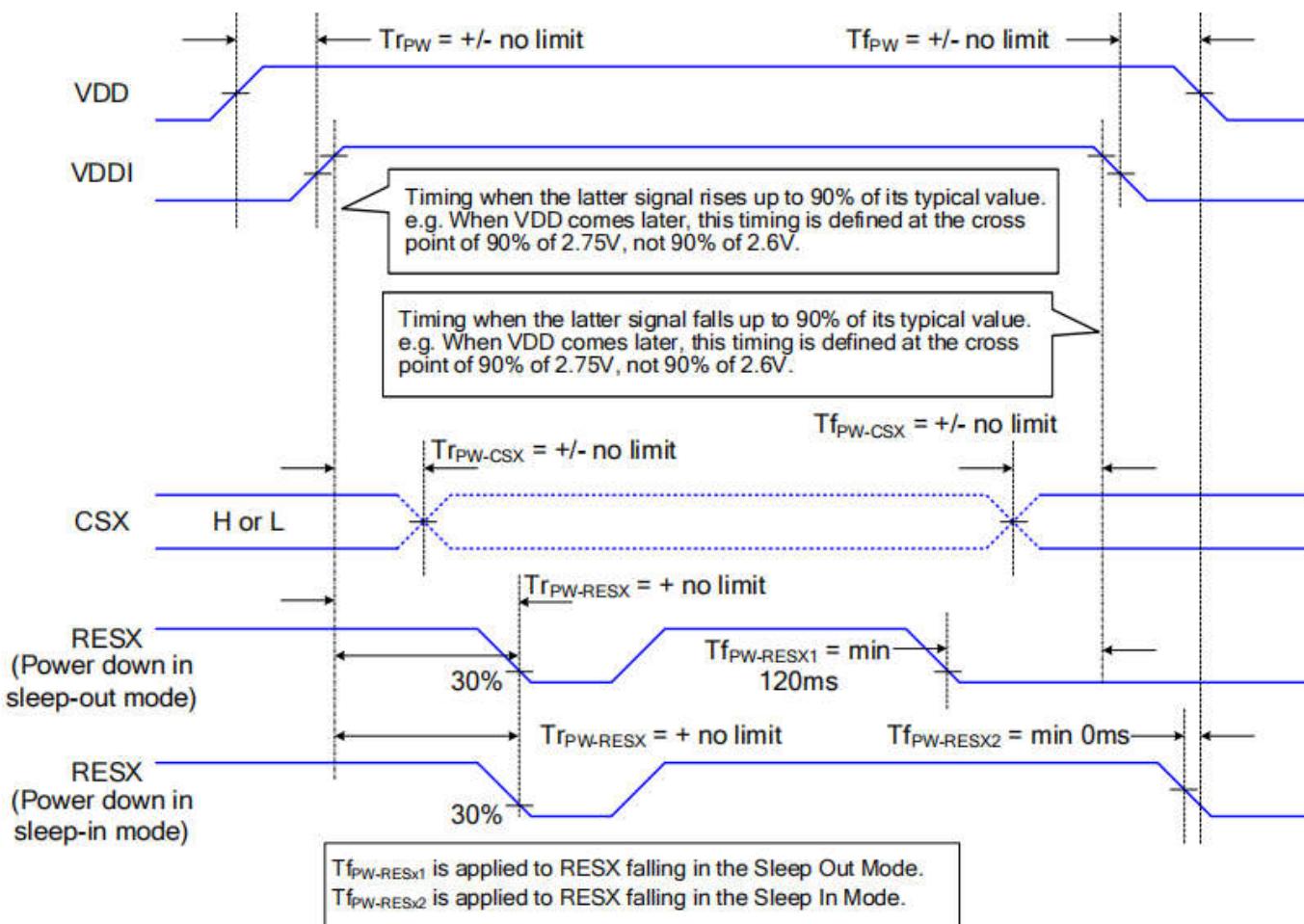
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:



10. RELIABILITY TEST CONDITIONS

No.	Test item	Test condition		Inspection after test	
11.1	High temperature storage test	+80°C/240 hours		Inspection after 2~4hours storage at room temperature, the sample shall be free from defects : 1. Current changing value before test and after test is 50% larger; 2. Function defect : Non-display, abnormal display, missing lines, Short lines, ITO corrosion; 3. Visual defect : Air bubble in the LCD, Seal leak, Glass crack.	
11.2	Low temperature storage test	-30°C/240 hours			
11.3	High temperature operating test	+70°C/120 hours			
11.4	Low temperature operating test	-20°C/120 hours			
11.5	Temperature cycle storage test	-30°C ~ 25°C ~ +80°C/10cycles (30min.) (10min.) (30min.)			
11.6	High temperature high humidity test	+50°C*90% RH/120 hours			
11.7	Vibration test	Frequency : 250 r/min Amplitude : 1 inch Time: 45min			
11.8	Drop test	Drop direction: 1 corner/3 edges/6 sides 10 times			
		Packing weight(kg)	Drop height(cm)		
		<11	80±1.6		
		11≤G<21	60±1.2		
		21≤G<31	50±1.0		
		31≤G<40	40±0.8		
11.9	ESD test	Air discharge: ±8KV, 10times Contact discharge: ±4KV, 10times			
Remark : 1. The test samples should be applied to only one test item. 2. Sample size for each test item is 3~5pcs. 3. For High temperature high humidity test, Pure water(Resistance>10MΩ) should be used. 4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part. 5. B/L evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence B/L has. 6. Failure judgment criterion: Basic specification, Electrical characteristic, Mechanical characteristic, Optical characteristic. 7. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.					

11.INSPECTION CRITERION

Refer to 《Inspection Criterion for TFT Products-To customer》 V1.0, DOCUMENT NO.: AVD(WI)-00-QA-048

12. HANDLING PRECAUTIONS

12.1 Mounting method

The LCD module consists of two thin glass plates with polarizers which easily be damaged. And since the module is so constructed as to be fixed by utilizing fitting holes in the printed circuit board. Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent

[recommended below] and wipe lightly :

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent :

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated :

- Soldering flux
- Chlorine (Cl) , Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you :

Connect any unused input terminal to Vdd or Vss, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

12.4 Packing

Module employ LCD elements and must be treated as such.

- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

12.5 Caution for operation

● It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.

● An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.

● Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's have dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.

● If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.

● A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

● Usage under the maximum operating temperature, 50%Rh or less is required.

● When fixed patterns are displayed for a long time, remnant image is likely to occur.

12.6 Storage

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

● Storing in an ambient temperature 10°C to 30°C, and in a relative humidity of 45% to 75%. Don't expose to sunlight or fluorescent light.

● Storing in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with no desiccant.

● Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.

- Storing with no touch on polarizer surface by the anything else.
It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

13. PRECAUTION FOR USE

13.1 A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

13.2 On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification.
- When a new problem is arisen which is not specified in this specifications.
- When an inspection specifications change or operating condition change in customer is reported to AVD, and some problem is arisen in this specification due to the change.
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14. PACKING SPECIFICATION

Please consult our technical department for detail information.

15. INITIALIZATION CODE

TBD

16. HSF COMPLIANCE

- This products complies with ROHS 2011/65/EU and 2015/863/EU、REACH 1907/2006/EC requirements, and the packaging complies with 94-62-EC.



Work Instruction

Inspection Criterion for TFT Products

Doc. No.	AVD (WI) -00-QA-048	Prepared by	chenpeng
Version	V1.1	Checked by	
Pages	10	Customer approval	
Effective date		Released No.	
Controlled Document		Keeping Properly	

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1. Objective

The TFT test criterion are set to formalize TFT quality standards for AVD with reference to those of the customer for inspection, release and acceptance of finished TFT products in order to guarantee the quality of TFT products required by the customer.

2. Scope

The criterion is applicable to all the TFT products manufactured by AVD.

3. Equipment for Inspection

Electrical tester, electrical testing machines, vernier calipers, microscopes, magnifiers, anti-static wrist straps, finger cots/gloves, labels, tri-phase cold and hot shock machine, constant temperature and humidity chamber, backlight table, ovens for high-low temperature experiments, refrigerators, constant voltage power supply (DC) , desk Lamps, etc.

4. Sampling Plan and Reference Standards

4.1 Sampling plan:

Refer to National Standard GB/T 2828.1---2012/ISO2859-1:1999, level II of normal levels:

Product Category	<u>Non-Consumer Electronics</u>	Industrial	Automobile
AQL	<u>MA=0.4 MI=1.5</u>	MA=0.25 MI=0.65	MA=0.15 MI=0.40

4.2 GB/T 2828.1---2012/ISO2859-1:1999 Sampling check procedure in count

4.3GB/T 18910. Standard for LCM parts

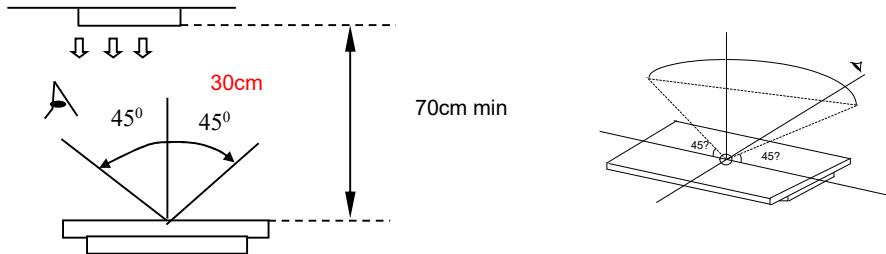
4.4GB/T24213-2008 Basic Environmental Test Procedures for Electrical and Electronic Products

4.5 IPC-A-610E Acceptability of Electronic Assemblies

5. Inspection Conditions and Inspection Reference

5.1Cosmetic inspection: shall be done normally at $23 \pm 5^{\circ}\text{C}$ of the ambient temperature and 45~75%RH of relative humidity, under the ambient luminance between 400lux~600lux and at the distance of 30cm apart between the inspector' s eyes and the LCD panel and normally in reflected light. For backlight LCM, cosmetic inspection shall be done under the ambient luminance between 400lux~600lux with the backlight on.

5.2 The TFT shall be tested at the angle of 45°left and right and 0-45° top and bottom as the following picture showing:



5.3 Definition of viewing area (VA)

A area: Active area (AA area)

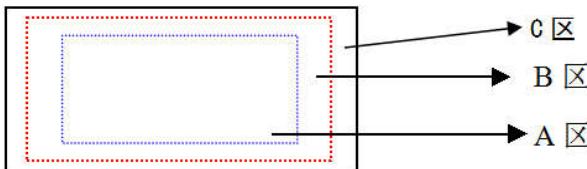
B area: Viewing area (VA area)

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C area: Non-viewing area (not viewing after customer assembly)

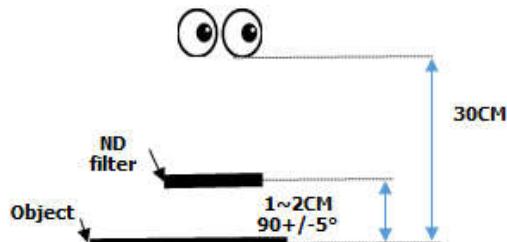
If there is any appearance viewing defect which do not affect product quality and customer assembly in C area, it's accepted in generally.

The criteria apply to A and B area except chipping and crack.



5.4 Inspection with naked eyes(exclusive of the inspection of the physical dimensions of defects carried out with magnifiers)

5.5 ND card use method(refer to below image) and scope: Multi-bright dot; Mura(Black/Gray pattern uneven); dark line and so on.



5.6 Undefined items or other special items, refer to mutual agreement and limited sample. If criterion does not match product specifications/ technical requirement, both should be subject to special inspection criterion agreed by customer.

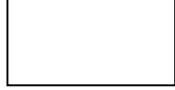
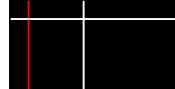
6. Defects and Acceptance Standards

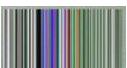
6.1 Electrical properties test

6.1.1 Test voltage(V): Refer to the instruction of testers and the product specification or drawing and the display content and parameters and display effects shall conform to the product specification and drawing.

6.1.2 Current Consumption(I): Refer to approved product specifications or drawings.

6.1.3 Function items(Defect category MA)

No.	Defects	Descriptions	Pictures	Inspection method/tools	Defect category
6.1.3.1	No display /reaction	shows no picture/display in normal connected situation.		Naked eyes/ testers	MA
6.1.3.2	Missing segment	Shows missing lines in normal display		Naked eyes/ testers	MA
6.1.3.3	Dark line	Only visible on gray pattern, 1 or more vertical/horizontal lines: 3%ND, not visible-->OK	/	Naked eyes/ testers	MA

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6.1.3.4	POL angle defect	Not accepted			Naked eyes/ testers	MA
6.1.3.5	Image retention (sticking)	Chess pattern stays for 2mins and change to 50% gray pattern, disappear in 30s, OK; if time>30s, NG			Naked eyes/ testers	MA
6.1.3.6	Display abnormal	Not accepted			Naked eyes/ testers	MA
6.1.3.7	Cross-talk	Refer to AVD specification		/	Naked eyes/ limited sample	MA
6.1.3.8	Display dim/bright	Refer to specification and drawing.		/	Naked eyes/ limited sample	MA
6.1.3.9	Contrast	Refer to specification and drawing.		/	Naked eyes/ limited sample	MA
6.1.3.10	Huge current	Refer to specification and drawing.		/	Ammeter	MA
6.1.3.11	TP function defect	Not accepted		/	Naked eyes/ Touch/ test program	MA

6.2 LCD dot/line defect

6.2.1 LCD pixel dot defect(defect category: MI)

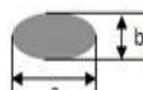
Item	Inspection criterion			
Size	S <5"	5≤S<10"	10≤S<15"	S≥15"
Single bright dot(RGB dot) quantity	1	2	2	3
2 connected bright dot quantity	0	1	1	1
3 connected bright dot or more quantity	0	0	0	0
Bright dot total quantity	1	2	3	4
Single dark dot quantity	2	3	4	5
2 connected dark dot quantity	1	1	2	2
3 connected dark dot or more quantity	0	0	0	0
Dark dot total quantity	3	4	5	6
Multi-bright dot quantity	ND 5 % hidden, OK			

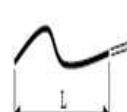
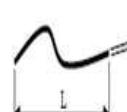
Remark: 2 bright dots distance DS≥15mm 2 dark dots distance DS≥5mm

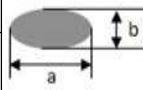
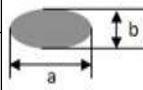
- 1) Bright dot: Power on TFT and RGB dot in black display and size $\geq 1/2$ dot; or bright dot in RGB display
- 2) Dark dot: Power on TFT and gray or black dot in RGB display and size $\geq 1/2$ dot
- 3) Multi-bright dot: Power on TFT and fluorescent tiny dot in black display(only visible in black display) and single dot size $<1/2$ dot

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6.2.2 LCD appearance dot defect (defect category: MI)

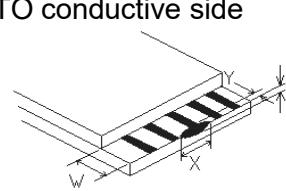
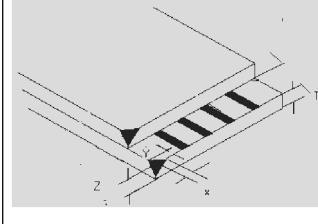
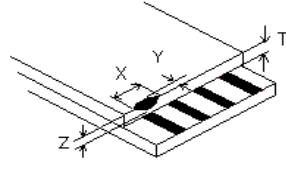
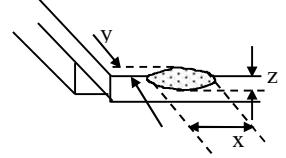
No.	Item	Inspection criterion					Picture	Inspection method/tools			
		Size	S <5"	5≤S<10"	10≤S<15"	S≥15"					
6.2.2.1	Dot defect (black dot, white dot, particle)	D≤0.15	ignore	ignore	D≤0.2; Not count	D≤0.2; ignore		Naked eyes /film card /magnifier			
		0.15< D≤0.25	3	3							
		0.25< D≤0.30	1	2	0.2~0.35 Q'ty ≤4	0.2~0.35 Q'ty ≤ 5					
		0.30< D≤0.35	0	1							
		0.35< D≤0.50	0	0	1	2					
		D>0.5	0	0	0	0					
Remark: D≤0.15mm, not count. Multi-dot as bulk is not accepted.											
Count dot quantity≤ 5; 2 round dots or linear dots in 1 cm is judged as multi-dot.											

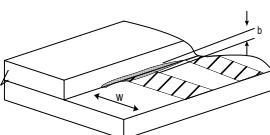
No.	Item	Length (mm)	Width (mm)	S <5"	5≤S<10"	10≤S<15"	S≥15"		Naked eyes /film card /magnifier
		Not count	W≤0.03	Ignored	Ignored	Ignored	Ignored		
6.2.2.2	Line defect (visible when power on)	L≤5	0.03≤W <0.05	3	3	Ignored	Ignored		Naked eyes /film card /magnifier
		L≤5	0.05≤W <0.08	0	1	3	3		
		L≤8	0.05≤W <0.08	0	0	1	2		
		L>8	W> 0.08	0	0	0	0		
Remark: Invisible when power on, only visible in special angle against light, show as watermark/folding/scratch but can not be touched, no control or refer to keeping sample.									

No.	Item	Size(mm)	S <5"	5≤S<10"	10≤S<15"	S≥15"		Naked eyes /film card /magnifier
		D≤0.20	Ignored	Ignored	Ignored	Ignored		
6.2.2.3	Polarizer scratch/ Dent/ bubble defect, particle on polarizer	0.20< D≤0.5	2	2	3	5		Naked eyes /film card /magnifier
		0.50< D≤0.8	0	1	2	3		
		0.8< D≤1.5	0	0	1	2		
		D> 1.5mm	0	0	0	0		

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6.3 Chipping defect

No.	Item	Accepted criterion(mm)				MAJ	MIN
6.3.1	 ITO conductive side	X	/	$\leq 1/8L$	/	√	
		Y	$Y \leq 1/6W$	$1/6W < Y \leq 1/4W$	$1/4W < Y$		
		Accept	2	2	0		
6.3.2	Corner chipping (ITO pins position)	X	/	$\leq 1/6L$	/	√	
		Y	$Y \leq 1/2W$	$1/2W < Y \leq W$	$W < Y$		
	 Corner chipping occurred in sealed edge position as per 6.3.3; at the same time it should not enter into black border of the frame and the corner chipping effect the electric connection position perform as per 6.3.1.	Accept	2	1	0		
6.3.3	Chipping in sealed area (outside chipping)  Chipping in sealed area (inside chipping) 	X	/	$\leq 1/8L$	/	√	
		Y (outside chipping)	Not enter into sealant	Enter $Y \leq H$	$H < Y$		
		Y (inside chipping)		Enter $Y \leq 1/2H$	$1/2H < Y$		
		Z	$\leq T$	$\leq 1/2T$	/		
		Accept	2	1	0		
	The standards of inner and outer chipping on edge sealing area are same. When the chipping occurred in the opposite of stage, Y as per the chipping on the non-conduction side standard in 6.3.1						
6.3.4	conductive side (back side chipping) 	X	/	$\leq 1/6L$	/	√	
		Y	$Y \leq 1/3W$	$1/3W < Y \leq 2/3W$	$2/3W < Y$		
		Accept	2	2	0		
Chipping into ITO side ,refer to 6.3.1							
6.3.5	Protruding LCD	X	/	$\leq 1/8L$	/		√

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	poor cutting and LCD burrs		Y	$\leq 1/6W$	$1/6W < Y \leq 1/5W$	$1/5W < Y$	
			Z	/	/	/	
			Accept	1	1	1	
		the outside protruding control as per the tolerance of drawing.					
6.3.6			Not allow to occur cracks without direction; the crack expand to inside is NG, but to outside is OK (confirmed as per the damaged standard)				✓
<p>Remark: 1) X means the length of chipping; Y means the width; Z means the thickness; W means the step width of the two glasses; H means the distance from the glass edge to the seal inner edge; t means glass thickness.</p>							

6.4 Backlight components

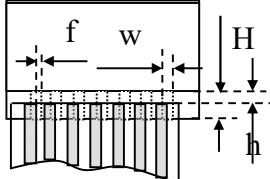
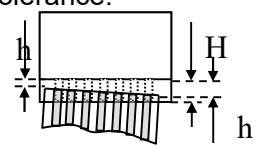
No.	Item	Description	Accepted criterion	MAJ	MIN
6.4.1	No backlight wrong Color	/	Rejected	✓	
6.4.2	Color deviation	When powered on, the LCD color differs from its sample and found that the color not conforming to the drawing after testing.	Refer to specification and drawing.		✓
6.4.3	Brightness deviation	When powered on, the LCD brightness differs from its sample and is found after testing not conforming to the drawing; or if it conforms to the drawing but the brightness over $\pm 40\%$ than its typical value.	Refer to specification and drawing.		✓
6.4.4	Uneven brightness	Uneven on the same LCD and out of the specification of the drawing. The no specification evenness= (the max value-the min value)/ mean value < 70%.	Refer to specification and drawing.		✓
6.4.5	Spot/line /scratch	When power on, it has dirty spot, scratches and so on spot and line defects.	Refer to 6.2.2		✓

6.5 Metal frame (Metal Bezel)

No.	Item	Description	Accepted criterion	MAJ	MIN
6.5.1	Surface color	There were individual and batch differences in surface color.	Accept	✓	
6.5.2	Tab twist Unconformity/ Tab not twisted	Wrong twist method or direction and twist tabs are not twisted as required.	Rejected	✓	
6.5.3	Bezel paint loss	Scratch/paint loss/Bezel surface	It is OK if the		✓

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6.5.4	Bezel scratch		concave-convex dot/dent	customer cannot see it after customer assembly	√
	Painting peel off, discoloration, dent, and scratch				√
6.5.6	Burr		Burr(s) on metal bezel not get into viewing area.	Accept	√

6.6 FPC

No.	Item	Description	Accepted criterion	MAJ	MIN
6.6.1	Model & P/N	Material model & P/N	Keep the same with drawing and technical requirement	√	
6.6.2	Dimension/ position	<p>Dimension in drawing spec</p>  <p>Remark: H=ITO pin length f=FPC width W=ITO pin width</p>	<p>$f \leq 1/3w$, $h \leq 1/3H$, dimension in drawing spec-> OK Conducive material and ITO/PDA connective area must over than 1/2. Entire dimension must be in spec tolerance.</p> 		√
6.6.3	FPC appearance	Hot pressing material get broken, folding line open; FPC golden finger oxidate, broken ,scratch ,foreign material which cause line short	Broken length<2mm; FPC line is OK- > Accepted Crack and line broken-> Rejected		√
6.6.4	FPC burr	Burr near FPC edge area	When cover line and burr length $\leq 1.0\text{mm}$ ->Accepted		√
6.6.5	FPC falling off	FPC bonding area falling off ; silica gel breaking	Rejected		√
6.6.6	Sealant missing ITO line	Sealant is not covered all ITO line	Rejected	√	
6.6.7	Missing sealant	No sealant	Rejected	√	
6.6.8	Sealant	Sealant height > product total height	Rejected	√	
6.6.9	FPC folding	FPC folding as below photo and function is OK->Accept	Accept		√

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6.6.1
0

[FPC connecting fingers](#)
[dent/scratch/ stain](#)

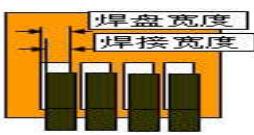
[FPC connecting fingers](#)
[dent/scratch/ stain as below](#)
[photo and function is](#)
[OK->Accept](#)



Accept

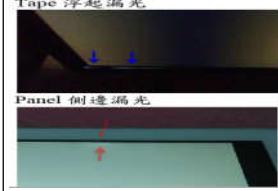
√

6.7 SMT

No.	Item	Description	Accepted criterion	MAJ	MIN
6.7.1	Soldering bridge	Solder between adjacent pads and components 	Rejected		√
6.7.2	Solder ball/splash	Solder ball/tin dross causing short circuit at the solder point. There are active solder ball and splash.	Rejected		√
6.7.3	Soldering excursion	Soldering slant > 1/3 soldering pad 	Rejected		√
6.7.4	Component wrong attaching	Component on PCB differs with drawing: wrong one, extra one, lack one, opposite polarity	Rejected	√	
		JUMP short circuit on PCB: extra soldering ,lack soldering.	Rejected	√	
6.7.5	Component falling off	Soldering but component is missing	Rejected	√	
6.7.6	Wrong component	Component model/spec differs from product specification	Rejected	√	

6.8 General Appearance

No.	Item	Description	Accepted criterion	MAJ	MIN
6.8.1	Protective film scratch/bubble	Protective film scratch/bubble is OK	Accepted	√	

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6.8.2	Surface stain	Defect mark or label are not removed residual glue, and finger print,etc;	Accepted			✓
6.8.3	Product label	Readable even unclear or misplaced part	Accepted			✓
6.8.4	Component mark	Silk screen mark clear, resistance measured value in spec	Accepted			✓
6.8.5	Newton's rings	Area<1/6 screen area&quantity≤1	Accepted			✓
6.8.6	Mura	1.In black/gray display ND 3% invisible ->OK; visible->NG 2.Naked eyes inspection RGB display invisible Black display, area<1/4 screen area	Accepted			✓
6.8.7	Light leak	1.LCD edge(near backlight) shadow by LCD lamps irregular illuminate 2.Judge in black/white/gray display (slight leaky is yellowish, greenish, bluefish ->NG) ;	Refer to limited sample 			✓
6.8.8	Polarizer	1.Polarizer slant.Cover AA and not over LCD edge 2.No unmovable stain or finger print in polarizer AA 3.Bubble/warped but not enter AA	Accepted			✓
6.8.9	TP defect	TP stain(foggy&unremovable)	Accepted			✓
6.8.10	<u>Product side, back</u>	<u>It is defined as a non-inspection area, and can not see the defect from the front side after customer assembly</u>	<u>Accepted</u>			✓

Remark: Anything which is not clearly defined in 6.5~6.8 should refer to IPC-A-610. Non-consumer Electronics refer to class 1 and Industrial, Automobile refer to Class 2.

7. Others

Items not specified in this document or released on compromise should be inspected with reference to mutual agreement and limit samples.