☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: G185BCE
SUFFIX: LE1

Customer:

APPROVED BY **SIGNATURE**

Name / Title ____________________ ____________________

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
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REVISION HISTORY

Version	Date	Page	Description
0.0	July.10, 2023	All	Tentative Specification was first issued.
0.1	Oct.16,2023	33.34	Add MECHANICAL CHARACTERISTICS picture.
1.0	May.10,2024	All	Preliminary Specification was first issued.
2.0	Jun.21,2024	All	Approval Specification was first issued.
2.1	Dec.27,2024	16	Modify converter connector pin assignment description.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

G185BCE-LE1 is a 18.5" IA TFT Liquid Crystal Display module with WLED Backlight unit and 30 pins 1ch-LVDS interface. This module supports 1366 x 768 HD mode and can display up to 16.7M colors. The converter module for Backlight is built in.

1.2 FEATURE

- HD (1366 x 768 pixels) resolution
- LVDS Interface with 1pixel/clock
- PSWG (Panel Standardization Working Group)
- RoHS compliance

1.3 APPLICATION

-TFT LCD Monitor

- Factory Application
- Amusement

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	18.51" real diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1366 x R.G.B. x 768	pixel	-
Pixel Pitch	0.3 (H) x 0.3 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Transmissive Mode	Normally Black	-	-
Surface Treatment	AG type, 3H hard coating, Haze 25	-	-
Luminance, White	400	cd/m2	
Color Gamut	72% of NTSC(Typ.)	-	-
TCO	TCO 5.0 compliance		
Power Consumption	Total 15.5 W @ cell 3.5 W , BL12W		(1)

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	429.87	430.37	430.87	mm	(1)
	Vertical (V)	254.1	254.6	255.1	mm	
	Thickness (T)	-	16.1	16.6	mm	
Bezel Area	Horizontal	413.1	413.4	413.7	mm	
	Vertical	233.7	234	234.3	mm	
Active Area	Horizontal	-	409.8	-	mm	
	Vertical	-	230.4	-	mm	
Weight		-	1315	1370	g	

Note (1)Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	60	ºC	(1)
Operating Ambient Temperature	TOP	0	60	ºC	(1), (2)

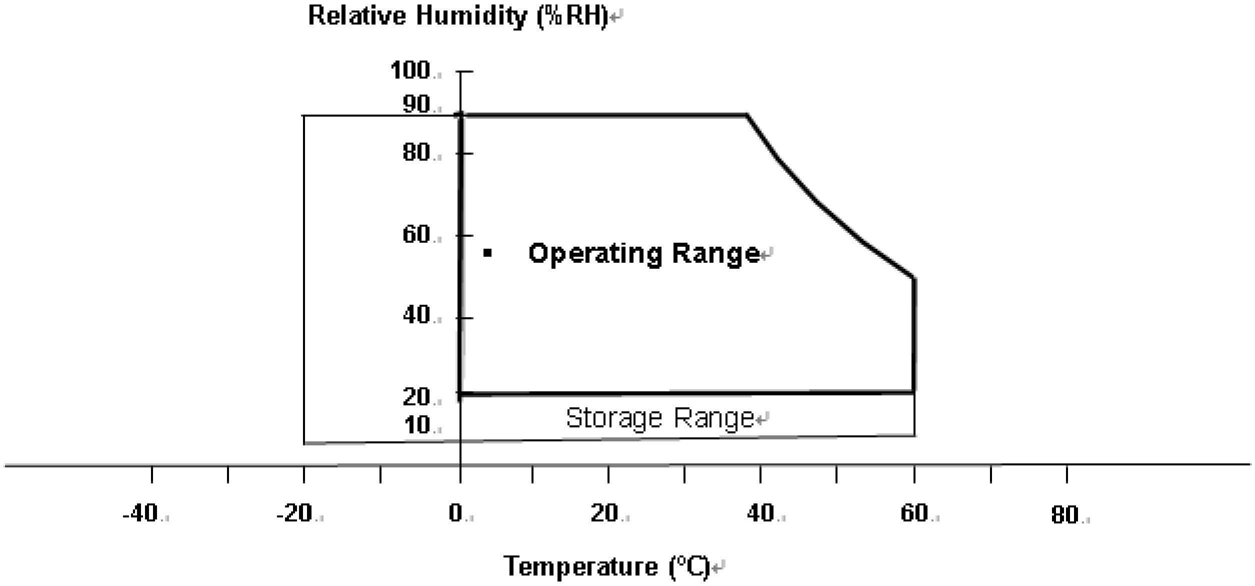
Note (1)

(a) 90 %RH Max.

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) Panel surface temperature should be 60℃ max under Vcc=5.0V, fr =60Hz, typical LED string current, 25℃ ambient temperature, and no humidity control. Any condition of ambient operating temperature ,the surface of active area should be keeping not higher than 60℃.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	6.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Converter Voltage	LED_V_{in}	-0.3	18.0	V	(1), (2) Duty=100%
Enable Voltage	LED_EN	-0.3	5.0	V	
Backlight Adjust	LED_PWM	-0.3	5.0	V	(1), (2) Pulse Width≦10msec. and Duty≦5%

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for LED (Refer to 3.2 for further information).

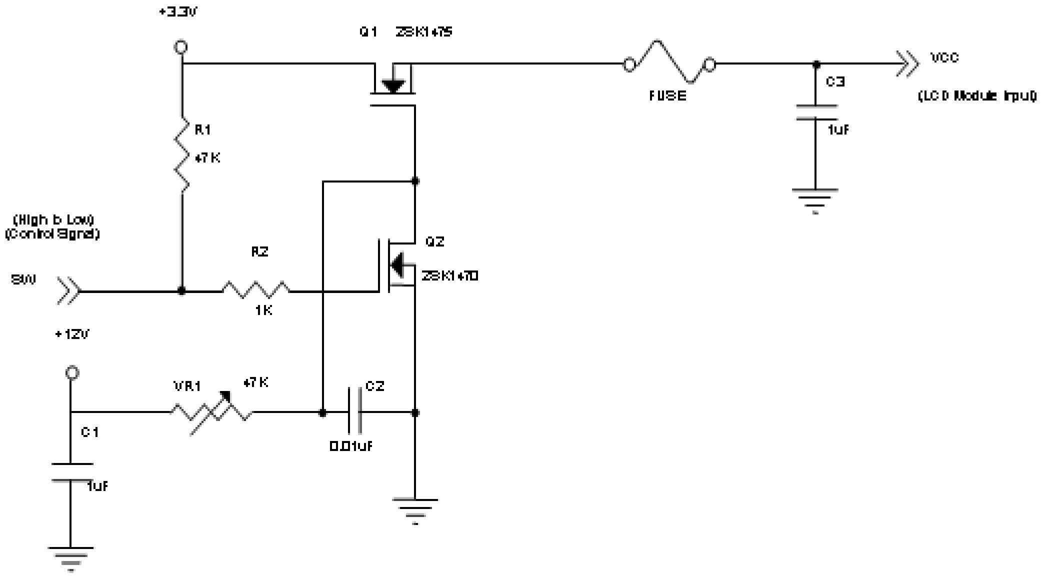
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

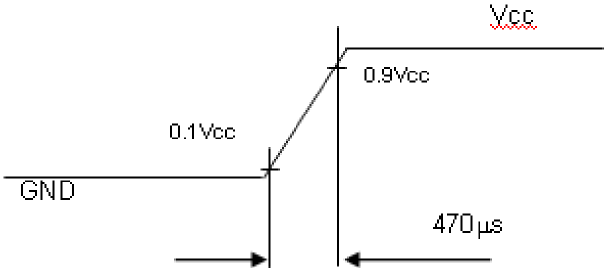
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	4.5	5.0	5.5	V	-
Ripple Voltage		V_{RP}	-	-	300	mVp-p	-
Inrush Current		I_{INRUSH}	-	-	2.0	A	(2)
Power Supply Current	White	Icc	-	0.7	0.84	A	(3)a
	Black		-	0.37	0.45	A	(3)b
	Vertical Stripe		-	0.7	0.84	A	(3)c
Power Consumption		PLCD	-	3.5	4.2	Watt	(4)
LVDS differential input voltage		V_{id}	100	-	600	mV	(5)
LVDS common input voltage		V_{ic}	1.0	1.2	1.4	V	(5)
Differential Input Voltage for LVDS Receiver Threshold	"H" Level	V_{IH}	-	-	100	mV	-
	"L" Level	V_{IL}	-100	-	-	mV	-
Terminating Resistor		R_T	-	100	-	Ohm	-

Note (1)The module should be always operated within above ranges.

Note (2)Measurement Conditions:



Vcc rising time is 470µs



Note (3) The specified power supply current is under the conditions at V_{DD} =5V, Ta = 25 ± 2 ℃, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

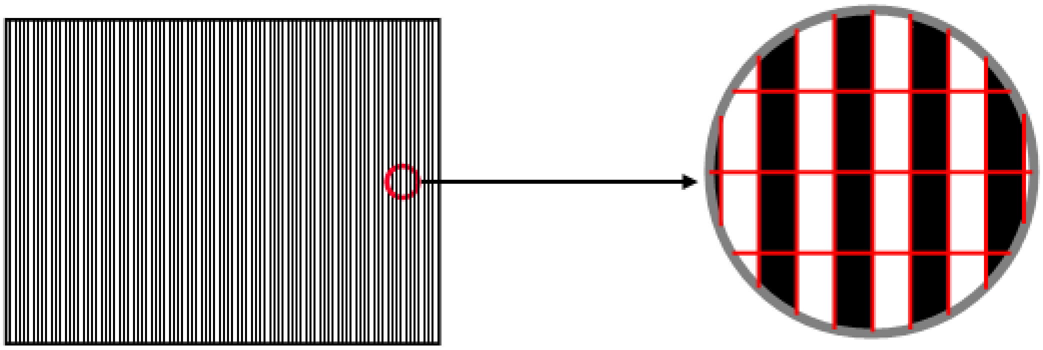
a. White Pattern

Active Area

b. Black Pattern

Active Area

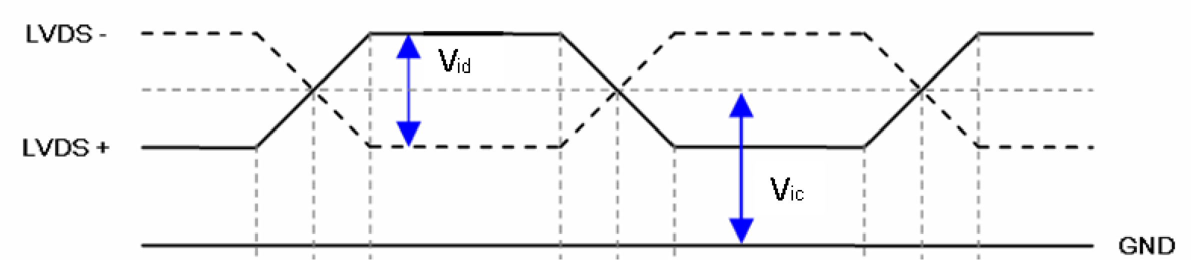
c. Vertical Stripe Pattern



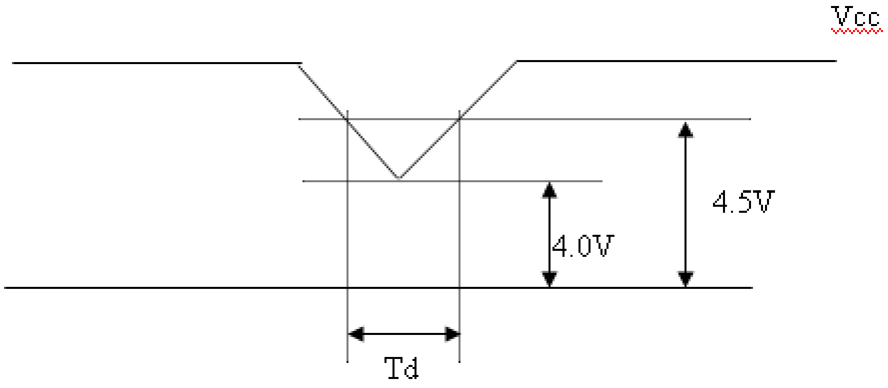
Active Area

Note (4) The power consumption is specified at the pattern with the maximum current.

Note (5) VID waveform condition



3.1.1 Vcc Power Dip Condition

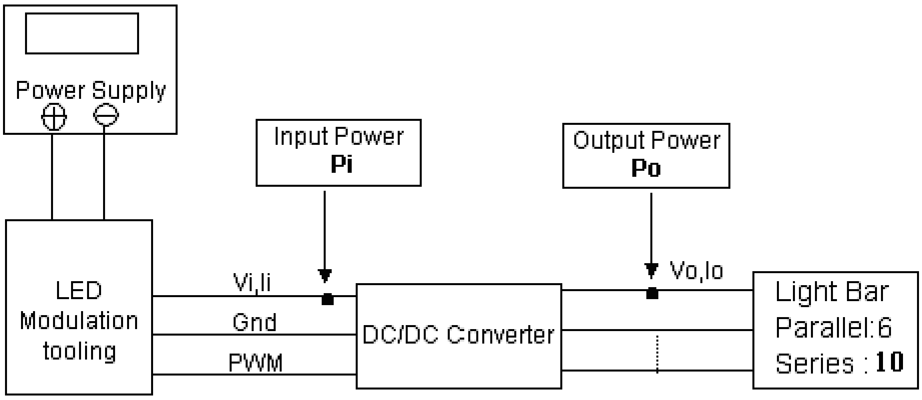


Dip Condition : 4.0V ≦ Vcc ≦ 4.5V, Td ≦ 20mS

3.2 BACKLIGHT UNIT

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Power Supply Voltage		LED_Vin	10.8	12.0	13.2	V	(Duty 100%)
Converter Input Ripple Voltage		V_{iRP}	-	-	500	mV	
Converter Power Supply Current		Ii	0.7	1.0	1.5	A	@LED_Vin= 12V Duty=100%
Converter Input Rush Current		Iirsh			3	A	@LED_Vin rising = 20mS (Vi =12V)
Power Consumption		P_{LED}	8.4	12	18.0	W	(1),@ LED_Vin = 12V Duty=100%
EN Control Level	Backlight on	LED_EN	2.5	3.3	5.0	V	
	Backlight off		0	0	0.3		
PWM Control Level	PWM High Level	LED_PWM	2.5	3.3	5.0	V	
	PWM Low Level		0	0	0.15		
PWN Noise Range		V_{Noise}	-	-	0.1	V	
PWM Control Frequency		f_{PWM}	190	200	20k	Hz	(2)
PWM Control Frequency		-	5		100	%	(3), Suggestion@ 190Hz≦f_{PWM}<1kHz
			20	-	100	%	(3), @ 1kHz≦f_{PWM}≦20kHz
LED Life Time		L_L	50,000			Hrs	(2)

Note (1)LED current is measured by utilizing a high frequency current meter as shown below:

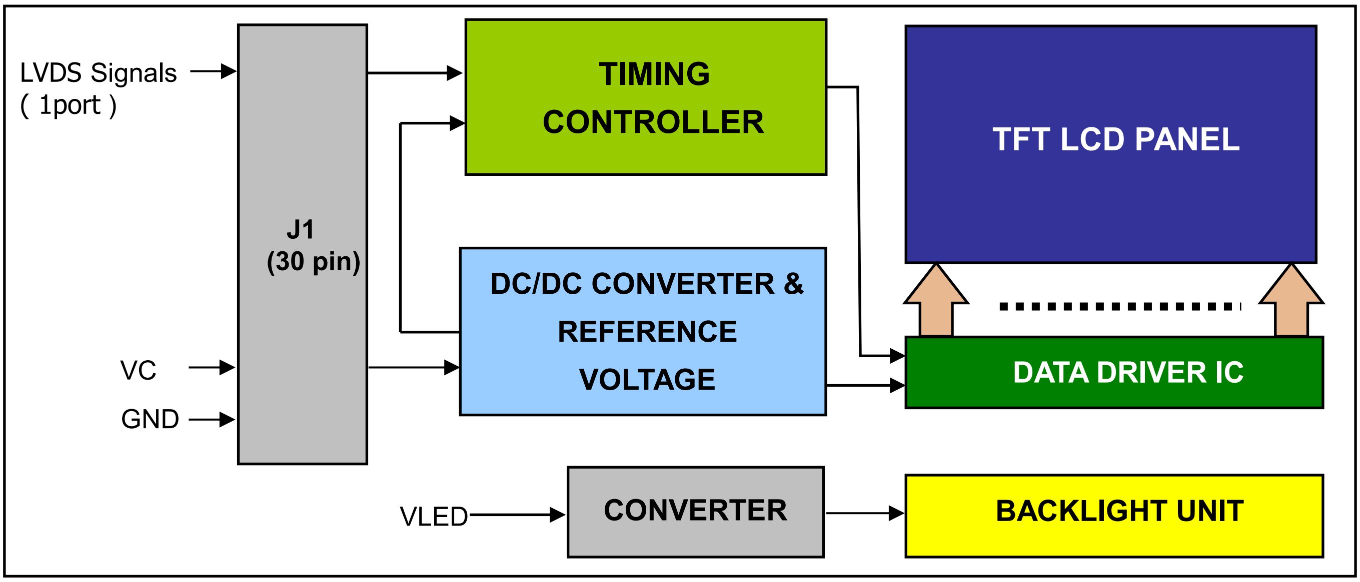


Note (2) The lifetime of LED is estimated data and defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and Duty 100% until the brightness becomes ≦ 50% of its original value.Operating LED at high temperature condition will reduce life time and lead to color shift.

Note (3) At 190 ~1kHz PWM control frequency, duty ratio range is restricted from 5% to 100%.1K ~20kHz PWM control frequency, duty ratio range is restricted from 20% to 100%. If PWM control frequency is applied in the range from 1KHz to 20KHZ, The “non-linear” phenomenon on the Backlight Unit may be found. So It’s a **suggestion** that PWM control frequency should be **less than** 1KHz

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin	Name	Description
1	NC	For LCD internal use only, Do not connect
2	NC	For LCD internal use only, Do not connect
3	NC	For LCD internal use only, Do not connect
4	GND	Ground
5	RX0-	Negative LVDS differential data input. Channel 0
6	RX0+	Positive LVDS differential data input. Channel 0
7	GND	Ground
8	RX1-	Negative LVDS differential data input. Channel 1
9	RX1+	Positive LVDS differential data input. Channel 1
10	GND	Ground
11	RX2-	Negative LVDS differential data input. Channel 2
12	RX2+	Positive LVDS differential data input. Channel 2
13	GND	Ground
14	RXCLK-	Negative LVDS differential clock input.
15	RXCLK+	Positive LVDS differential clock input.
16	GND	Ground
17	RX3-	Negative LVDS differential data input. Channel 3
18	RX3+	Positive LVDS differential data input. Channel 3
19	GND	Ground
20	NC	For LCD internal use only, Do not connect
21	NC	For LCD internal use only, Do not connect
22	NC	For LCD internal use only, Do not connect
23	GND	Ground
24	GND	Ground
25	GND	Ground
26	Vcc	+5.0V power supply
27	Vcc	+5.0V power supply
28	Vcc	+5.0V power supply
29	Vcc	+5.0V power supply
30	Vcc	+5.0V power supply

Note (1) Connector Part No.: STM MSCK2407P30.D or equivalent

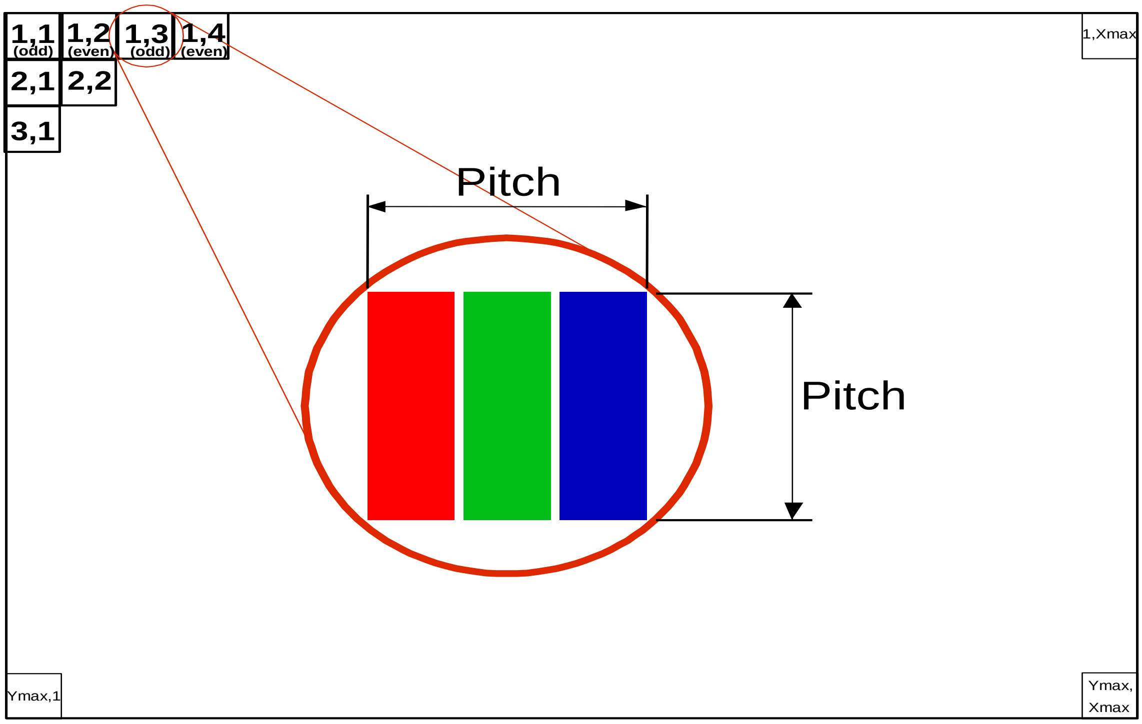
Note (2) User’s connector Part No:

Mating Wire Cable Connector Part No.: FI-X30H(JAE) or FI-X30HL(JAE)

Mating FFC Cable Connector Part No.: 217007-013001 (P-TWO) or JF05X030-1 (JAE).

Note (3) The first pixel is odd.

Note (4) Input signal of even and odd clock should be the same timing.

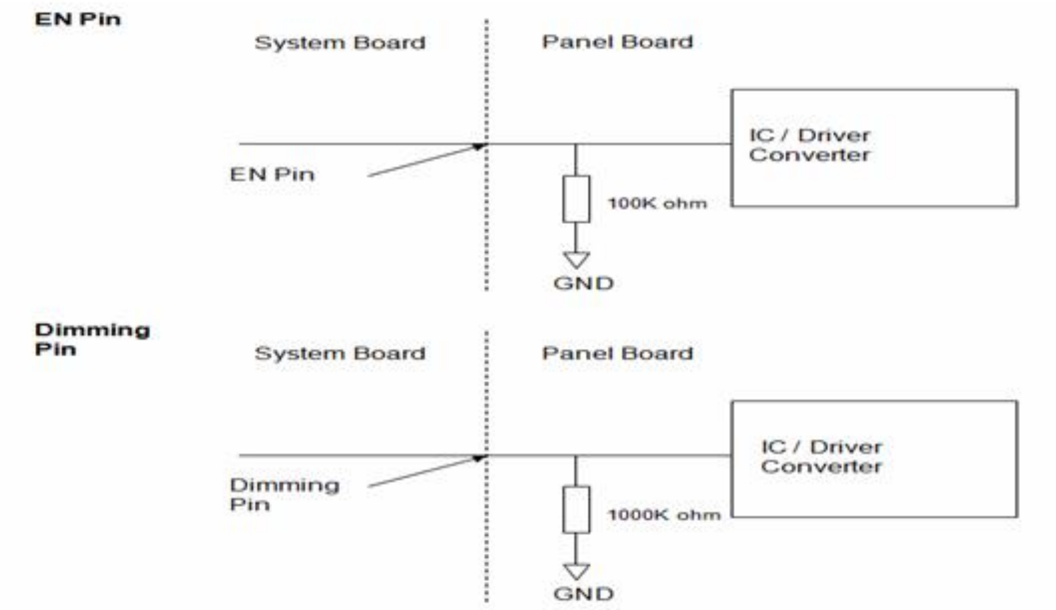

1,1
(odd)
1,2
(even)
1,3
(odd)
1,4
(even)
2,1
2,2
3,1
1,Xmax
Ymax,1
Ymax,
Xmax
Pitch
Pitch

5.2 BACKLIGHT UNIT(Converter connector pin)

Pin	Symbol	Description
1	Vi	Power Supply
2	GND	GND
3	ENABLE	EN_LED
4	Dimming	Dimming
5	NC	NC

Note(1) Connector Part No.: CviLux, CI4205M2HRP-NH or equivalent

Note(2) User's mating connector part No.: CviLux, CI4205SL000 or equivalent



5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1)0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

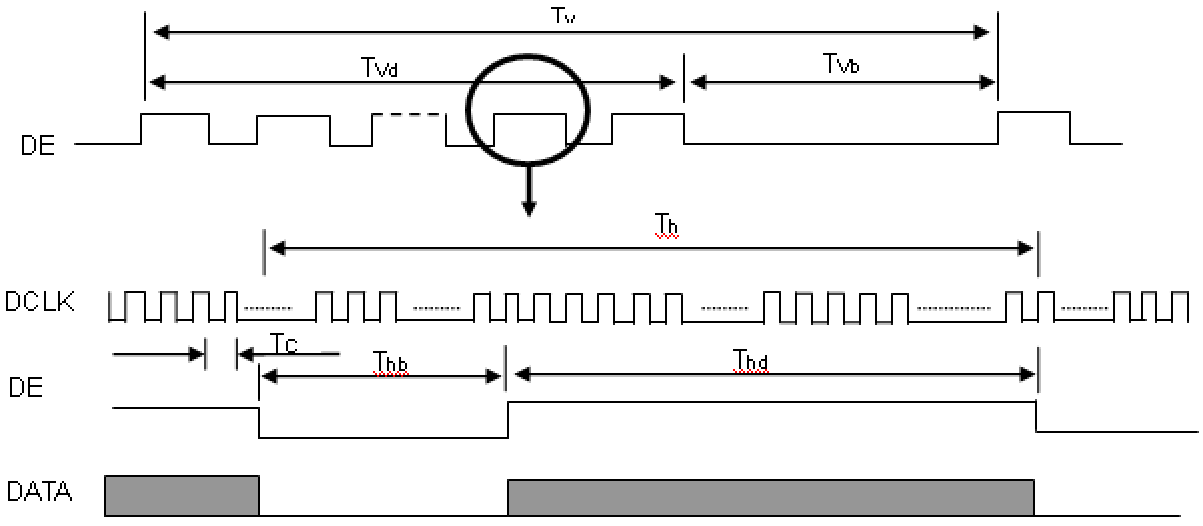
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	Fc	60	76	96	MHz	-
	Period	Tc	10.42	13.16	16.67	ns	
	Input cycle to cycle jitter	T_{rcl}			200	ps	(a)
	Input Clock to data skew	TLVCCS	-400		+400	ps	(b)
	Spread spectrum modulation range	Fclkin_ mod	0.987*Fc		1.013*Fc	MHz	(c)
	Spread spectrum modulation frequency	F_{SSM}			200	KHz	
	High Time	T_{ch}	---	4/7	---	T_{ch}	
	Low Time	T_{cl}	---	3/7	---	T_{ch}	
Vertical Display Term	Frame Rate	Fr	50	60	75	Hz	Tv=Tvd+Tvb
	Total	Tv	800	806	815	Th	-
	Active Display	Tvd	768	768	768	Th	-
	Blank	Tvb	Tv-Tvd	38	Tv-Tvd	Th	-
Horizontal Display Term	Total	Th	1500	1560	1570	Tc	Th=Thd+Thb
	Active Display	Thd	1366	1366	1366	Tc	-
	Blank	Thb	Th-Thd	194	Th-Thd	Tc	-

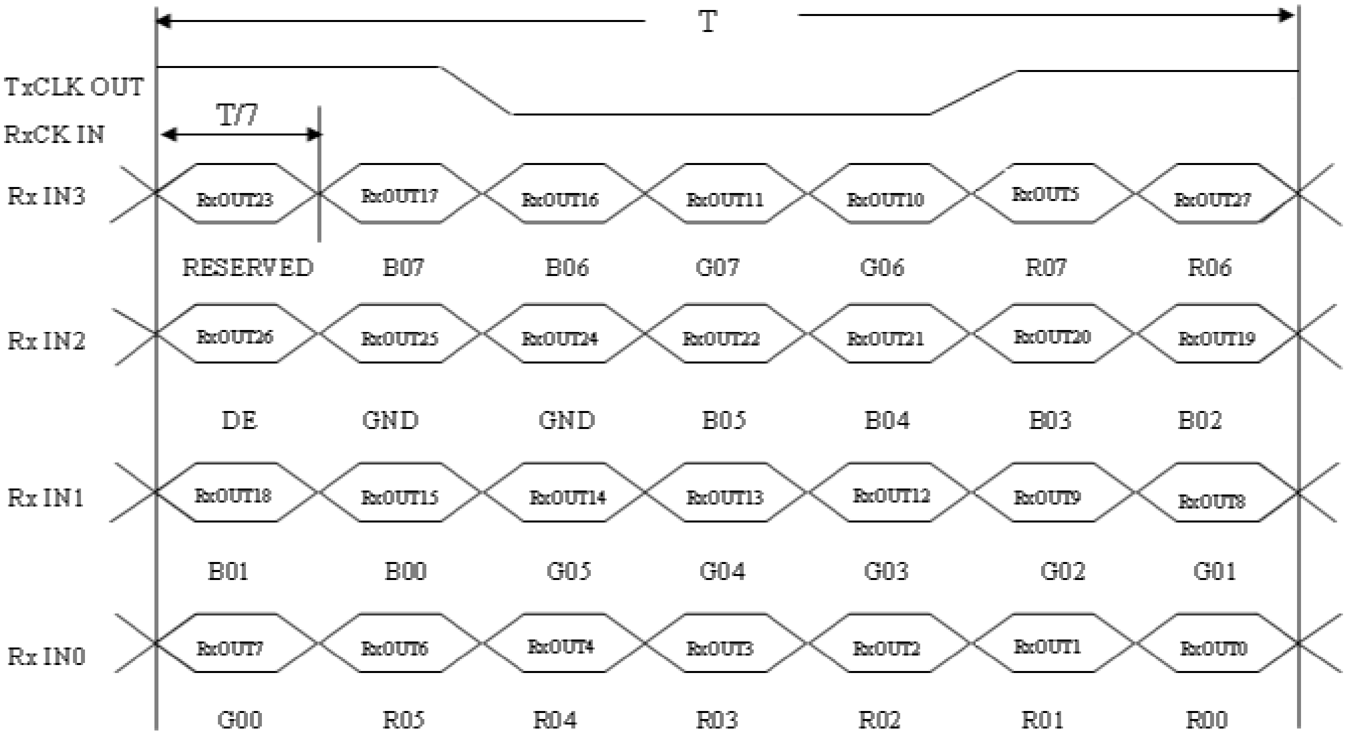
Note (1) Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

Note (2) The Tv(Tvd+Tvb) must be integer, otherwise, the module would operate abnormally.

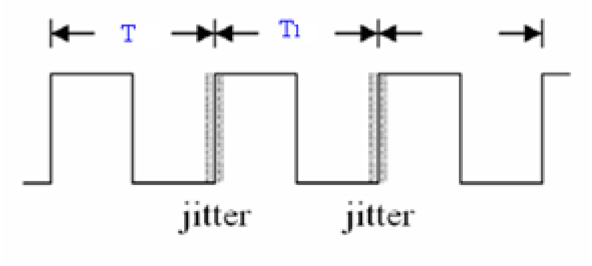
INPUT SIGNAL TIMING DIAGRAM



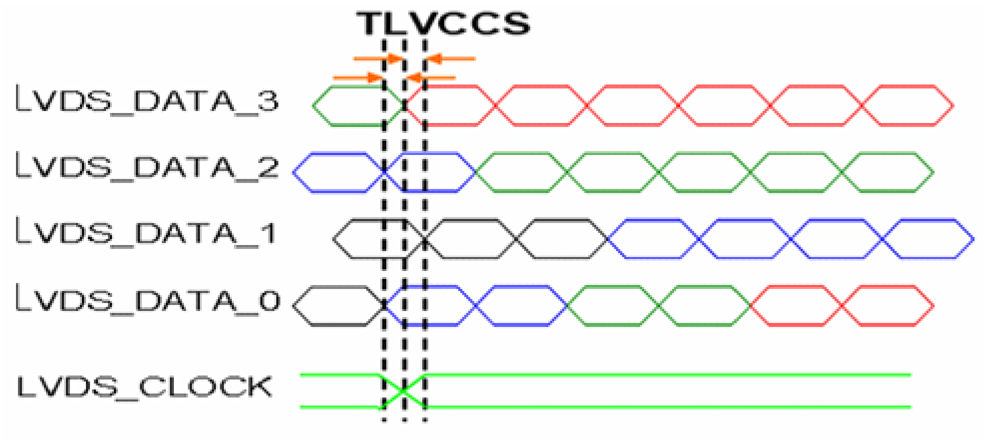
TIMING DIAGRAM of LVDS



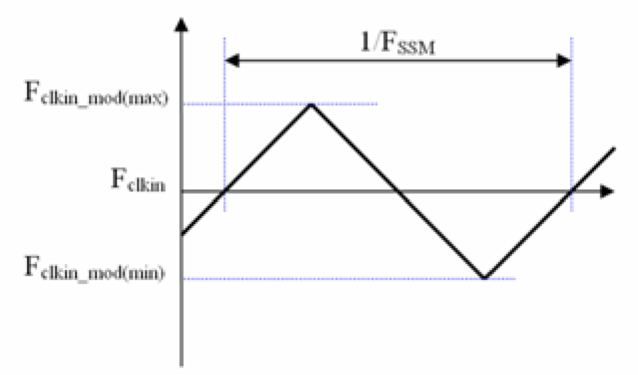
Note (a) The input clock cycle-to-cycle jitter is defined as below figures. $T_{rcl} = | T1 - T|$



Note (b) Input Clock to data skew is defined as below figures.

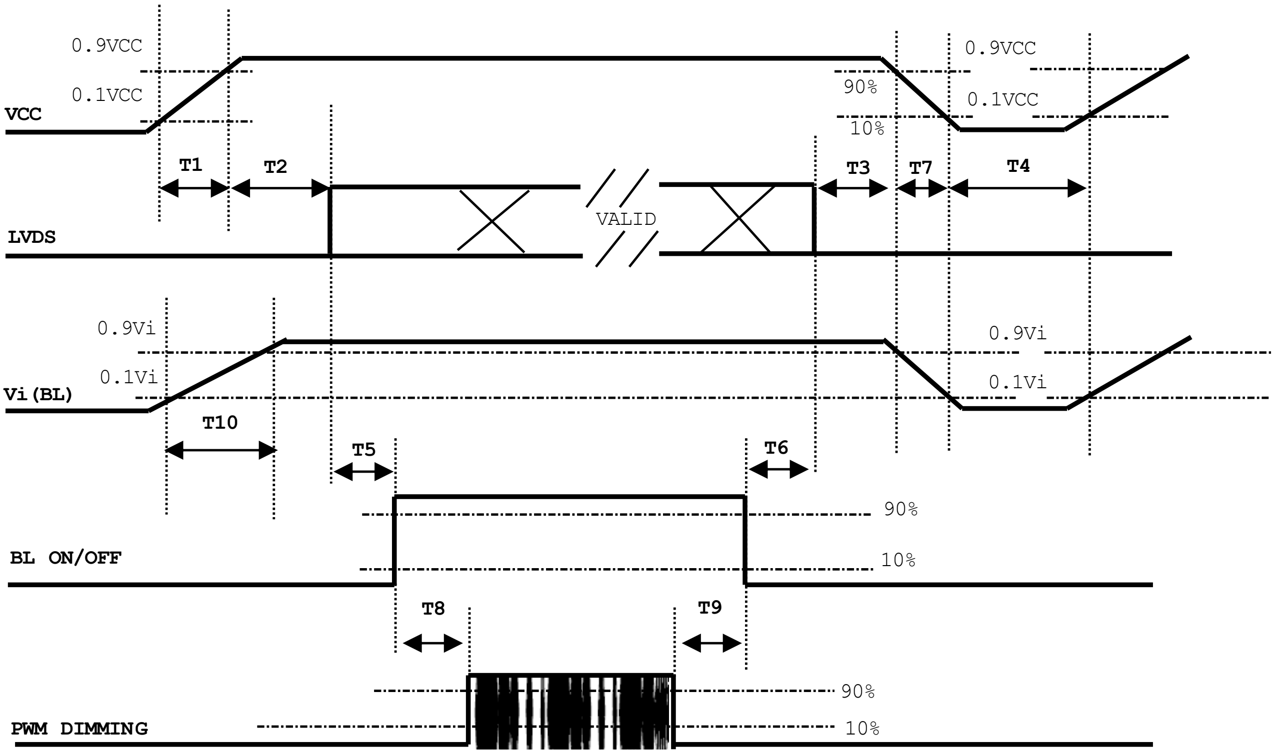


Note (c) The SSCG (Spread spectrum clock generator) is defined as below figures.



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD assembly, the power on/off sequence should be as the diagram below.



Parameter	Value			Units
	Min	Typ	Max	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	0	-	50	ms
T4	500	-	-	ms
T5	450	-	-	ms
T6	200	-	-	ms
T7	10	-	100	ms
T8	10	-	-	ms
T9	10	-	-	ms
T10	20	-	50	ms

Note:

(1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.

(2) When the backlight turns on before the LCD operation of the LCD turns off, the display may momentarily become abnormal screen.

(3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

(6) INX won't take any responsibility for the products which are damaged by the customers not following the Power Sequence.

(7) There might be slight electronic noise when LCD is turned off (even backlight unit is also off). To avoid this symptom, we suggest "Vcc falling timing" to follow "T7 spec".

6.3 SCANNING DIRECTION

The following figures show the image see from the front view. The arrow indicates the direction of scan.

PCBA on the top side

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	According to typical value and tolerance in "ELECTRICAL CHARACTERISTICS"		
Input Signal			
PWM Duty Ratio	D	100	%

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown here and all items are measured at the center point of screen unless otherwise noted. The following items should be measured under the test conditions described above and stable conditions shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rx	θX=0°, θY =0° Grayscale Maximum	0.600	0.650	0.700	-	(1), (5)
		Ry		0.289	0.339	0.389		
	Green	Gx		0.270	0.320	0.370		
		Gy		0.560	0.610	0.660		
	Blue	Bx		0.100	0.150	0.200		
		By		0.000	0.050	0.100		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
Center Luminance of White		LC		320	400		nits	(4), (5)
Contrast Ratio		CR		700	1000		-	(2), (5)
Response Time		TR	θX=0°, θY =0°	-	13	18	-	(3)
		TF		-	12	17	-	
White Variation		δW	θX=0°, θY =0°	75	-	-	%	(5), (6)
Viewing Angle	Horizontal	θX+	CR≧10	80	89	-	Deg.	(1), (5)
		θX-		80	89	-		
	Vertical	θY+		80	89	-		
		θY-		80	89	-		

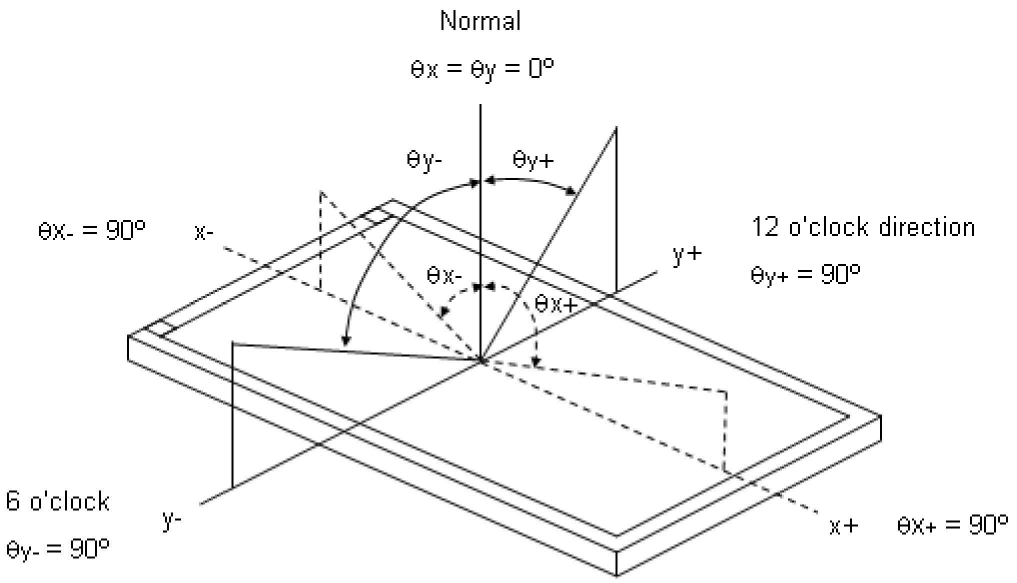
Definition：

Grayscale Maximum : Grayscale 255 (10 bits: grayscale 1023 ; 8 bits : grayscale 255 ; 6 bits: grayscale 63)

White : Luminance of Grayscale Maximum (All R,G,B)

Black : Luminance of grayscale 0 (All R,G,B)

Note (1)Definition of Viewing Angle (θx, θy):

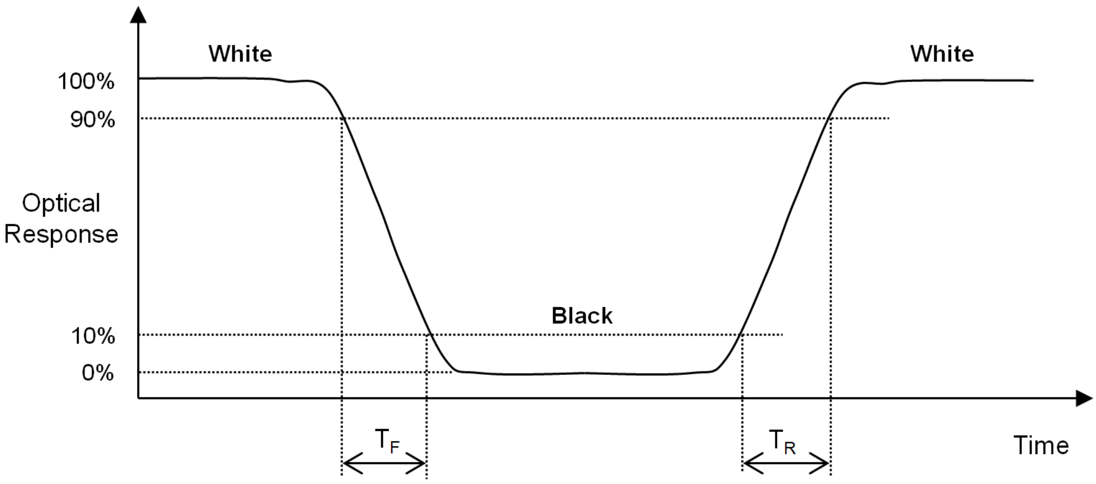


Note (2)Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression at center point.

Contrast Ratio (CR) = White / Black

Note (3) Definition of Response Time (T_R, T_F):

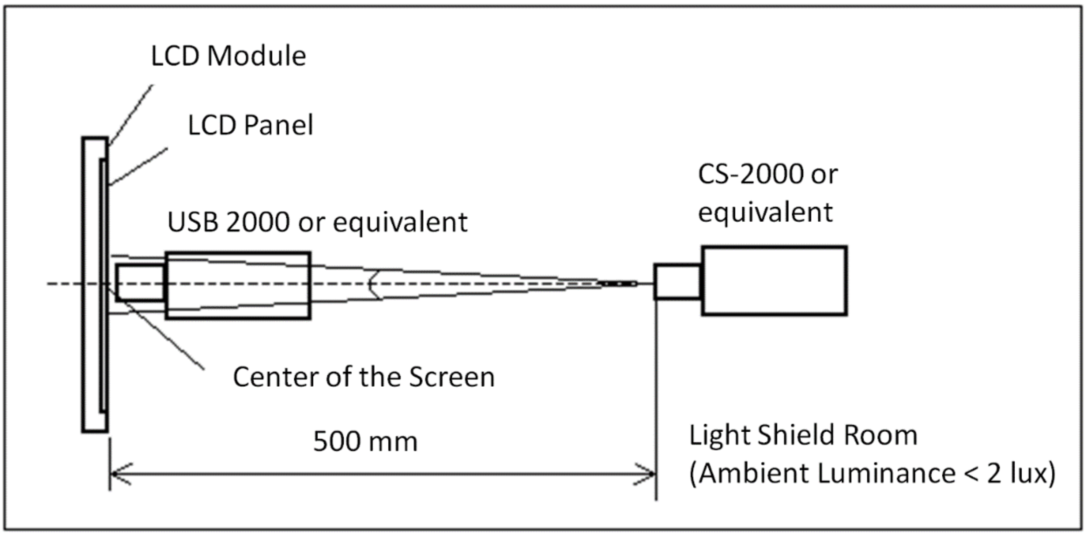


Note (4) Definition of Luminance of White (L_C):

Measure the luminance of White at center point.

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 40 minutes in a windless room. The measurement placement of module should be in accordance with module drawing.

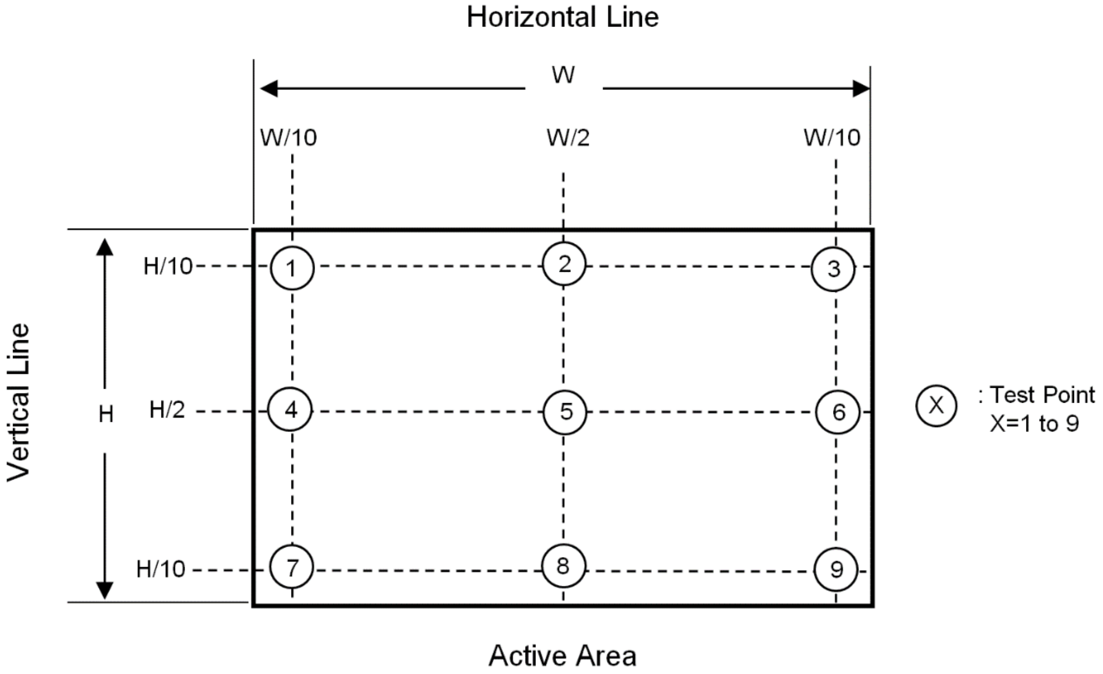


Note (6) Definition of White Variation (δW):

Measure the luminance of White at 9 points.

Luminance of White : L(X) , where X is from 1 to 9.

$$\delta W = \frac{\text{Minimum } [\,L(1) \text{ to } L(9)\,]}{\text{Maximum } [\,L(1) \text{ to } L(9)\,]} \times 100\%$$



8. RELIABILITY TEST CRITERIA

Test Item	Test Condition	Note
High Temperature Storage Test	60℃, 240 hours	(1),(2) (4),(5)
Low Temperature Storage Test	-20℃, 240 hours	
Thermal Shock Storage Test	-20℃, 0.5 hour⟷60℃, 0.5 hour; 100cycles, 1 hour/cycle)	
High Temperature Operation Test	60℃, 240 hours	
Low Temperature Operation Test	0℃, 240 hours	
High Temperature & High Humidity Operation Test	50℃, RH 80%, 240 hours	
ESD Test (Operation)	150pF, 330Ω, 1 sec/cycle Condition 1 : panel contact, ±8 KV Condition 2 : panel non-contact ±15 KV	(1), (4)
Shock (Non-Operating)	50G, 11ms, half sine wave, 1 time for ± X, ± Y, ± Z direction	(2), (3)
Vibration (Non-Operating)	1.5G, 10 ~ 300 Hz sine wave, 30 min/cycle, 1 cycles each X, Y, Z direction	

Note (1)There should be no condensation on the surface of panel during test ,

Note (2) Temperature of panel display surface area should be 60ºC Max.

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Note (4) In the standard conditions, there is no function failure issue occurred. All the cosmetic specification is judged before reliability test.

Note (5) Before cosmetic and function test, the product must have enough recovery time, at least 24 hours at room temperature.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 10pcs LCD modules / 1 Box

(2) Box dimensions: 525 (L) X 284 (W) X 360 (H) mm

(3) Weight: approximately 16.3Kg (10 modules per box)

9.2 PACKING METHOD

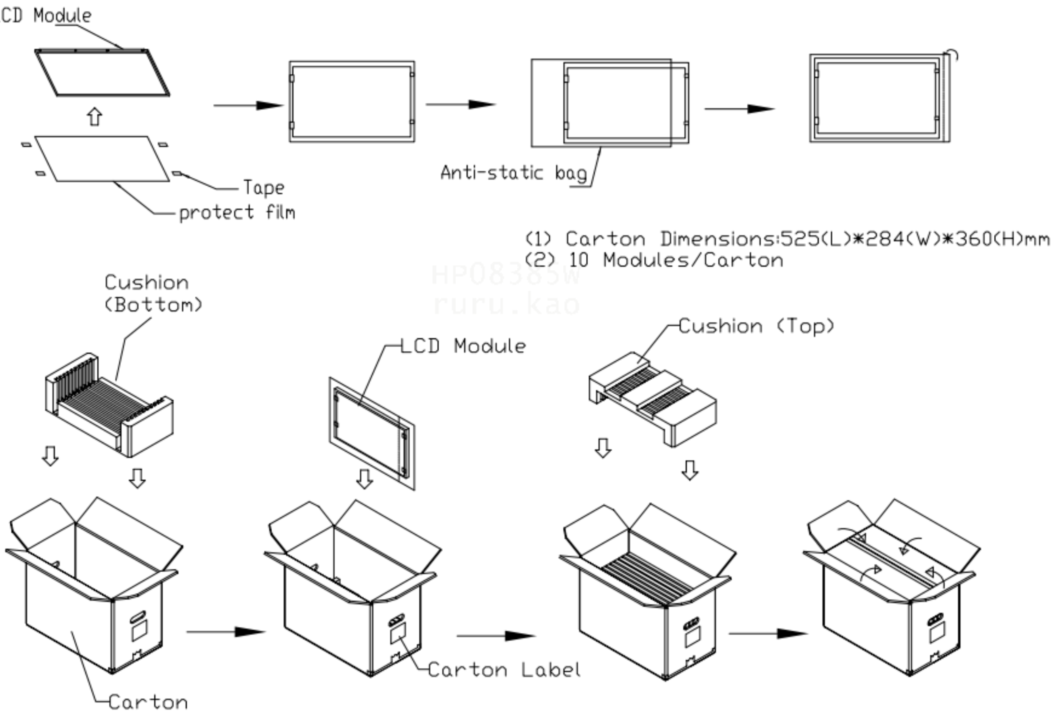


Figure. 9-1 Packing method

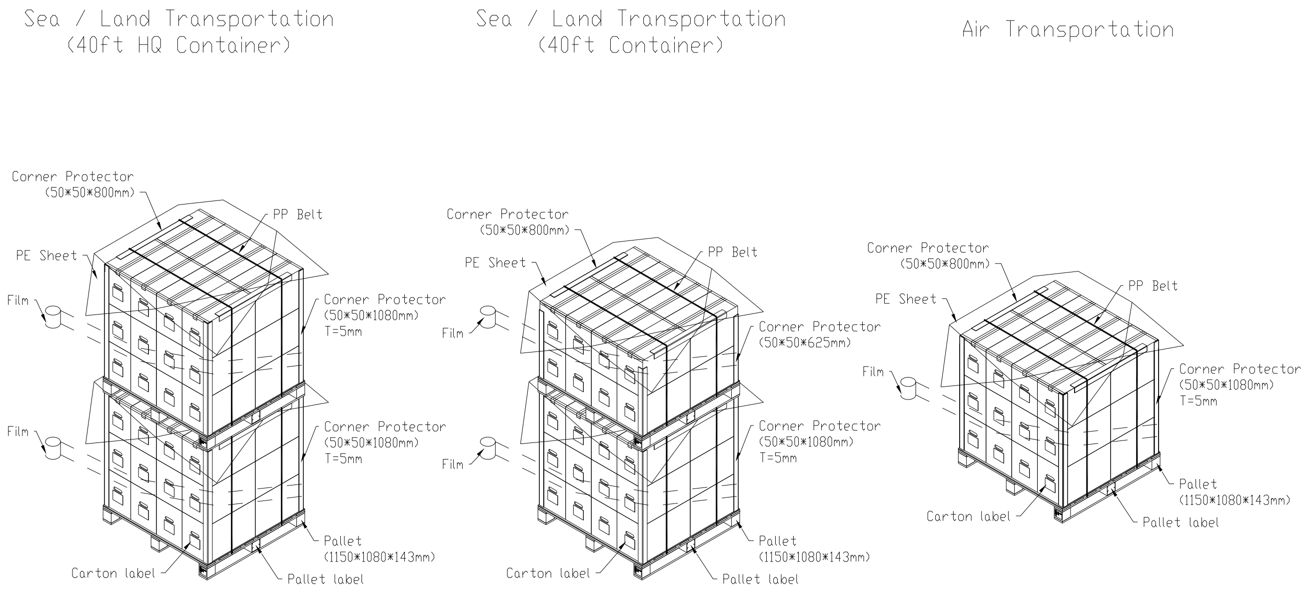


Figure. 9-2 Packing method

9.3 UN-PACKING METHOD

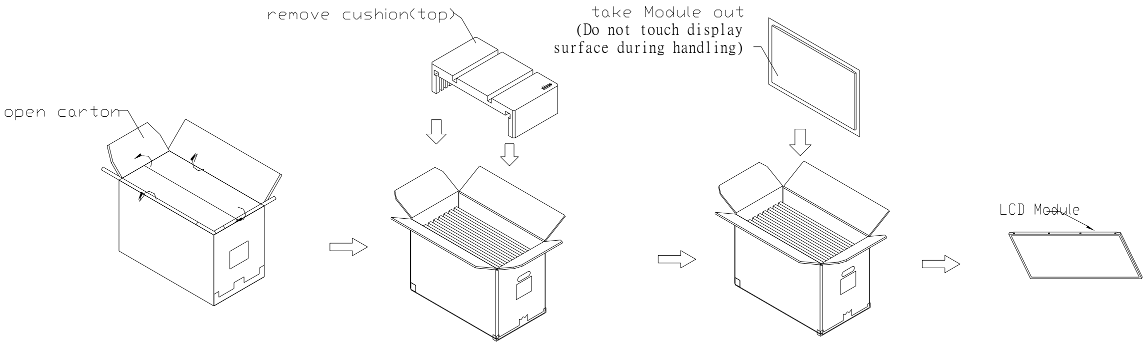
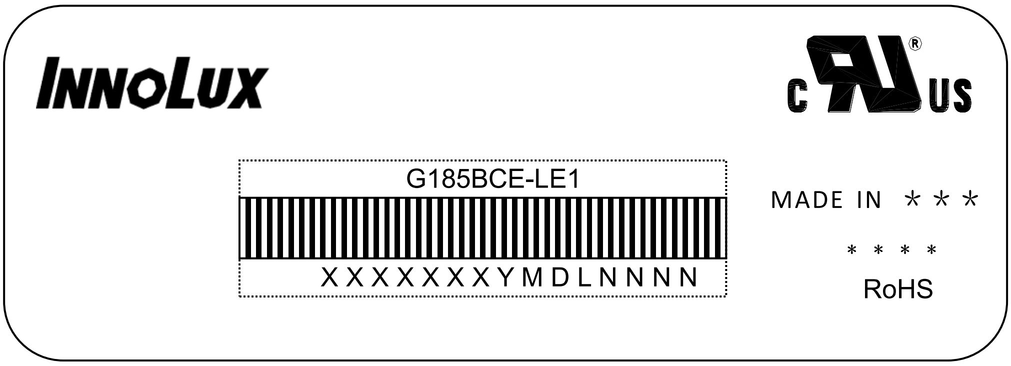


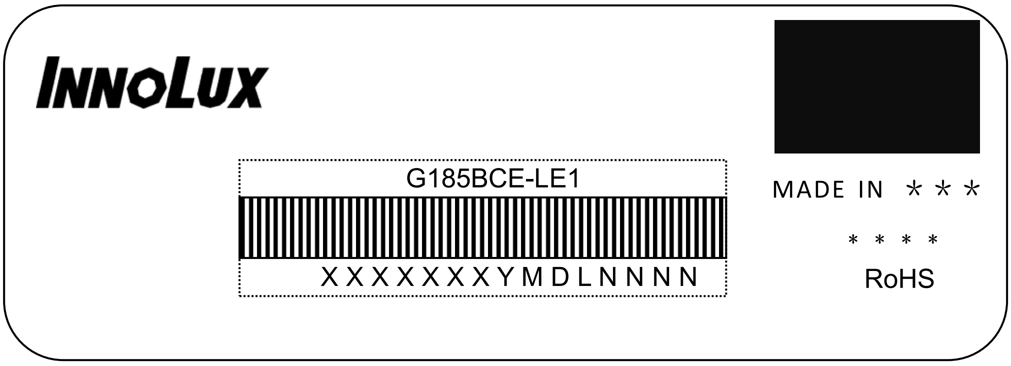
Figure. 9-3 UN-Packing method

10. DEFINITION OF LABELS

10.1 INX MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



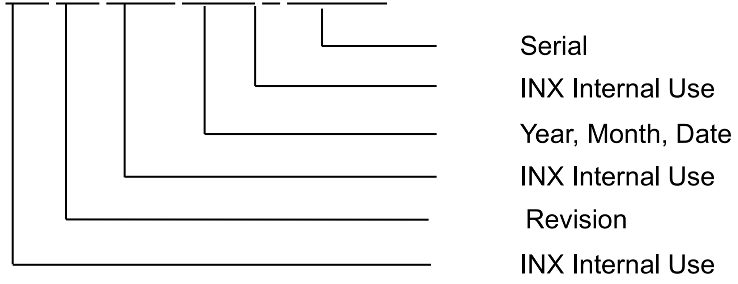


Note (1) Safety Compliance(UL logo) will open after C1 version.

(a) Model Name: G185BCE-LE1

(b) ＊＊＊＊ : Factory ID

(c) Serial ID: X X X X X X X Y M D X N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2021~2029

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

11. PRECAUTIONS

11.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the lamp wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

11.2 STORAGE PRECAUTIONS

(1)When storing for a long time, the following precautions are necessary.

(a) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 30°C at humidity 50+-10%RH.

(b) The polarizer surface should not come in contact with any other object.

(c) It is recommended that they be stored in the container in which they were shipped.

(d) Storage condition is guaranteed under packing conditions.

(e) The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition

(2) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(3) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(4) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

(5) Storage must be in a fully packaged state (PET bag) and do not expose the sample (module)

11.3 OTHER PRECAUTIONS

(1) Normal operating condition

(a) Display pattern: dynamic pattern (Real display)

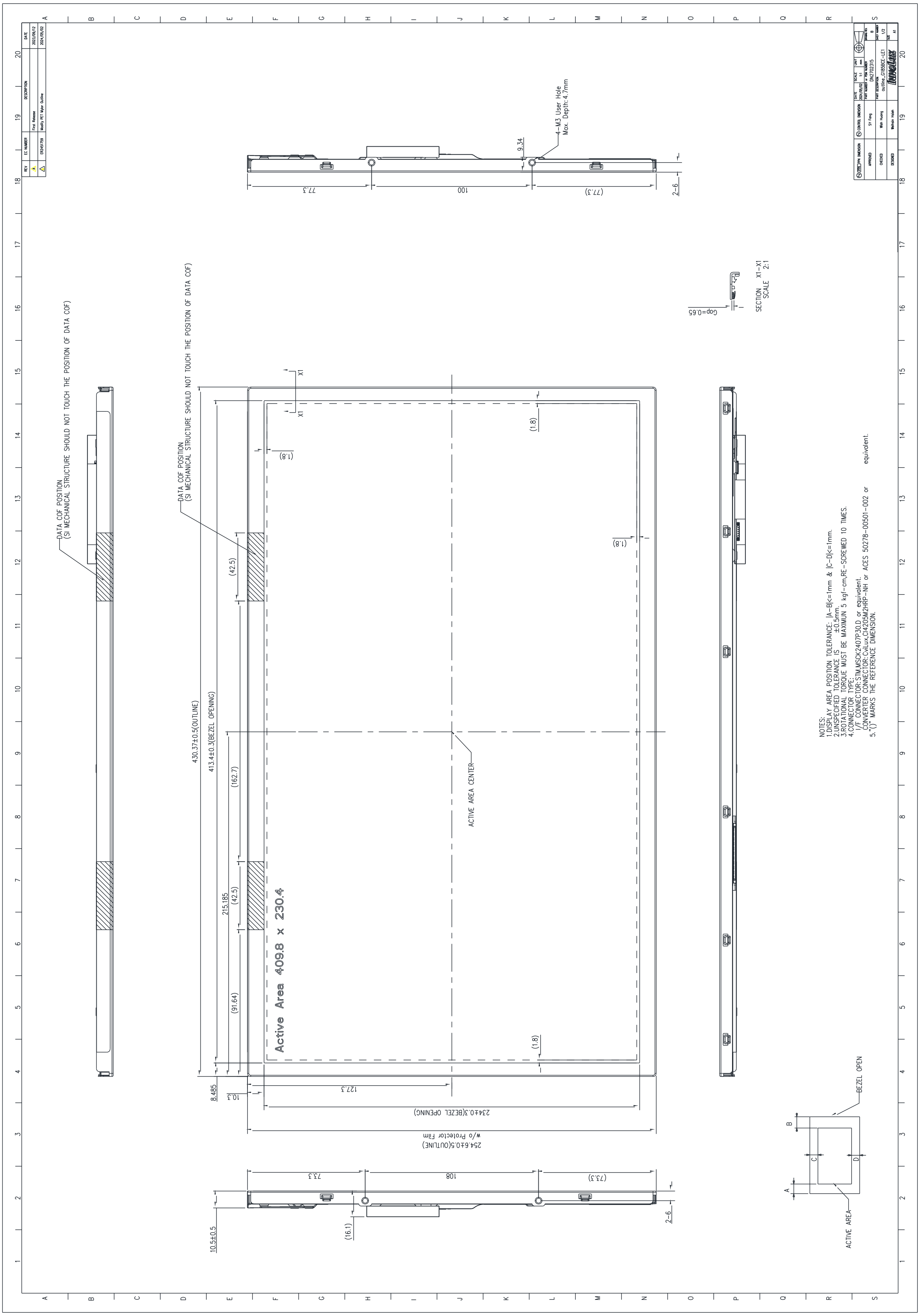
(Note) Long-term static display can cause image sticking.

(2) Operating usages to protect against image sticking due to long-term static display

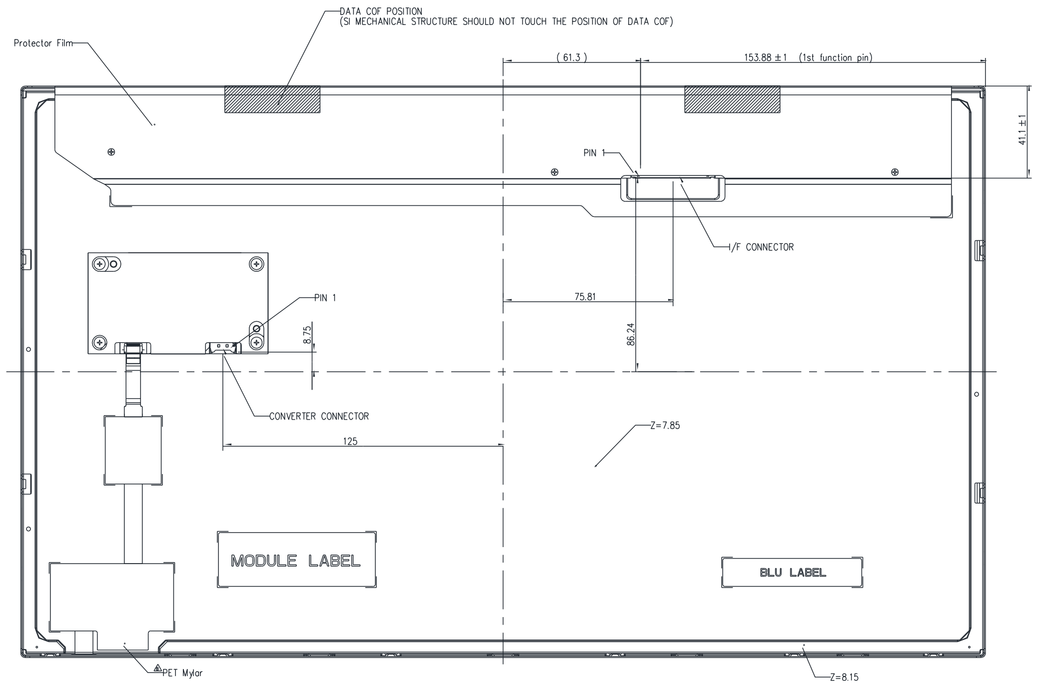
(a) Static information display recommended to use with moving image.

(3) Abnormal condition just means conditions except normal condition.

12. MECHANICAL CHARACTERISTICS



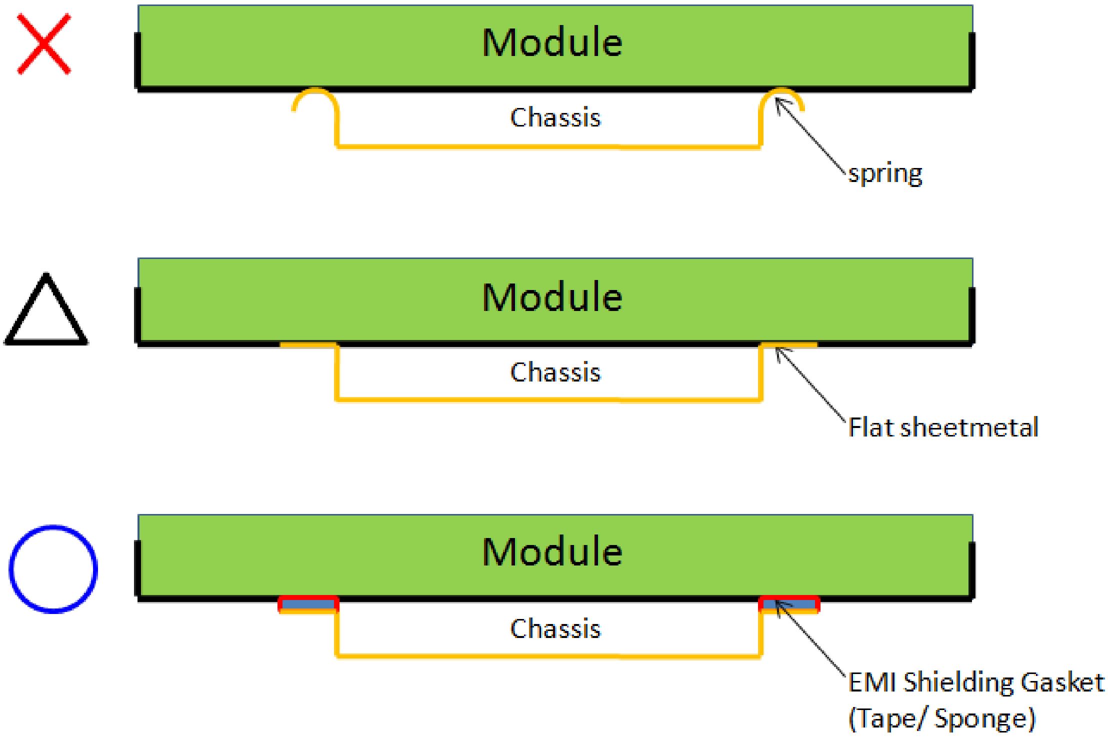
REV	EC NUMBER	DESCRIPTION	DATE
A		First Release	2023/09/12
B	ER2451759	Modify PET Mylar Outline	2024/05/02



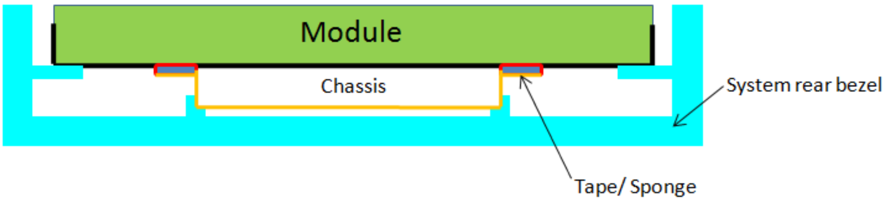
NOTES:
1.DISPLAY AREA POSITION TOLERANCE: |A−B|<=1mm & |C−D|<=1mm.
2.UNSPECIFIED TOLERANCE IS ±0.5mm.
3.ROTATIONAL TORQUE MUST BE MAXIMUN 5 kgf−cm,RE−SCREWED 10 TIMES.
4.CONNECTOR TYPE:
  I/F CONNECTOR:STM,MSCK2407P30.D or equivalent.
  CONVERTER CONNECTOR:CviLux,CI4205M2HRP−NH or ACES 50278−00501−002 or equivalent.
5."()" MARKS THE REFERENCE DIMENSION.

Ⓝ PPK PPK DIMENSION	Ⓝ CONTROL DIMENSION	DATE 2024/05/02	SCALE 1:1	UNIT mm	
APPROVED	SY Feng	PART NUMBER or PDM NUMBER DN2702315			DRAWING REV. B
CHECKED	Wish Huang	PART DESCRIPTION outline_G185BCE-LE1			SHEET NUMBER 2/2
DESIGNED	Weihsin Hsieh	InnoLux			SIZE A1

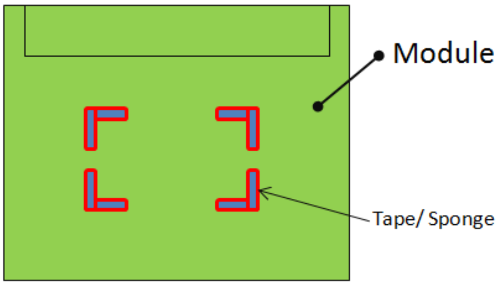
Appendix. SYSTEM COVER DESIGN NOTICE

<table>
<tr><th>1</th><th>Set Chassis and IA Module touching Mode</th></tr>
<tr><td colspan="2">
</td></tr>
<tr><td>Definition</td><td>a. To prevent from abnormal display & white spot after mechanical test, it is not recommended to use spring type chassis.
b. We suggest the contact mode between Chassis and Module rear cover is Tape/Sponge, second is Flat sheet metal type chassis.</td></tr>
</table>

2	**Tape/Sponge design on system inner surface**



✕



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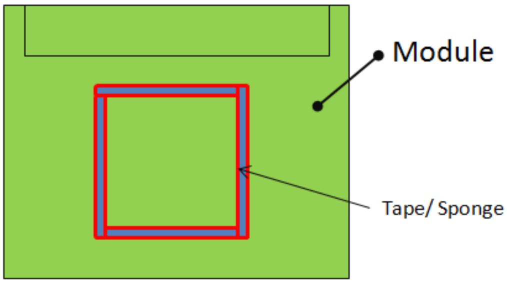
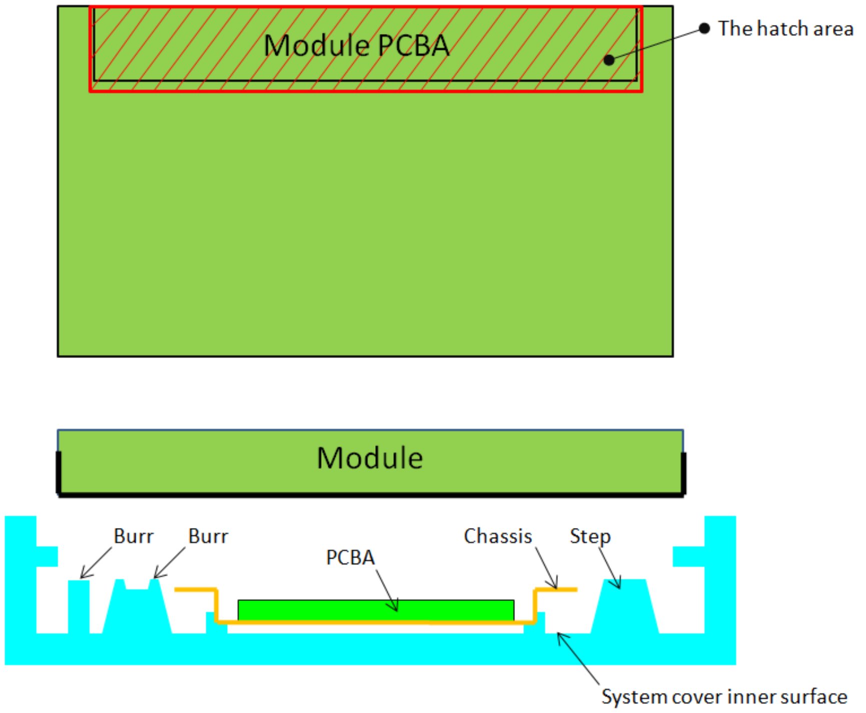
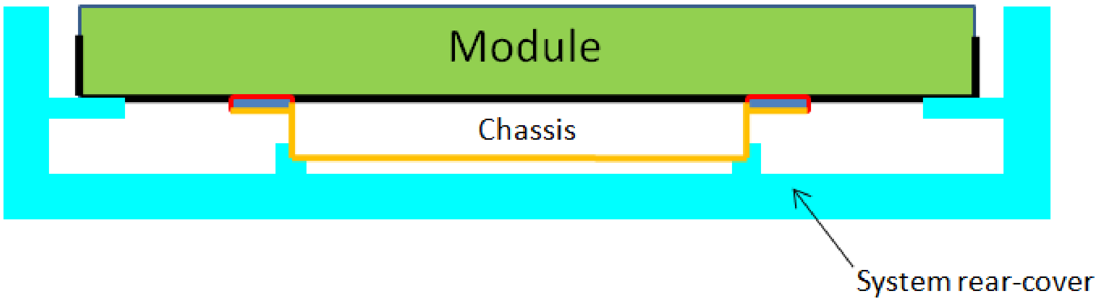
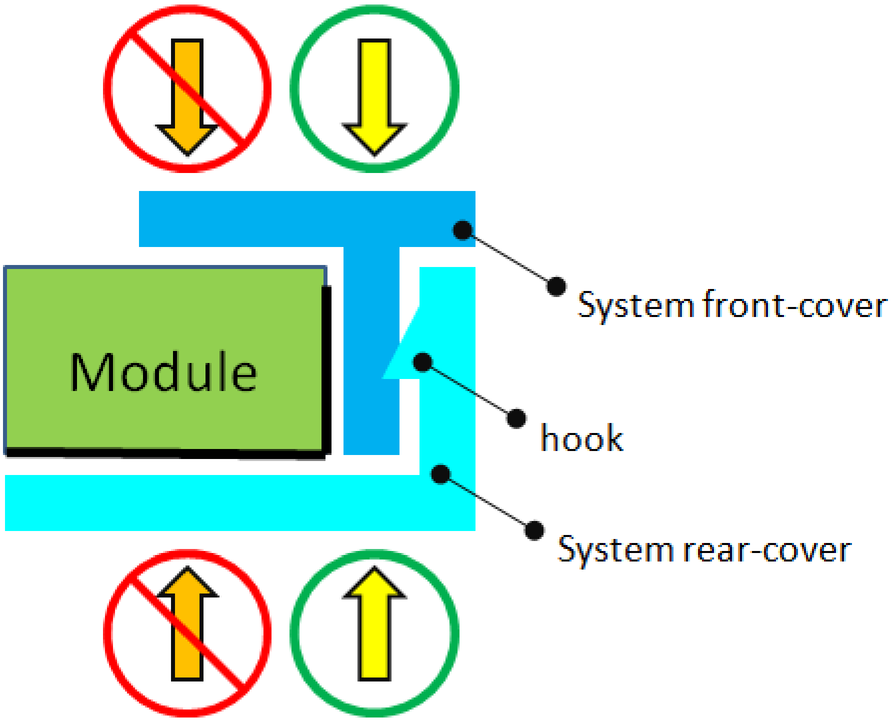
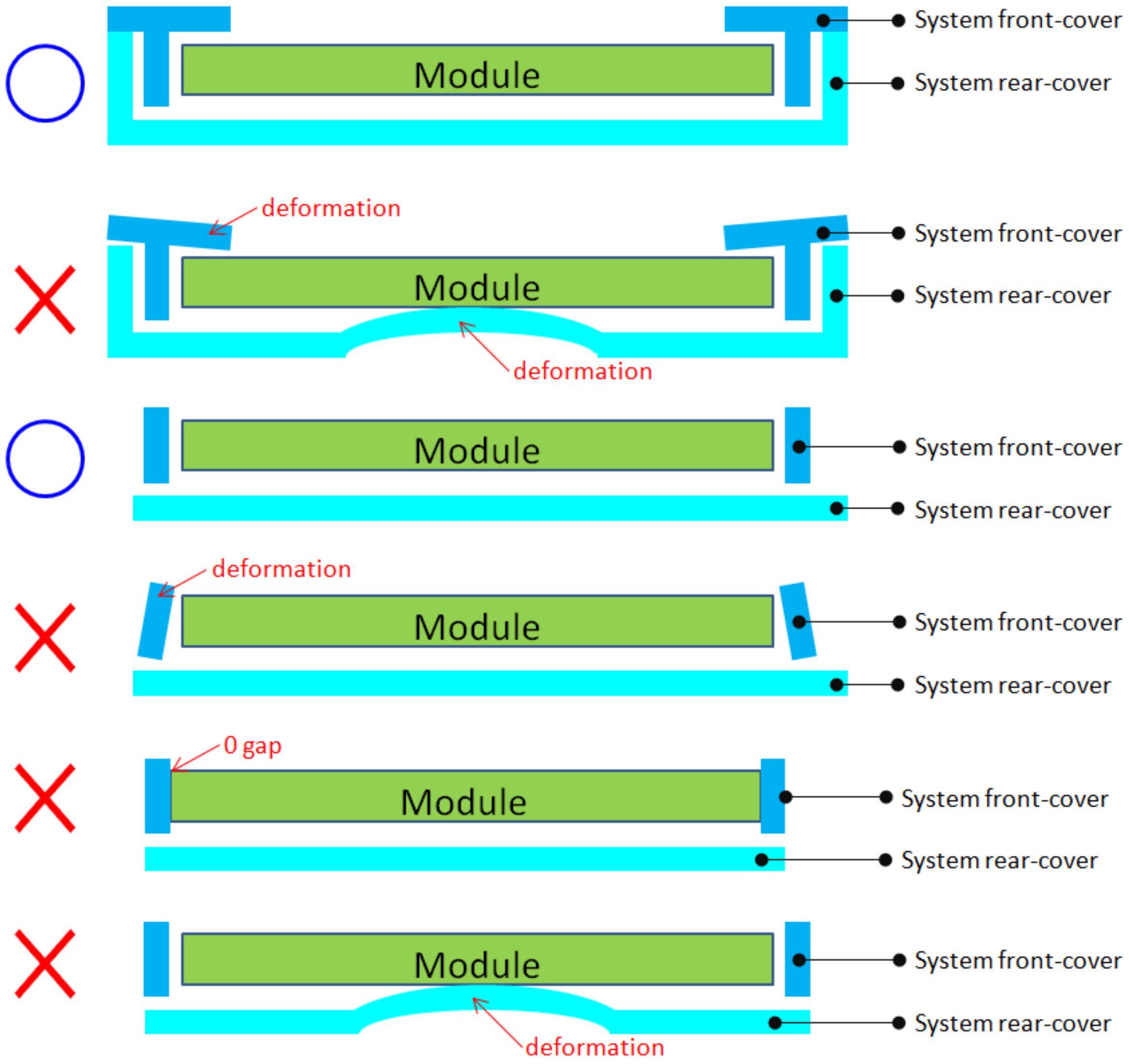


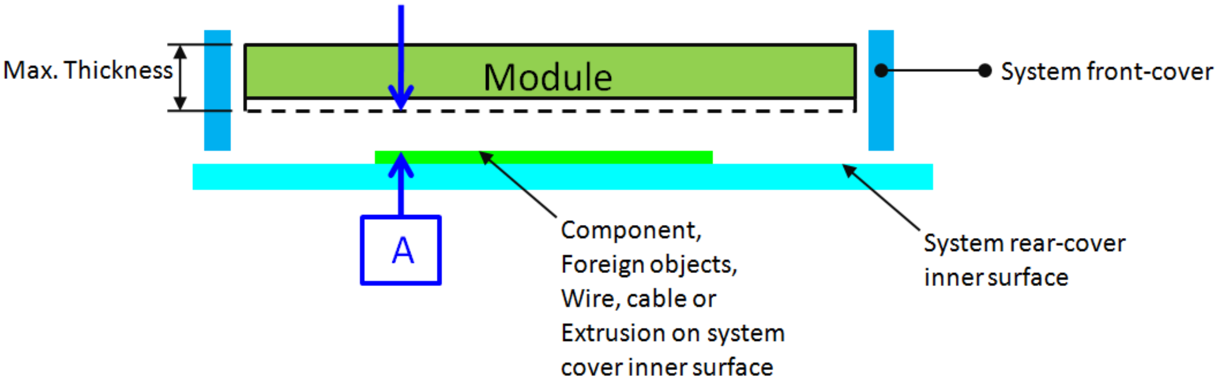
Definition	a. To prevent from abnormal display & white spot after mechanical test, we suggest using Tape/Sponge as medium between chassis and Module rear cover could reduce the occurrence of white spot. b. When using the Tape/Sponge, we suggest it be lay over between set chassis and Module rear cover. It is not recommended to add Tape/Sponge in separate location. Since each Tape/Sponge may act as pressure concentration location.

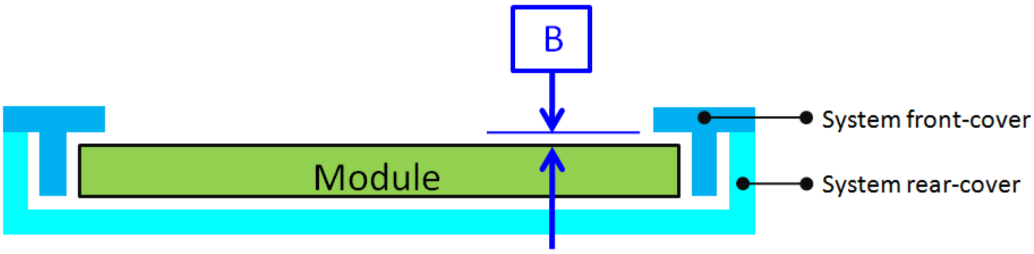
<table>
<tr><td>3</td><td>System inner surface examination</td></tr>
<tr><td colspan="2">
</td></tr>
<tr><td>Definition</td><td>a. The hatch area on Module PCBA should keep at least 1mm gap(X,Y,Z direction) to any structure with system cover inner surface.
b. Burr, Step, PCB protrusion may cause stress concentration. White spot may occur during reliability test.</td></tr>
</table>

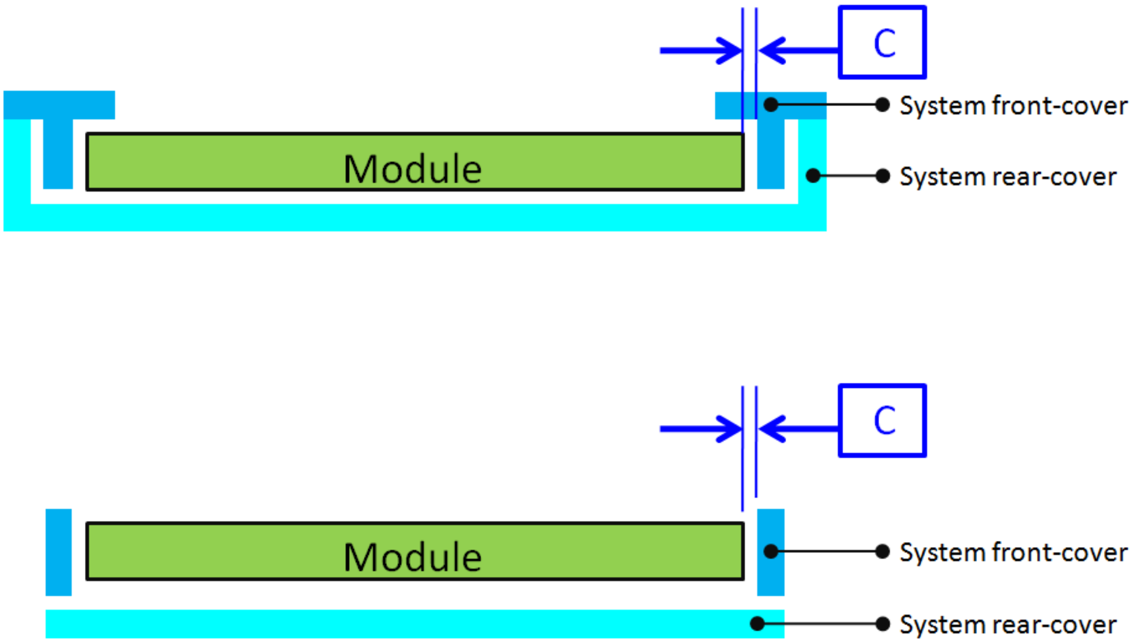
<table>
<tr><td>4</td><td>Material used for system rear-cover</td></tr>
<tr><td colspan="2">
</td></tr>
<tr><td>Definition</td><td>System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss position for module's bracket are deformed open-close test.
Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.</td></tr>
</table>

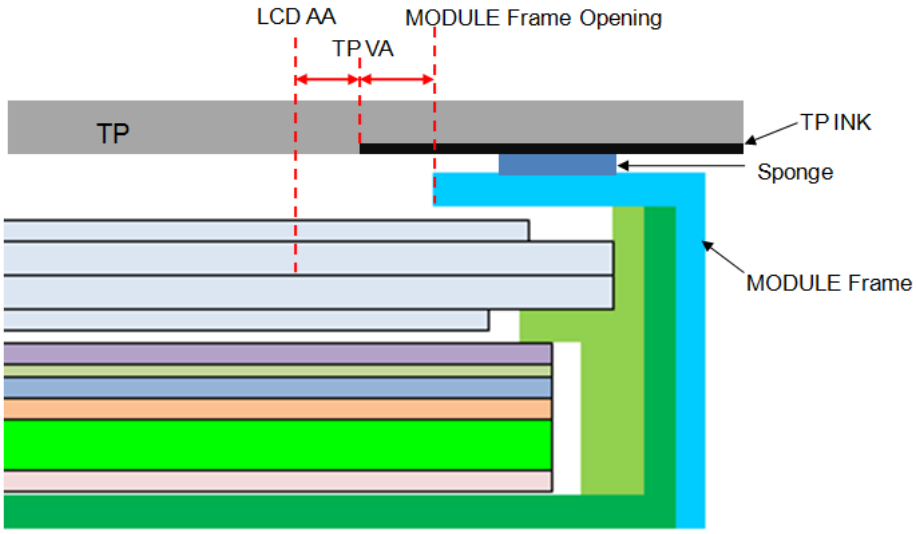
5	Assembly SOP examination for system front-cover with hook structure
	
Definition	To prevent panel crack during system front-cover assembly process with hook structure, it is not recommended to press panel or any location that relate directly to the panel.

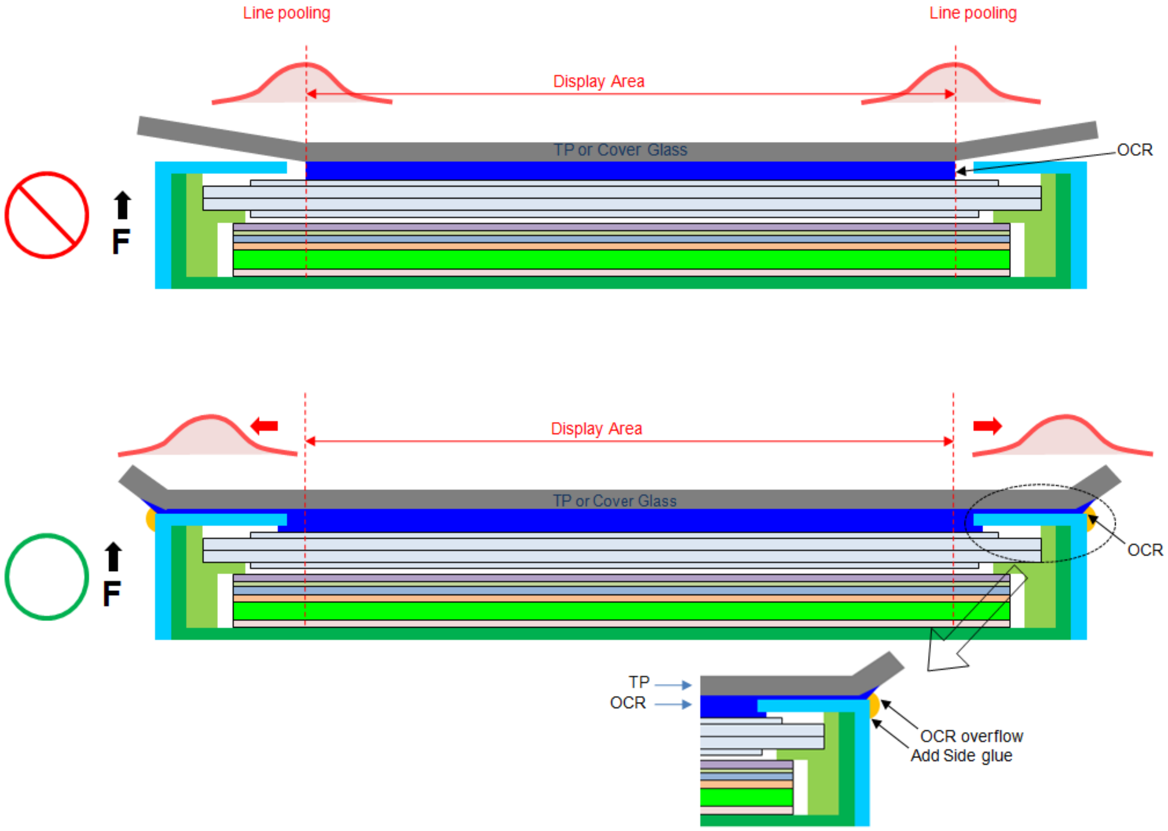
6	Permanent deformation of system cover after reliability test
	
Definition	System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell creak. Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

7	Design gap A between panel & any components on system rear-cover
	
Definition	System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell creak. Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

8	Design gap B between system front-cover & panel surface
	
Definition	Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended. Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

9	**Design gap C between panel & system front-cover or protrusions**
	
Definition	Gap between panel & system front-cover or protrusions is needed to prevent shock test failure. Because system front-cover or protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur. The gap should be large enough to absorb the maximum displacement during the test. Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

10	**Design distance between TP AA to LCD AA**
	
Definition	TP VA should avoid TP ink area covering LCD AA or causing the module frame to be exposed.

11	**Use OCR Lamination**
	
Definition	1.OCR glue as possible beyond module, in order to avoid Line Pooling 2.Add side glue to avoid Line Pooling