

**MODEL NO :** P2130QXF1MA00  
**SPEC VERSION :** V1.2  
**ISSUED DATE:** 2024-5-30

**Preliminary Specification**  
 **Final Product Specification**

**Customer :** \_\_\_\_\_

Approved by	Notes

**TIANMA Confirmed :**

Prepared by	Checked by	Approved by
Zhou Jie	Zhu Guanchen	Zhu Guanchen

This technical specification is subjected to change without notice

## Table of Contents

Table of Contents .....	2
Record of Revision .....	3
1 General Specifications .....	4
2 Input/Output Terminals .....	5
3 Absolute Maximum Ratings .....	11
4 Mechanical Characteristics .....	12
5 Electrical Characteristics .....	12
6 Timing Chart .....	21
7 Optical Characteristics .....	27
8 Environmental / Reliability Test .....	31
9 Mechanical Drawing .....	32
10 Packing Drawing .....	33
11 Precautions For Use of LCD Modules .....	36

**Record of Revision**

<b>Rev</b>	<b>Issued Date</b>	<b>Description</b>	<b>Editor</b>
1.0	2023-11-14	Preliminary Specification Released.	Zhou Jie
1.1	2024-3-13	P4: Response time Ton+Toff 35Typ. => 25 Typ. P27: View Angles Min. 70° => Min. 85° Response Time Typ. 35ms, Max. 45ms => Typ. 25ms, Max. 40ms Chromaticity tolerance ±0.5 => ±0.3 Luminance Min. 720 => 800	Zhou Jie
1.2	2024-5-30	P27: Update chromaticity red, green and blue.	Zhou Jie

## 1 General Specifications

Feature		Spec
Display Spec.	Size (inch)	21.3
	Resolution	1536(RGB)*2048
	Technology Type	SFT
	Pixel Configuration	RGB vertical stripe
	Pixel Pitch (mm)	0.2115 x 0.2115
	Display Mode	Transmissive, Normally Black
	Polarizer pencil-hardness	3H (min.) [by JIS K5600]
	Surface Treatment (Up Polarizer)	Antiglare
Optical Characteristics	Luminance (cd/m2)	900 Typ.
	Contrast ratio	2000:1 Typ.
	Response time Ton+Toff (ms)	25 Typ.
	Viewing angle R/L/U/D (Degree)	89/89/89/89 Typ. At the contrast ratio $\geq$ 10:1
Mechanical Characteristics	LCM (W x H x D) (mm)	336.1 x 453.0 x 10.5 Typ.
	Active Area (mm)	324.864 x 433.152
	With /Without TSP	Without TSP
	Weight (g)	1930g Typ.
	Backlight LED replacement	Not Available
Electrical Characteristics	Interface	4port LVDS, 10bit
	Power supply voltage (V)	LCD panel: 12.0 Typ.
		Backlight: 24.0 Typ.
	Color Depth	1,024 gray scales per 1 sub-pixel (10-bit), (3,072 gray scales per 1 pixel)
	Backlight LED driver	Build in
	Power consumption (W)	48.6 W (typ.) At checkered flag pattern, the maximum luminance control

Note 1 : Requirements on Environmental Protection: Q/S0002

Note 2 : LCM weight max. tolerance : +10%

## 2 Input/Output Terminals

### 2.1 TFT LCD Panel

CN1 socket (LCD module side): FI-RE51S-HF (Japan Aviation Electronics Industry Limited (JAE))  
 Adaptable plug: FI-RE51HL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	
3	GND	Ground	
4	DA0-	Pixel data A0	LVDS differential data input
5	DA0+		Note2
6	GND	Ground	Note1
7	DA1-	Pixel data A1	LVDS differential data input
8	DA1+		Note2
9	GND	Ground	Note1
10	DA2-	Pixel data A2	LVDS differential data input
11	DA2+		Note2
12	GND	Ground	Note1
13	CKA-	Pixel clock A	LVDS differential data input
14	CKA+		Note2
15	GND	Ground	Note1
16	DA3-	Pixel data A3	LVDS differential data input
17	DA3+		Note2
18	GND	Ground	Note1
19	DA4-	Pixel data A4	LVDS differential data input
20	DA4+		Note2
21	GND	Ground	Note1
22	DB0-	Pixel data B0	LVDS differential data input
23	DB0+		Note2
24	GND	Ground	Note1
25	DB1-	Pixel data B1	LVDS differential data input
26	DB1+		Note2
27	GND	Ground	Note1
28	DB2-	Pixel data B2	LVDS differential data input
29	DB2+		Note2
30	GND	Ground	Note1
31	CKB-	Pixel clock B	LVDS differential data input
32	CKB+		Note2
33	GND	Ground	Note1
34	DB3-	Pixel data B3	LVDS differential data input
35	DB3+		Note2
36	GND	Ground	Note1
37	DB4-	Pixel data B4	LVDS differential data input
38	DB4+		Note2
39	GND	Ground	Note1

Pin No.	Symbol	Signal	Remarks
40	GND	Ground	Note1
41	RSVD	-	For internal use, Keep this pin Open.
42	RSVD	-	For internal use, Keep this pin Open.
43	RSVD	-	For internal use, Keep this pin Open.
44	RSVD	-	For internal use, Keep this pin Open.
45	GND	Ground	Note1
46	GND	Ground	Note1
47	GND	Ground	Note1
48	RSVD	-	For internal use, Keep this pin Open.
49	RSVD	-	For internal use, Keep this pin Open.
50	RSVD	-	For internal use, Keep this pin Open.
51	GND	Ground	Note1

Note1: All GND terminals should be used without any non-connected lines.

Note2: Twist pair wires with  $100\Omega$  (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN2 socket (LCD module side): FI-RE41S-HF (Japan Aviation Electronics Industry Limited (JAE))  
 Adaptable plug: FI-RE41HL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	
3	GND	Ground	
4	DC0-	Pixel data C0	LVDS differential data input Note2
5	DC0+		
6	GND	Ground	Note1
7	DC1-	Pixel data C1	LVDS differential data input Note2
8	DC1+		
9	GND	Ground	Note1
10	DC2-	Pixel data C2	LVDS differential data input Note2
11	DC2+		
12	GND	Ground	Note1
13	CKC-	Pixel clock C	LVDS differential data input Note2
14	CKC+		
15	GND	Ground	Note1
16	DC3-	Pixel data C3	LVDS differential data input Note2
17	DC3+		
18	GND	Ground	Note1
19	DC4-	Pixel data C4	LVDS differential data input Note2
20	DC4+		
21	GND	Ground	Note1
22	DD0-	Pixel data D0	LVDS differential data input Note2
23	DD0+		
24	GND	Ground	Note1
25	DD1-	Pixel data D1	LVDS differential data input Note2
26	DD1+		
27	GND	Ground	Note1
28	DD2-	Pixel data D2	LVDS differential data input Note2
29	DD2+		
30	GND	Ground	Note1
31	CKD-	Pixel clock D	LVDS differential data input Note2
32	CKD+		
33	GND	Ground	Note1
34	DD3-	Pixel data D3	LVDS differential data input Note2
35	DD3+		
36	GND	Ground	Note1
37	DD4-	Pixel data D4	LVDS differential data input Note2
38	DD4+		
39	GND	Ground	Note1
40	GND	Ground	Note1
41	GND	Ground	Note1

Note1: All GND terminals should be used without any non-connected lines.

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN3 socket (LCD module side): 53261-1271 (MOLEX Inc.)  
Adaptable plug: 51021-1200 (MOLEX Inc.)

Pin No.	Symbol	Function	Description
1	GND	Signal ground	Note1
2			
3			
4			
5			
6			
7	VDD	Power supply	Note1
8			
9			
10			
11			
12			

Note1: All VDD and GND terminals should be used without any non-connected lines.

## 2.2 Backlight

CN201 socket (LCD module side): DF3EA-10P-2H(21) (HIROSE ELECTRIC Co., Ltd.)  
Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co., Ltd.)

Pin No	Symbol	Function	Description
1	GNDB	LED driver ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDBB		
7	VDBB	Power supply	Note1
8	VDBB		
9	VDBB		
10	VDBB		

Note1: All VDBB and GNDB terminals should be used without any non-connected lines.

Note2: Pin Numbering on module is opposite from pin numbering in the manufacturers datasheet"

CN202 socket (LCD module side): 53261-0971 (MOLEX Inc.)

Adaptable plug: 51021-0900 (MOLEX Inc.)

Pin No	Symbol	Function	Description
1	PWSEL	Selection of luminance control signal method	Note1, Note2
2	GNDB	LED driver ground	Note3
3	BRTP	BRTP signal	
4	BRTI	Luminance control terminal	Note1
5	BRTH		
6	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
7	N. C.	-	Keep this pin Open.
8	GNDB	LED driver ground	Note3
9	GNDB		

Note1: See "5.3 LUMINANCE CONTROL".

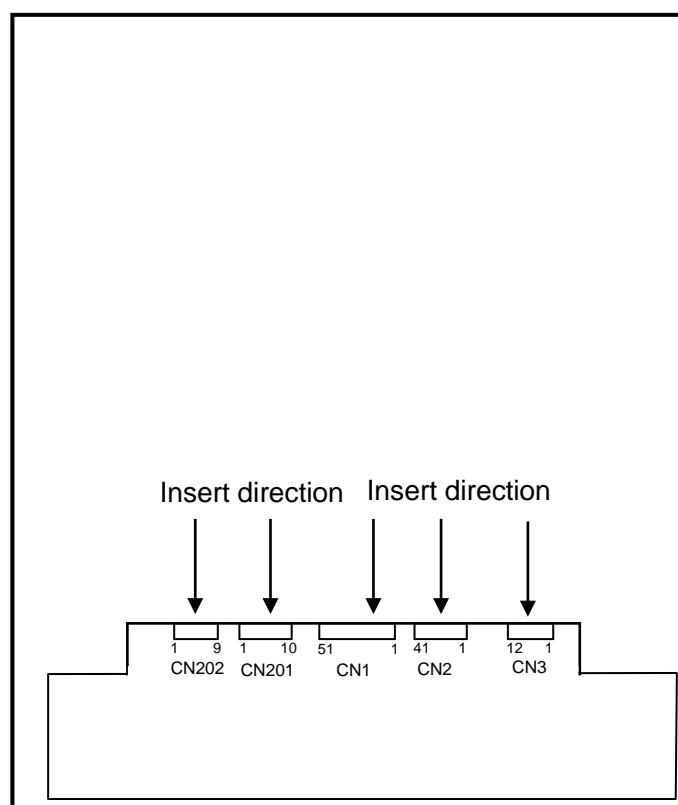
Note2: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

Note3: All GNDB terminals should be used without any non-connected lines.

Note4: Pin Numbering on module is opposite from connector pin numbering in the connector manufacturers datasheet".

**2.3 Positions of Socket**

Rear side



### 3 Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VDD	-0.3 to +15.0	V	Ta= 25°C
	LED driver	VDDB	-0.3 to +28.0	V	
Input voltage for signals	LCD panel signal processing board Note1	Vi	-0.3 to +2.8	V	VDD= 12.0V Ta= 25°C  VDDB= 24.0V Ta= 25°C
	LED driver	VBI	-0.3 to +1.5	V	
		VBP	-0.3 to +5.5	V	
		VBC	-0.3 to +5.5	V	
	PWSEL signal	VBS	-0.3 to +5.5	V	
Storage temperature		Tst	-20 to +60	°C	-
Operating temperature	Center of front surface	TopF	0 to +60	°C	Note2
	Edge of front surface	TopF	0 to +65	°C	Note2
	Edge of rear surface	TopR	0 to +70	°C	Note3
Relative humidity Note4, Note6		RH	≤ 95	%	Ta ≤ 40°C
			≤ 85	%	40°C < Ta ≤ 50°C
			≤ 55	%	50°C < Ta ≤ 60°C
Absolute humidity Note4, Note6		AH	≤ 70 Note5	g/m³	Ta > 60°C

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

Note2: Measured at LCD panel surface (including self-heat)

Note3: Measured at LCD module's rear shield surface (including self-heat)

Note4: No condensation

Note5: Water amount at Ta= 60°C and RH= 55%

Note6: Rapid change of humidity and temperature may cause degradation of the image quality.

## 4 Mechanical Characteristics

Parameter	Specification	Unit
Module size	336.1 ±0.5 (W) × 453.0 ±0.5 (H) ×10.5 ±0.5 ( D ) Note1	mm
Weight	1930 (typ.), 2130 (max.)	g

Note1: See " 9 Mechanical Drawing ".

## 5 Electrical Characteristics

### 5.1 Driving TFT LCD Panel

(Ta= 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply voltage	VDD	10.8	12.0	13.2	V	-
Power supply current	IDD	-	650 Note1	800 Note2	mA	At VDD=12.0V
Permissible ripple voltage	VRP	-	-	200	mVp-p	for VDD Note3,4,5
Differential input threshold voltage	High	VTH	-	-	+100	mV
	Low	VTL	-100	-	-	mV
Input voltage swing	VI	100	-	600	mV	Note7
Terminating resistance	RT	-	100	-	Ω	-

Note1: Checkered flag pattern [by IEC 61747-6]

Note2: Pattern for maximum current

Note3: This product works even if the ripple voltage levels are over the permissible values, but there might be noise on the display image.

Note4: The permissible ripple voltage includes spike noise.

Note5: The load variation influence does not include.

Note6: Common mode voltage for LVDS driver

Note7: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

## 5.2 Driving Backlight

Ta= 25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply voltage		VDDB	22.8	24.0	25.2	V	Note1
Power supply current		IDDB	-	1700	1800 Note2	mA	VDDB= 24.0V, At the maximum luminance control
Permissible ripple voltage		VRPB	-	-	200	mVp-p	for VDDB Note3, 4, 5
Input voltage for signals	BRTI signal	VBI	0	-	1.0	V	
	BRTP signal	VBPH	2.0	-	5.25	V	
		VBPL	0	-	0.8	V	
	BRTC signal	VBCH	2.0	-	5.25	V	
		VBCL	0	-	0.8	V	
	PWSE L signal	VBSH	2.0	-	5.25	V	
		VBSL	0	-	0.8	V	
Input current for signals	BRTI signal	IBI	-200	-	-50	uA	
	BRTP signal	IBPH	-	-	1,000	uA	
		IBPL	-600	-	-	uA	
	BRTC signal	IBCH	-	-	300	uA	
		IBCL	-300	-	-	uA	
	PWSE L signal	IPSH	-	-	1,000	uA	
		IPSL	-600	-	-	uA	
LED life time		Hr		50000		hour	Note 6

Note1: When designing of the power supply, take the measures for prevention of surge voltage.

Note2: This value excludes peak current such as overshoot current.

Note3: This product works even if the ripple voltage levels are over the permissible values, but there might be noise on the display image.

Note4: The permissible ripple voltage includes spike noise.

Note5: The power supply lines (VDDB and GND) may have ripple voltage during luminance control of LED. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on.

Note6: Optical performance should be evaluated at Ta=25°C. Only If LED is driven by high current, high ambient temperature &amp; humidity condition. The life time of LED will be reduced.

Operating life means brightness goes down to 50% of initial brightness. Typical operating life time is an estimated data.

### 5.3 Luminance Control

#### 5.3.1 Luminance control methods

(Ta= 25°C)

Method	Adjustment and luminance ratio	PWSEL terminal	BRTP terminal						
Variable resistor control Note1	<ul style="list-style-type: none"> <li>Adjustment The variable resistor (R) for luminance control should be <math>10k\Omega \pm 5\%</math>, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance. The resistor (R) must be connected between BRTH-BRTI terminals.</li> </ul>  <ul style="list-style-type: none"> <li>Luminance ratio Note3</li> </ul> <table border="1"> <thead> <tr> <th>Resistance</th> <th>Luminance ratio</th> </tr> </thead> <tbody> <tr> <td>0Ω</td> <td>10% (typ.)</td> </tr> <tr> <td>10kΩ</td> <td>100%</td> </tr> </tbody> </table>	Resistance	Luminance ratio	0Ω	10% (typ.)	10kΩ	100%	High or Open	Open
Resistance	Luminance ratio								
0Ω	10% (typ.)								
10kΩ	100%								
Voltage control Note1	<ul style="list-style-type: none"> <li>Adjustment Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance. Luminance is the maximum when BRTI terminal is Open.</li> <li>Luminance ratio Note3</li> </ul> <table border="1"> <thead> <tr> <th>BRTI Voltage (VBI)</th> <th>Luminance ratio</th> </tr> </thead> <tbody> <tr> <td>0V</td> <td>10% (typ.)</td> </tr> <tr> <td>1.0V</td> <td>100%</td> </tr> </tbody> </table>	BRTI Voltage (VBI)	Luminance ratio	0V	10% (typ.)	1.0V	100%		
BRTI Voltage (VBI)	Luminance ratio								
0V	10% (typ.)								
1.0V	100%								
Pulse width modulation (PWM) Note1 Note2 Note4	<ul style="list-style-type: none"> <li>Adjustment Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal. Keep BRTI and BRTH terminals Open when using PWM method.</li> <li>Luminance ratio Note3</li> </ul> <table border="1"> <thead> <tr> <th>Duty ratio</th> <th>Luminance ratio</th> </tr> </thead> <tbody> <tr> <td>0.21</td> <td>21% (typ.)</td> </tr> <tr> <td>1.0</td> <td>100%</td> </tr> </tbody> </table>	Duty ratio	Luminance ratio	0.21	21% (typ.)	1.0	100%	Low	BRTP signal
Duty ratio	Luminance ratio								
0.21	21% (typ.)								
1.0	100%								

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.

**Use Pulse width modulation (PWM) method, if interference noises appear on the display image!**

Note2: The LED driver will stop working, if the Low period of BRTP signal is more than 50ms while BRTC signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The LED driver will start to work when power is supplied again.

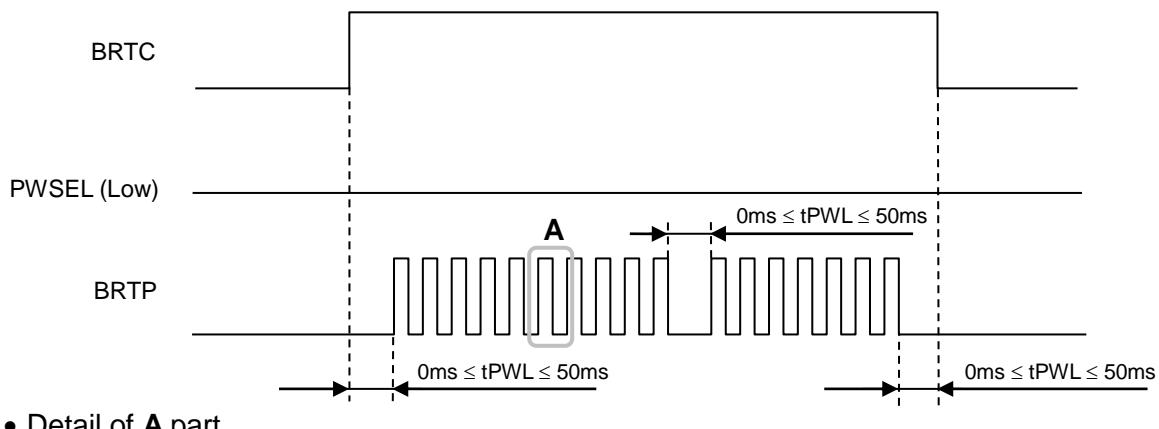
Note3: These data are the target values.

Note4: See "5.3.2 Detail of BRTP timing".

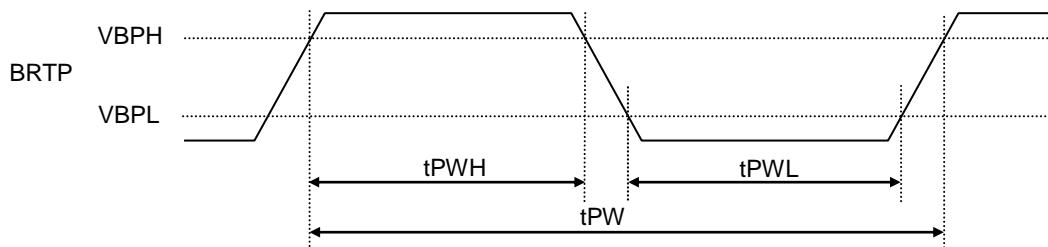
## 5.3.2 Detail of BRTP timing

## (1) Timing diagrams

- Outline chart



- Detail of A part



## (2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
PWM frequency	$f_{PWM}$	185	-	20k	Hz	Note1,2,3
PWM duty ratio	$DR_{PWM}$	1	-	100	%	$185 \leq f_{PWM} < 950$ (Hz) Note4,5
		21	-	100	%	$950 \leq f_{PWM} < 20K$ (Hz) Note4,5
PWM pulse width	$tPWH$	10	-	-	$\mu s$	Note1,4,5

Note1: Definition of parameters is as follows.

$$f_{PWM} = \frac{1}{tPW} , DR_{PWM} = \frac{tPWH}{tPW}$$

Note2: A recommended  $f_{PWM}$  value is as follows.

$$f_{PWM} = \frac{2n-1}{4} \times fv$$

(n= integer, fv= frame frequency of LCD module)

Note3: Depending on the frequency used, a noise may appear on the screen, please conduct a thorough evaluation.

Note4: While the BRTC signal is high, do not set the tPWH (PWM pulse width) is less than the minimum values. It may cause abnormal working of the backlight. In this case, turn the backlight off and then on again by BRTC signal.

Note5: Regardless of the PWM frequency, both PWM duty ratio and PWM pulse width must be always more than the minimum values.

## 5.4 Method of connection for LVDS transmitter

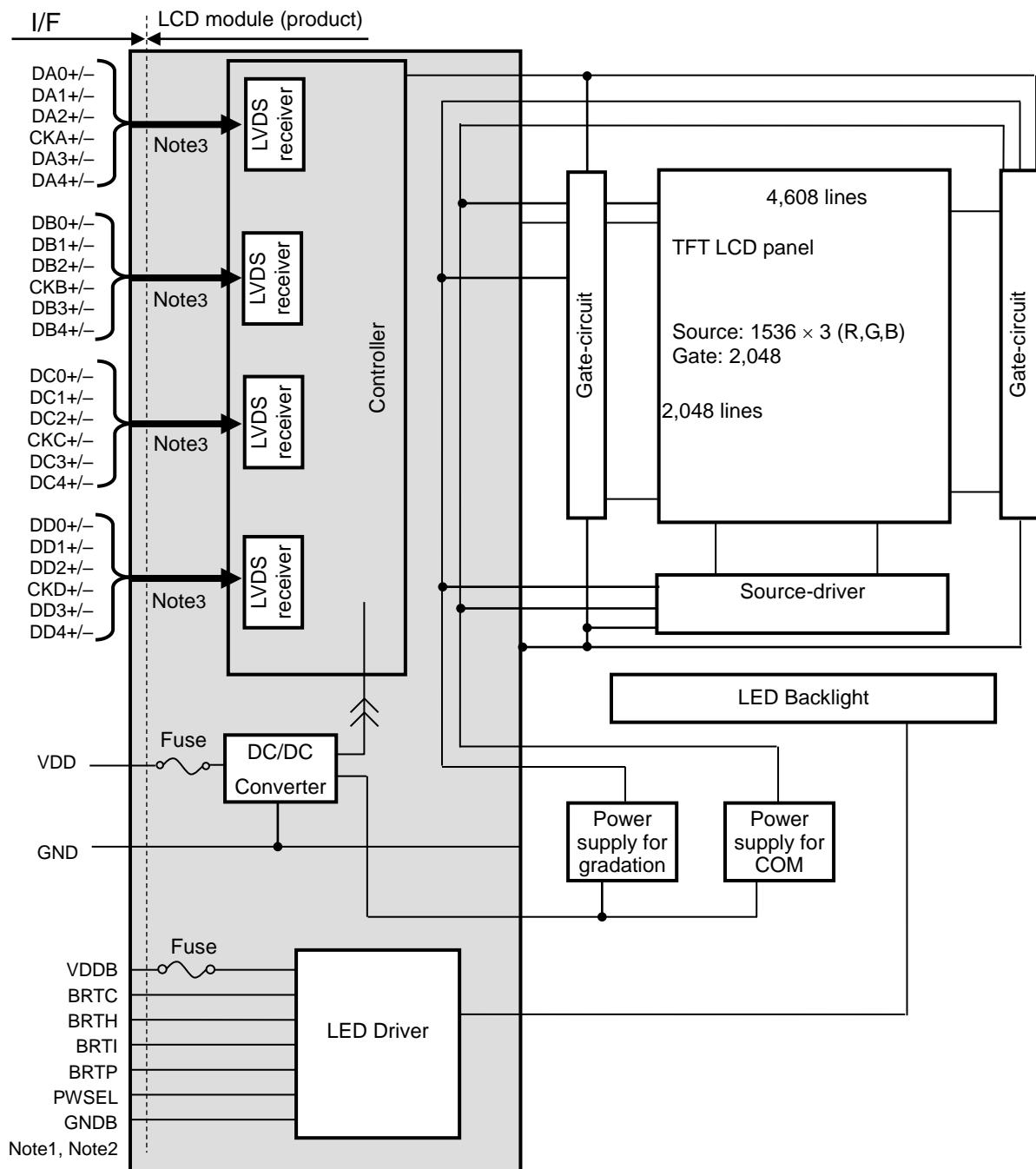
Bit mapping	Transmitter Pin Assignment		Output Connector
	THine THC63LVD1023B		
Pixel data A	RA4	R14	ATA- ATA+
	RA5	R15	
	RA6	R16	
	RA7	R17	
	RA8	R18	
	RA9	R19	
	GA4	G14	
	GA5	G15	
	GA6	G16	
	GA7	G17	
	GA8	G18	
	GA9	G19	
	BA4	B14	
	BA5	B15	
Pixel data B	BA6	B16	ATB- ATB+
	BA7	B17	
	BA8	B18	
	BA9	B19	
	Hsync	HSYNC	
	Vsync	VSYNC	
	DE	DE	
	RA2	R12	
	RA3	R13	
	GA2	G12	
	GA3	G13	
	BA2	B12	
	BA3	B13	
	N.C.	-	
Pixel data B	RA0	R10	ATD- ATD+
	RA1	R11	
	GA0	G10	
	GA1	G11	
	BA0	B10	
	BA1	B11	
	N.C.	-	
	CLK	CLK	
	RB4	R24	BTA- BTA+
	RB5	R25	
	RB6	R26	
	RB7	R27	
	RB8	R28	
	RB9	R29	
	GB4	G24	
	GB5	G25	
	GB6	G26	
	GB7	G27	
	GB8	G28	
	GB9	G29	
	BB4	B24	
	BB5	B25	
Pixel data B	BB6	B26	BTB- BTB+
	BB7	B27	
	BB8	B28	
	BB9	B29	
	Hsync	HSYNC	
	Vsync	VSYNC	
	DE	DE	
	RB2	R22	
	RB3	R23	
	GB2	G22	
	GB3	G23	
	BB2	B22	
	BB3	B23	
	N.C.	-	
Pixel data B	RB0	R20	BTD- BTD+
	RB1	R21	
	GB0	G20	
	GB1	G21	
	BB0	B20	
	BB1	B21	
	N.C.	-	
	CLK	CLK	
	BTE-	BTE+	BTE- BTE+
	31	CKB-	
	32	CKB+	
	34	DB3-	
	35	DB3+	
	37	DB4-	
	38	DB4+	
	22	DB0-	
	23	DB0+	
	25	DB1-	
	26	DB1+	
	28	DB2-	
	29	DB2+	
	30	DB3-	
	31	DB3+	
	32	DB4-	
	33	DB4+	
	13	CKA-	
	14	CKA+	
	4	DA0-	
	5	DA0+	
	7	DA1-	
	8	DA1+	
	10	DA2-	
	11	DA2+	
	16	DA3-	
	17	DA3+	
	19	DA4-	
	20	DA4+	

Note1: Twist pair wires with  $100\Omega$  (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

	Bit mapping	Transmitter Pin Assignment		Output Connector	Note1	CN2
		THine THC63LVD1023B				
Pixel data C	RC4	R14		CTA- CTA+	→	
	RC5	R15			→	4 DC0-
	RC6	R16				5 DC0+
	RC7	R17				
	RC8	R18				
	RC9	R19				
	GC4	G14				
	GC5	G15				
	GC6	G16				
	GC7	G17			→	7 DC1-
	GC8	G18			→	8 DC1+
	GC9	G19		CTB- CTB+		
	BC4	B14				
	BC5	B15				
	BC6	B16				
	BC7	B17				
	BC8	B18			→	10 DC2-
	BC9	B19			→	11 DC2+
	Hsync	Hsync				
	Vsync	Vsync				
	DE	DE				
Pixel data D	RC2	R12		CTD- CTD+	→	
	RC3	R13			→	
	GC2	G12				
	GC3	G13				
	BC2	B12				
	BC3	B13		CTE- CTE+	→	
	N.C.	-			→	
	RC0	R10				
	RC1	R11				
	GC0	G10			→	19 DC4-
	GC1	G11			→	20 DC4+
	BC0	B10				
	BC1	B11				
	N.C.	-				
	CLK	CLK		CTCLK- CTCLK+	→	
Pixel data D	RD4	R24		DTA- DTA+	→	
	RD5	R25			→	
	RD6	R26				
	RD7	R27				
	RD8	R28				
	RD9	R29		DTB- DTB+	→	
	GD4	G24			→	
	GD5	G25				
	GD6	G26				
	GD7	G27				
	GD8	G28				
	GD9	G29				
	BD2	B24				
	BD3	B25				
	BD6	B26		DTC- DTC+	→	
	BD7	B27			→	
	BD8	B28				
	BD9	B29				
	Hsync	Hsync				
Pixel data D	Vsync	Vsync		DTD- DTD+	→	
	DE	DE			→	
	RD2	R22				
	RD3	R23				
	GD2	G22				
	GD3	G23		DTE- DTE+	→	
	BD2	B22			→	
	BD3	B23				
	N.C.	-				
	RD0	R20				
	RD1	R21				
	GD0	G20				
	GD1	G21				
	BD0	B20				
	BD1	B21				
	N.C.	-				
	CLK	CLK		DTCLK- DTCLK+	→	

Note1: Twist pair wires with  $100\Omega$  (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

## 5.5 Block Diagram



Note1: Relations between GND (Signal ground), FG (Frame ground) and GNDB (LED driver ground) in the LCD module are as follows.

GND - FG	Connected
GND - GNDB	Not connected
FG - GNDB	Not connected

Note2: GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that these grounds to be connected together in customer equipment.

Note3: Each pair of the LVDS signal lines has  $100\Omega$  terminating resistance.

Note3: Each pair of the LVDS signal has a  $100\Omega$  terminating resistance.

**5.6 Fuse**

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16202ABTP	KAMAYA	2.A	4A@5S	Note1
			36V		
VDBB	CRUCQ12LV3 A63V	CONQUER	3A	6A@5S	
			63V		

Note1: The power supply's rated current must be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

## 6 Timing Chart

### 6.1 Timing Characteristics

(Note1, Note2, Note3, Note4)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks	
CLK	Frequency	1/ tc	54	55.7	58	MHz	17.9ns (typ.)	
	Duty ratio	-				-	-	
	Rise time, Fall time	-				ns	-	
DATA	CLK-DAT	Setup time	-			ns	-	
		A	Hold time	-		ns	-	
	Rise time, Fall time		-			ns	-	
DE	Horizontal	Cycle	th	-	8.03	-	μs	
				442	448	518	CLK	
	Vertical (One frame)	Display period	thd	384			CLK	
							-	
	CLK-DE	Cycle	tv	-	16.7	-	ms	
				2067	2,074	2081	H	
	Setup time		-	See the data sheet of LVDS transmitter.			60.0Hz (typ.)	
	Hold time		-				-	
	Rise time, Fall time		-				-	

Note1: Definition of parameters is as follows.

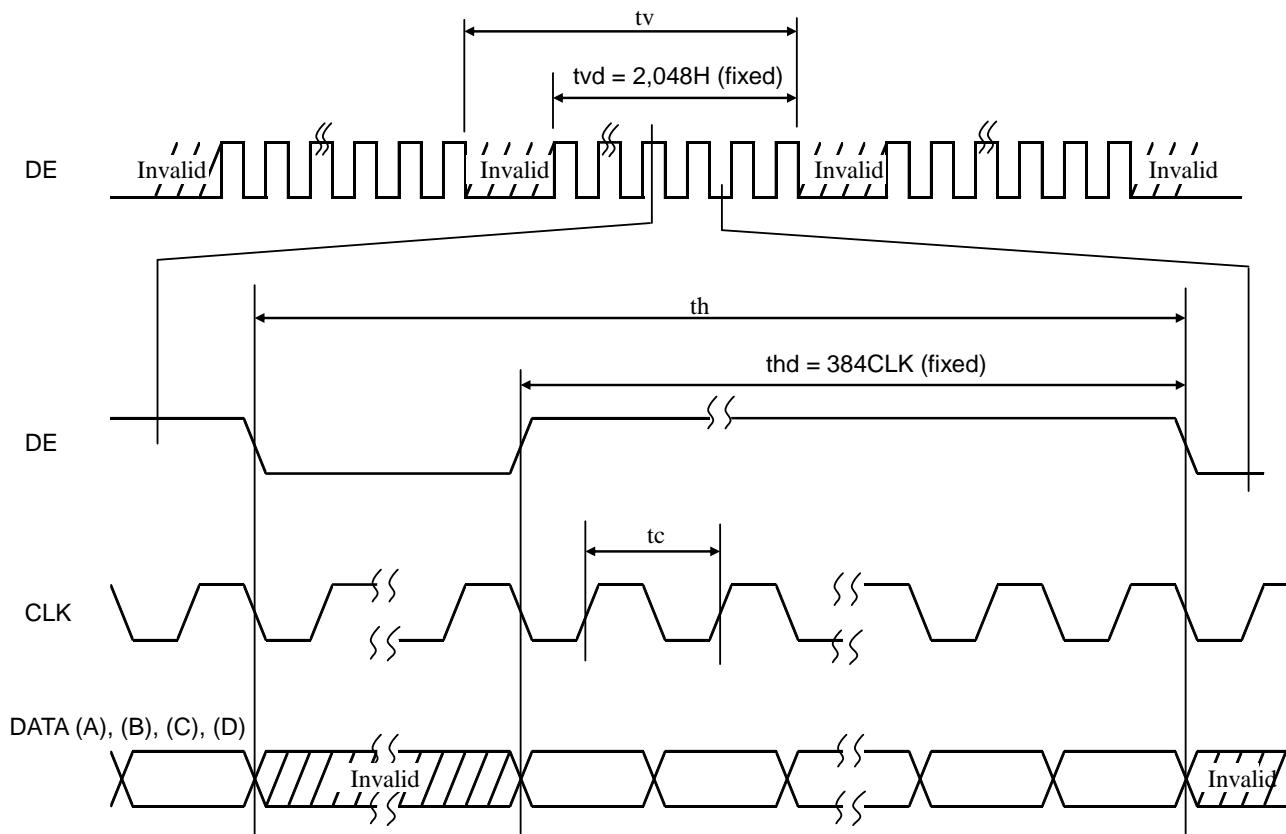
tc= 1CLK, th= 1H

Note2: See the data sheet of LVDS transmitter.

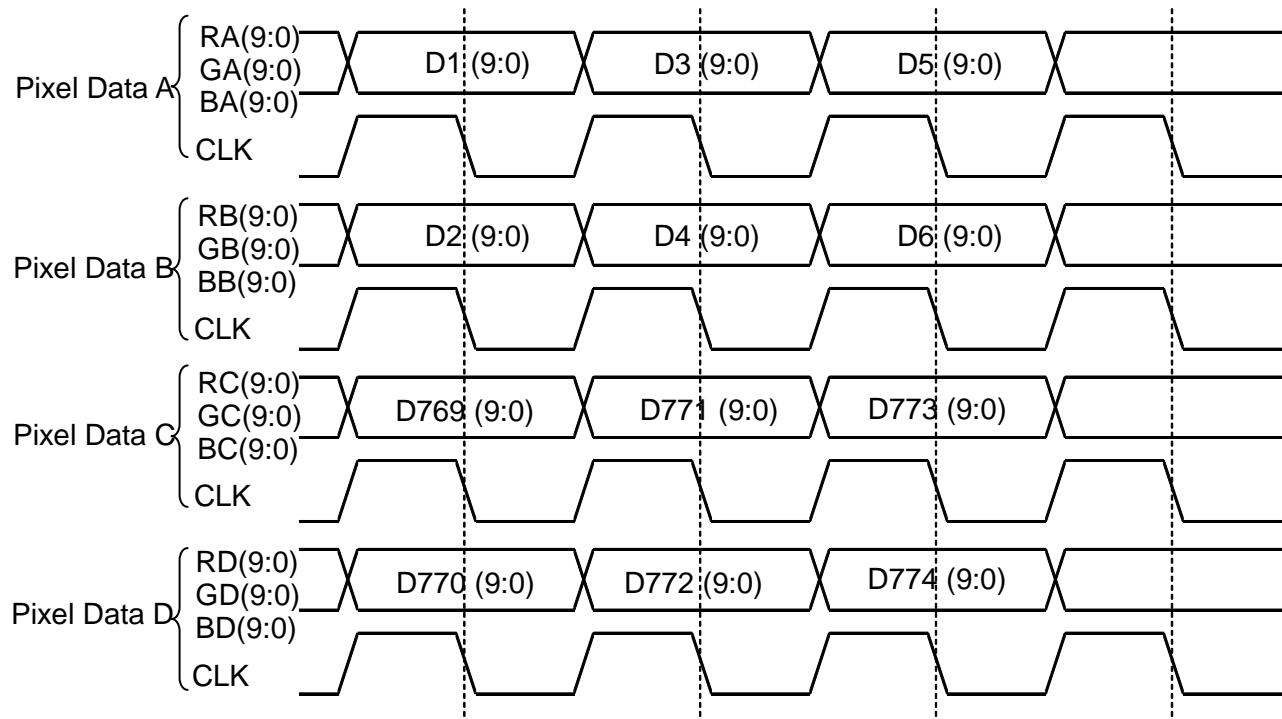
Note3: Vertical cycle (tv) should be specified in integral multiple of Horizontal cycle (th).

Note4: Definition for landscape

## 6.2 Input Signal Timing Chart



## 6.3 Input Data Mapping



The information contained herein is the exclusive property of Tianma Microelectronics Co., Ltd., and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Tianma Microelectronics Co., Ltd..

#### 6.4 Display Colors and Input Data Signals

This product can display 1,024 gray scales in each RGB sub-pixel and 3,072 gray scales per 1 pixel. Also the relation between display gray scale and input data signals is as follows.

Display gray scale		Data signal (0: Low level, 1: High level)																							
		RA9 RA8 RA7 RA6 RA5 RA4 RA3 RA2 RA1 RA0	GA9 GA8 GA7 GA6 GA5 GA4 GA3 GA2 GA1 GA0	BA9 BA8 BA7 BA6 BA5 BA4 BA3 BA2 BA1 BA0																					
		RB9 RB8 RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0	GB9 GB8 GB7 GB6 GB5 GB4 GB3 GB2 GB1 GB0	BB9 BB8 BB7 BB6 BB5 BB4 BB3 BB2 BB1 BB0																					
		RC9 RC8 RC7 RC6 RC5 RC4 RC3 RC2 RC1 RC0	GC9 GC8 GC7 GC6 GC5 GC4 GC3 GC2 GC1 GC0	BD9 BC8 BC7 BC6 BC5 BC4 BC3 BC2 BC1 BC0																					
		RD9 RD8 RD7 RD6 RD5 RD4 RD3 RD2 RD1 RD0	GD9 GD8 GD7 GD6 GD5 GD4 GD3 GD2 GD1 GD0	BD9 BD8 BD7 BD6 BD5 BD4 BD3 BD2 BD1 BD0																					
		Black	0 0	0 0	0 0																				
Left sub-pixel gray scale	dark	0 0	0 0	0 0																					
	↑	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	↓	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	bright	1 1 1 1 1 1 1 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0																					
	White	1 1	0 0	0 0																					
Center sub-pixel gray scale	Black	0 0	0 0	0 0																					
	dark	0 0	0 0	0 0																					
	↑	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	↓	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	bright	0 0	0 1	1 0																					
Right sub-pixel gray scale	White	0 0	0 1	1 0																					
	Black	0 0	0 0	0 0																					
	dark	0 0	0 0	0 0																					
	↑	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	↓	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	bright	0 0	0 0	0 0																					
	White	0 0	0 1	1 0																					

The information contained herein is the exclusive property of Tianma Microelectronics Co., Ltd., and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Tianma Microelectronics Co., Ltd..

## 6.5 Display Positions

		D (1, 1)      D (2, 1)			D (769, 1)      D (770, 1)		
		RA	GA	BA	RB	GB	BB
1		D(1, 1)	D(2, 1)	...	D(769, 1)	D(770, 1)	...
2		D(1, 2)	D(2, 2)	...	D(769, 2)	D(770, 2)	...
Y		•	•	•	•	•	•
		•	•	•	•	•	•
		•	•	•	•	•	•
2047		D(1, 2047)	D(2, 2047)	...	D(769, 2047)	D(770, 2047)	...
2048		D(1, 2048)	D(2, 2048)	...	D(769, 2048)	D(770, 2048)	...

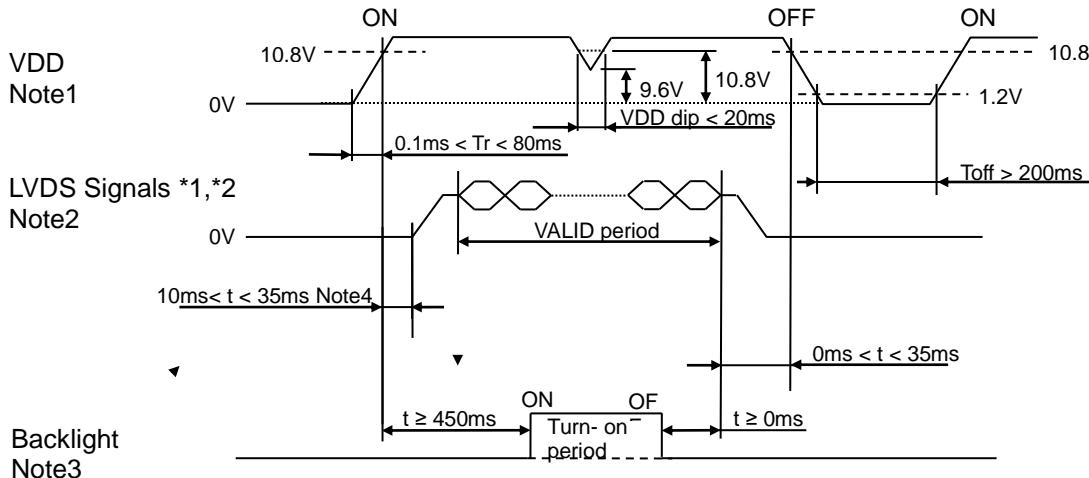
## 6.6 Scanning Direction

		1	2	1536		
		R G B	R G B	...	...	R G B
1		• • •	• • •	• • •	• • •	• • •
2,048		R G B	R G B	...	...	R G B

Note1: Definition for portrait

## 6.7 Power On/Off Sequence

### 6.7.1 LCD panel signal processing board

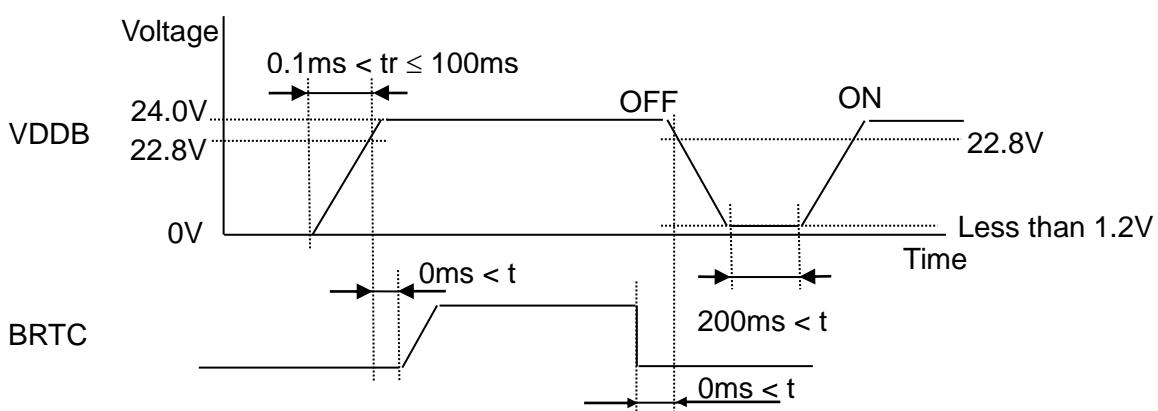


\*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

\*2: LVDS signals should be measured at the terminal of  $100\ \Omega$  resistance.

- Note1: If there is a voltage variation (voltage drop) at the rising edge of VDD below 10.8V, there is a possibility that a product does not work due to a protection circuit.
- Note2: LVDS signals must be set to Low or High-impedance, except the VALID period (See above sequence diagram), in order to avoid the circuitry damage. If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. If a customer stops the display and function signals, VDD also must be shut down.
- Note3: The backlight should be turned on within the turn-on period, in order to avoid unstable data display.
- Note4: After turning VDD on, terminal voltages on LVDS input terminals (\*1) will rise. This is caused by initial operation of the product.

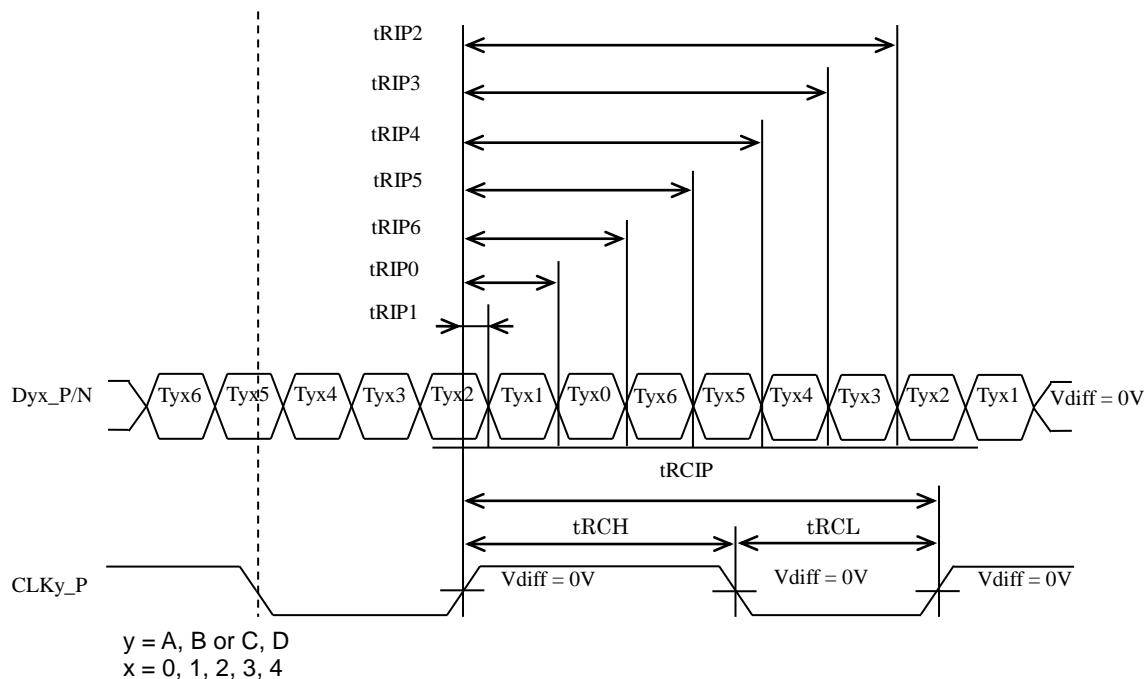
### 6.7.2 LED Driver



- Note1: If  $tr$  is more than 100ms, the backlight will be turned off by a protection circuit for LED driver.
- Note2: When VDDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

## 6.8 LVDS Rx AC SPEC

Symbol	Parameter	min.	typ.	max.	Unit
t <sub>RCIP</sub>	CKy_+ Period	17.24	-	18.52	ns
t <sub>RCIH</sub>	CKy_+ High pulse width	-	$\frac{4}{7} t_{RCIP}$	-	ns
t <sub>RCIL</sub>	CKy_+ Low pulse width	-	$\frac{3}{7} t_{RCIP}$	-	ns
t <sub>RMG</sub>	Receiver Data Input Margin CLK = 56MHz	-0.676	-	0.676	ns
t <sub> RIP1</sub>	Input Data Position 0	-  t <sub>RMG</sub>	0.0	+  t <sub>RMG</sub>	ns
t <sub> RIP0</sub>	Input Data Position 1	$\frac{t_{RCIP}}{7} -   t_{RMG}  $	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7} +   t_{RMG}  $	ns
t <sub> RIP6</sub>	Input Data Position 2	$2 \frac{t_{RCIP}}{7} -   t_{RMG}  $	$2 \frac{t_{RCIP}}{7}$	$2 \frac{t_{RCIP}}{7} +   t_{RMG}  $	ns
t <sub> RIP5</sub>	Input Data Position 3	$3 \frac{t_{RCIP}}{7} -   t_{RMG}  $	$3 \frac{t_{RCIP}}{7}$	$3 \frac{t_{RCIP}}{7} +   t_{RMG}  $	ns
t <sub> RIP4</sub>	Input Data Position 4	$4 \frac{t_{RCIP}}{7} -   t_{RMG}  $	$4 \frac{t_{RCIP}}{7}$	$4 \frac{t_{RCIP}}{7} +   t_{RMG}  $	ns
t <sub> RIP3</sub>	Input Data Position 5	$5 \frac{t_{RCIP}}{7} -   t_{RMG}  $	$5 \frac{t_{RCIP}}{7}$	$5 \frac{t_{RCIP}}{7} +   t_{RMG}  $	ns
t <sub> RIP2</sub>	Input Data Position 6	$6 \frac{t_{RCIP}}{7} -   t_{RMG}  $	$6 \frac{t_{RCIP}}{7}$	$6 \frac{t_{RCIP}}{7} +   t_{RMG}  $	ns



The information contained herein is the exclusive property of Tianma Microelectronics Co., Ltd., and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Tianma Microelectronics Co., Ltd..

## 7 Optical Characteristics

Ta=25°C

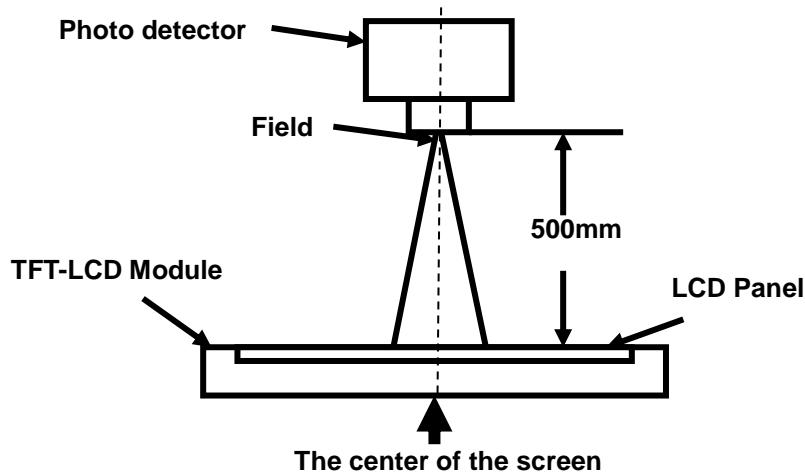
Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles	θT	CR ≥ 10	85	89	-	Degree	Note 2
	θB		85	89	-		
	θL		85	89	-		
	θR		85	89	-		
Contrast Ratio	CR	θ=0°	1400	2000	-	-	Note1 Note3
Response Time	T <sub>ON</sub> +T <sub>OFF</sub>	25°C	-	25	40	ms	Note1 Note4
Chromaticity	White	x	Backlight is on	Typ-0.03	0.314	Typ+0.03	Note5 Note1
					0.326		
	Red	x			0.657		
		y			0.333		
	Green	x			0.328		
		y			0.621		
	Blue	x			0.148		
		y			0.061		
Uniformity	LU1	White (1023/1023gray)	80	-	-	%	Note1 Note6
	LU2	Gray (102/1023gray)	-	-	20		
	LU3	Gray (816/1023gray)	-	-	20		
NTSC	-	-	67	72	-	%	Note 5
Luminance	L	White (1023/1023gray)	800	900	-	cd/m <sup>2</sup>	Note1 Note7

## Test Conditions:

1. The ambient temperature is 25±2°C. humidity is 65±7%. PWM duty ratio is 100%.
2. The test systems refer to Note 1 and Note 2.
3. Contrast Ratio, Chromaticity, Uniformity, and Luminance is measured by SR-UL, SR-3AR or equivalent.
4. Response Time is measured by TRD-100, LCD-5200 or equivalent.

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 20 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system.

Viewing angle is measured at the center point of the LCD by LCD5200.

The 12 o'clock direction is upper side of outline in "**9 Mechanical Drawing**".

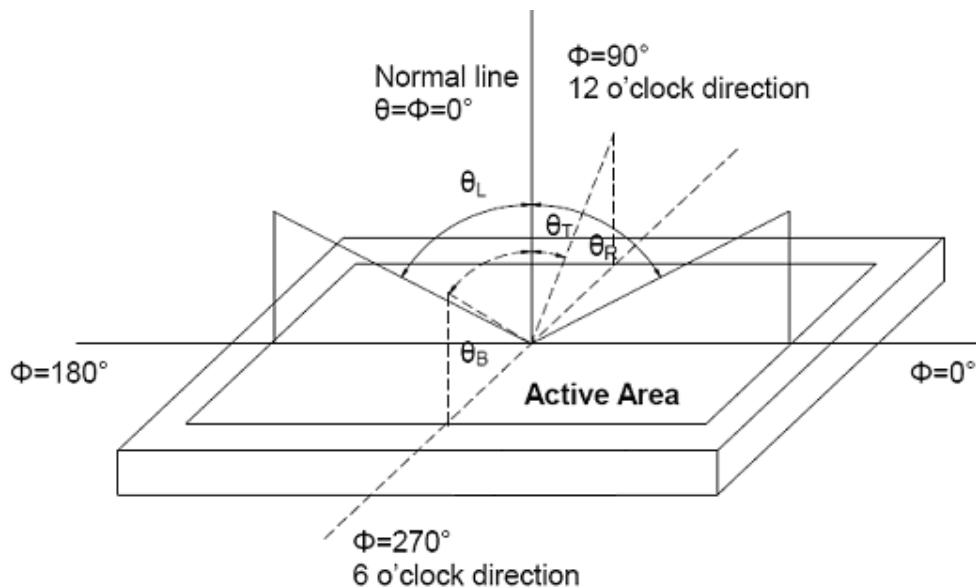


Fig. 1 Definition of viewing angle

## Note 3: Definition of contrast ratio

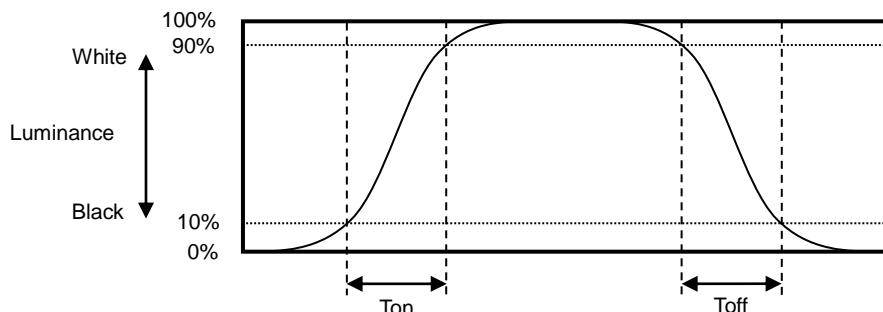
The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

## Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "Black" state and "White" state. Rise time (Ton) is the time between photo detector output intensity changed from 10% to 90%. And fall time (Toff) is the time between photo detector output intensity changed from 90% to 10%.

Product surface temperature: TopF= 29°C.



## Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

## Note 6: Definition of Luminance Uniformity

LU1:

Active area is divided into 9 measuring areas (Refer Fig. 2).

$$\text{Luminance Uniformity(LU)} = \text{Lmin} / \text{Lmax}$$

L-----Active area length W----- Active area width

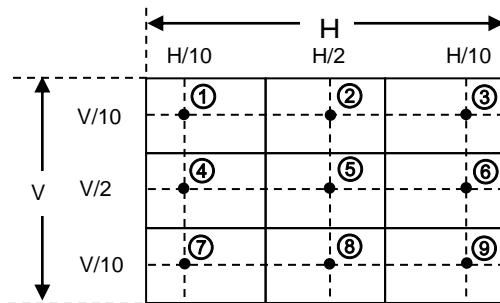


Fig. 2 Definition of uniformity

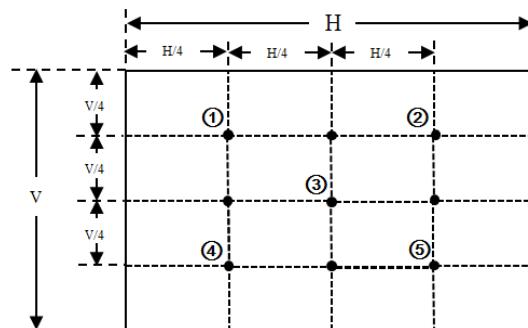
Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

The Gray luminance uniformity is calculated by using following formula.

$$\text{LU2/ LU3} = 200^* \frac{\text{Maximum luminance from } ① \text{ to } ⑤ - \text{Minimum luminance from } ① \text{ to } ⑤}{\text{Maximum luminance from } ① \text{ to } ⑤ + \text{Minimum luminance from } ① \text{ to } ⑤}$$

The luminance is measured at near the 5 points shown below.



## Note 7: Definition of Luminance :

Measure the luminance of white state at center point.

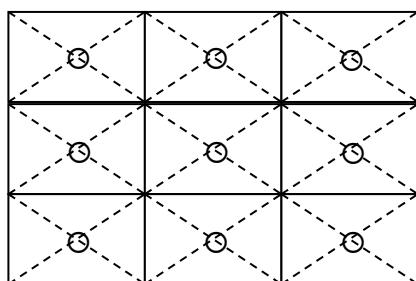
## 8 Environmental / Reliability Test

Test item	Condition	Judgment	Note1
High temperature and humidity (Operation)	① $60 \pm 2^\circ\text{C}$ , RH= 60%, 240hours ② Display data is white.		
Heat cycle (Operation)	① $0 \pm 3^\circ\text{C}$ 1hour $60 \pm 3^\circ\text{C}$ 1hour ② 50cycles, 4hours/cycle ③ Display data is white.	No display malfunctions Note2	
Thermal shock (Non operation)	① $-20 \pm 3^\circ\text{C}$ 30minutes $60 \pm 3^\circ\text{C}$ 30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.		
Vibration (Non operation)	① 5 to 100Hz, $11.76\text{m/s}^2$ ② 1 minute/cycle ③ X, Y, Z directions ④ 10 times each direction	No display malfunctions	
Mechanical shock (Non operation)	① $294\text{m/s}^2$ , 11ms ② $\pm X, \pm Y, \pm Z$ directions ③ 3 times each direction	No physical damages	
ESD (Operation)	Contact Discharge ① 150pF, 330 $\mu\text{s}$ , $\pm 8\text{kV}$ ② 9 places on a panel surface Note3 ③ 25 times each place at 1 sec interval Air Discharge ① 150pF, 330 $\mu\text{s}$ , $\pm 15\text{kV}$ ② 9 places on a panel surface ③ 25times each place at 1 sec interval	No display malfunctions Note3	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: Luminance:  $600\text{cd/m}^2$  at luminance control.

Note3: See the following figure for discharge points



## 9 Mechanical Drawing

## 9.1 Mechanical Drawing Of LCM

The information contained herein is the exclusive property of Tianma Microelectronics Co., Ltd., and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Tianma Microelectronics Co., Ltd..

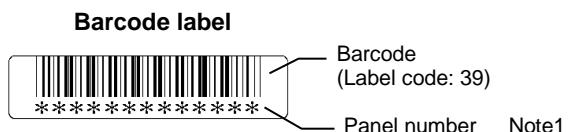
## 9.2 Markings

The marking is attached to this product.

### 9.2.1 Nameplate label



### 9.2.2 Barcode label

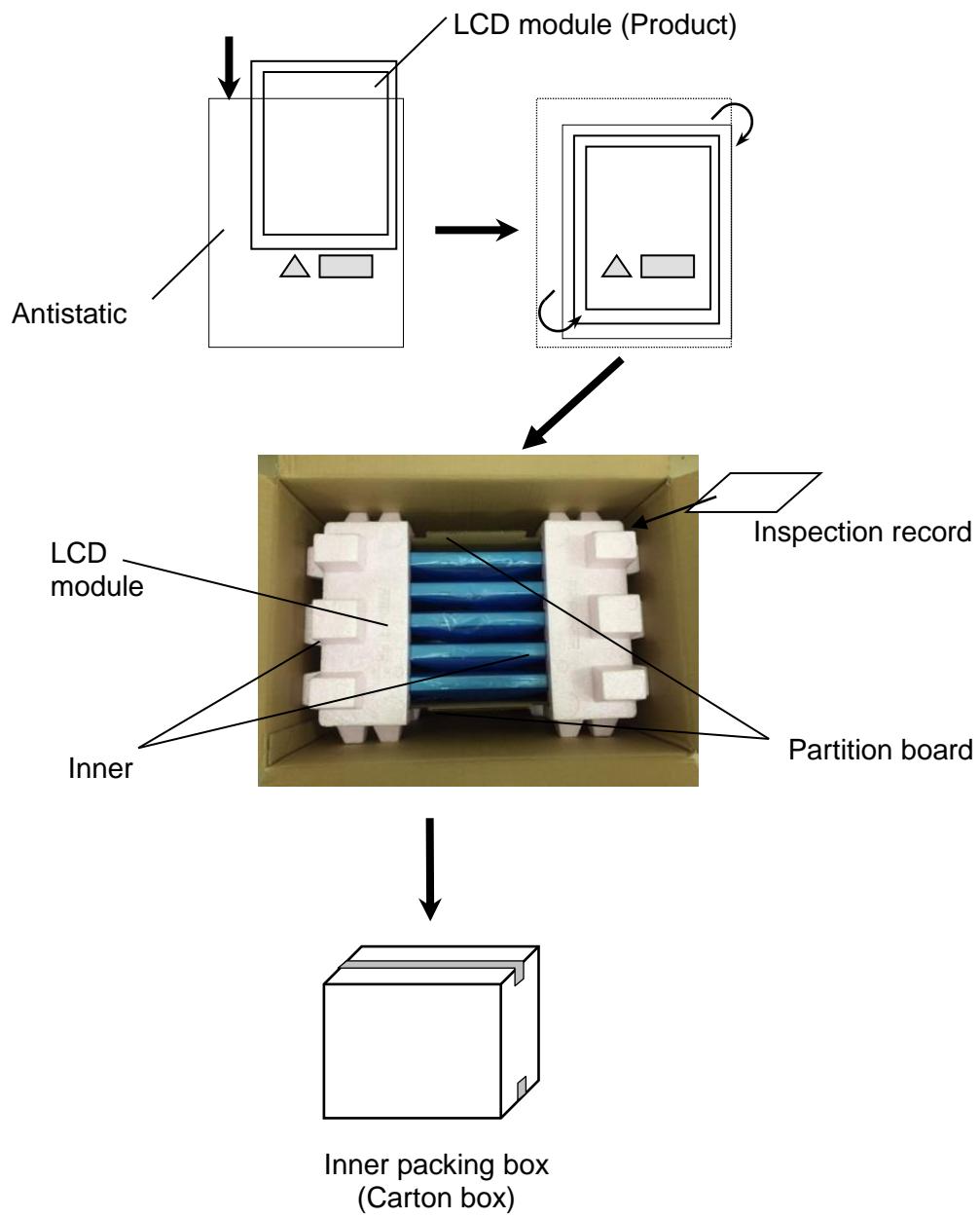


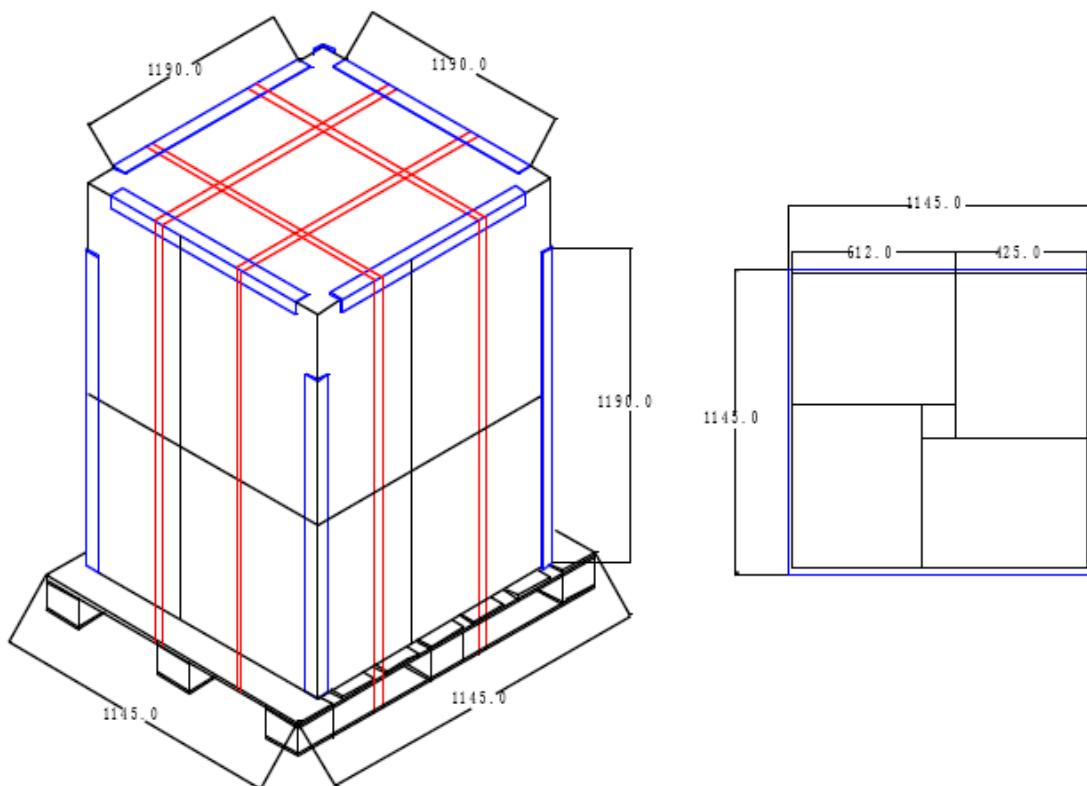
**Note1: Do not attach anything like another label on the nameplate label!**

## 10 Packing Drawing

No	Item	Model (Material)	Dimensions(mm)	Unit Weight(Kg)	Quantity	Remark
1	LCM module	TM213XDGP05-00	336.1x453.0x10.5	1.93	5	
2	Partition board	Corrugated paper	460x378	0.075	2	
3	Anti-static Bag	LD-PE	600x420	0.022	5	
4	EPP-Bottom	EPP	597x410x190	0.34	1	
5	EPP-Top	EPP	410x185x110	0.064	2	
6	Carton-inside	Corrugated paper	612x425x520	1.65	1	
7	Barcode Label	Paper	76x104	0.001	2	
8	Total weight	<b>12.03 ±10% kg</b>				

## 10.1 LCD Module Packing Method



**10.2 Stacking method (2 x 2 x 2)**

## 11 Precautions For Use of LCD Modules

### 11.1 Handling Precautions

- 11.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- 11.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
- 11.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- 11.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- 11.1.5 Do not get the polarizer contacted with Petroleum solvents, such as Hydrocarbon solvents, N-heptane .
- 11.1.6 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:
  - Isopropyl alcohol
  - Ethyl alcoholSolvents other than those mentioned above may damage the polarizer. Especially, do not use the following:
  - Water
  - Ketone
  - Aromatic solvents
- 11.1.7 Do not attempt to disassemble the LCD Module.
- 11.1.8 If the logic circuit power is off, do not apply the input signals.
- 11.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  - 11.1.8.1 Be sure to ground the body when handling the LCD Modules.
  - 11.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.
  - 11.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  - 11.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated
- 11.1.9 The torque for product mounting screws must never exceed (0.8) N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be  $\leq$  (7) mm.

### 11.2 Storage Precautions

- 11.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.
- 11.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0°C ~ 40°C      Relatively humidity:  $\leq$ 80%
- 11.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

**11.3 Transportation Precautions**

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.