SPECIFICATION

PRODUCT NO. : **TCXD050IBLMA-2**
VERSION : **Ver 1.1**
ISSUED DATE : **2020-5-6**

This module uses ROHS material

FOR CUSTOMER: _____

■: APPROVAL FOR SPECIFICATION
□: APPROVAL FOR SAMPLE

DATE	APPROVED BY

Xinli Optoelectronics :

Presented by	Reviewed by	Organized by
馮志文	趙春曉	王俊傑

Note:

1.Xinli Optoelectronics reserves the right to make changes without further notice to any products herein to improve reliability, function or design.

1. Revision Recode

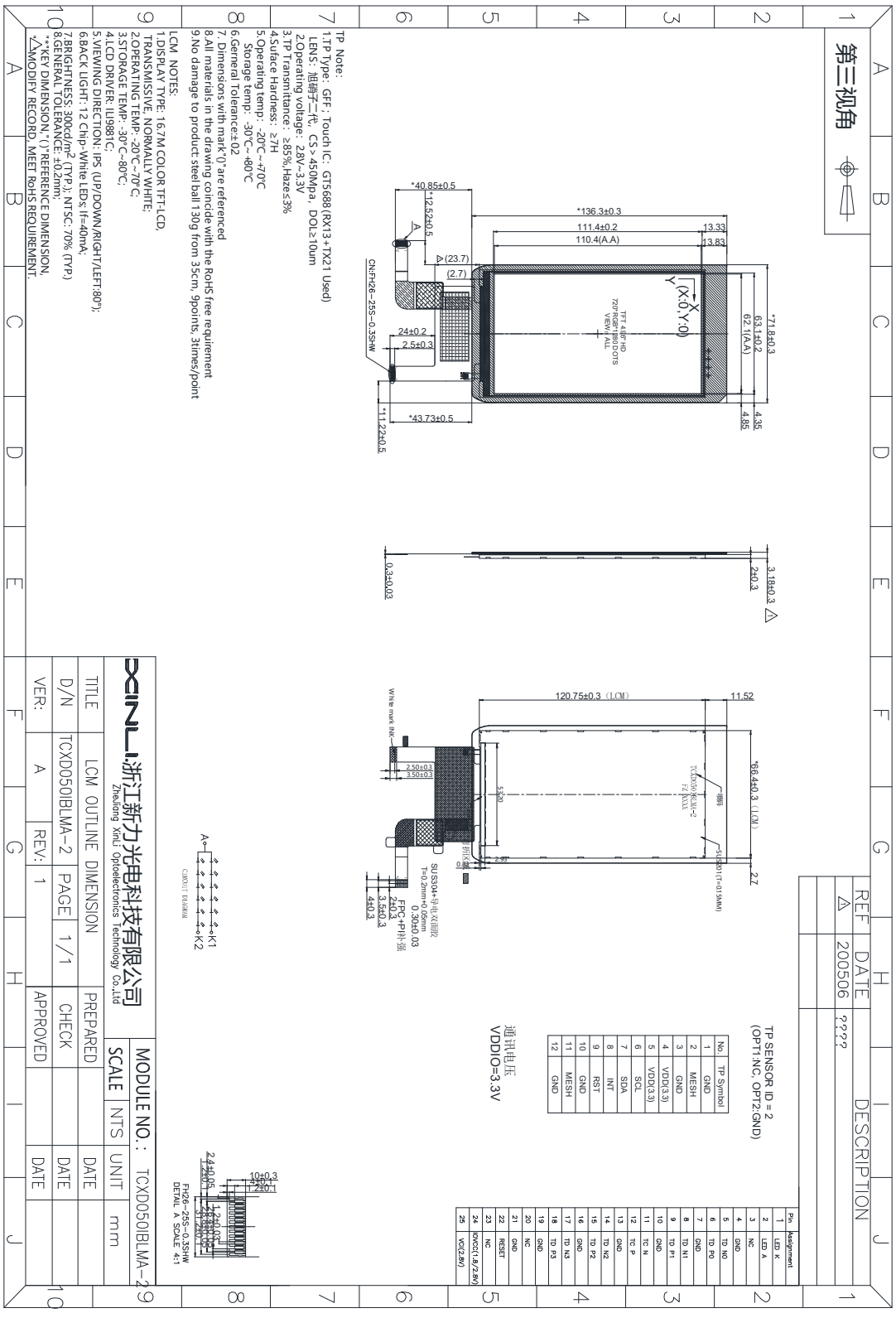
Revision	Description	Date
1.0	Initial Release	2020/4/30
1.1	Change modle thickness and interface definition	2020/5/6

2. General Description and Features

The 5.0 inch Module named TCXD050IBLMA-2 is a-Si TFT-LCD module, which is the type of transmissive. It is consisted of TFT-LCD Panel, one Driver IC ,one FPC and one Back-Light one TP unit. Features of this product are listed in the following table.

NO	Item	Contents	Unit
(1)	Module Outline	71.8(H)*136.3(V)*3.18(T)	mm
(2)	LCD Active area	62.1(H)*110.4(V)	mm
(3)	Dot Number	720*3(RGB)*1280	/
(4)	Dot size	28.75*86.25	um
(5)	LCD type	TFT Transmissive	/
(6)	Display Color	16.7M	/
(7)	Viewing direction	ALL	O'clock
(8)	Power Supply	2.8(TYP)	V
(10)	Interface	FH26-25S-0.3SHW	/
(12)	Interface type	MIPI	/
(13)	Module weight	TBD	g

3. Mechanical Dimension



4. Interface Pin Connection

4.1This model used FH26-25S-0.3SHW manufactured by HIROSE.

No.	Symbol	I/O	Function	Remark
1	LEDK	P	Backlight ground	
2	LEDA	P	Backlight anode	
3	NC	-	NC	
4	GND	P	Ground	
5	TD N0	I	MIPI-DSI data Lane 0 negative-end input/output pin	
6	TD P0	I	MIPI-DSI data Lane 0 positive-end input/output pin	
7	GND	P	Ground	
8	TD N1	I	MIPI-DSI data Lane 1 negative-end input/output pin	
9	TD P1	I	MIPI-DSI data Lane 1 positive-end input/output pin	
10	GND	P	Ground	
11	TD N	I	MIPI-DSI clock Lane negative-end input pin	
12	TD P	I	MIPI-DSI clock Lane positive-end input pin	
13	GND	P	Ground	
14	TD N2	I	MIPI-DSI data Lane 2 negative-end input/output pin	
15	TD P2	I	MIPI-DSI data Lane 2 positive-end input/output pin	
16	GND	P	Ground	
17	TD N3	I	MIPI-DSI data Lane 3 negative-end input/output pin	
18	TD P3	I	MIPI-DSI data Lane 3 positive-end input/output pin	
19	GND	P	Ground	
20	NC	-	NC	
21	GND	I	GROUND	
22	RESET	I	Reset signal	
23	NC	-	NC	

24	IOVCC(1.8V /2.8V)	P	POWER(1.8V/2.8V)	
25	VCI(2.8V)	P	POWER(2.8V)	

4.2 CTP Interface.

Firmware versions: Rev.0x03.

NO	Symbol	Level	Description
1	GND	P	Ground.
2	MESH	I	-
3	GND	P	Ground.
4	VDD(3.3)	P	POWER3.3V
5	VDD(3.3)	P	POWER3.3V
6	SCL	I	I2C:serial clock.
7	SDA	I	I2C:serial data.
8	INT	I	Indicate coor dinate ready.
9	RST	I	System reset signal input，active low.
10	GND	P	Ground.
11	MESH	I	-
12	GND	P	Ground.

5. Maximum Rating

Item	Symbol	Rating	Unit
Operating temperature	Top	-20 to 70	℃
Storage temperature	Tst	-30 to 80	℃
power supply	VDD	1.65 ~ 3.6V	V

NOTE:

If the module was used these absolute maximum ratings as above, it may be damaged permanently. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability. VDD>GND must be maintained.

6. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VCI	-	2.5	2.8	6.6	V	
Analog operating voltage	VCIREF		2.5	2.8	6.6	V	
Digital operating voltage	VDDI	-	1.65	2.8	3.6	V	
Digital operating voltage	VCC1		1.65	2.8	6.6	V	
Digital operating voltage	VCC2		1.65	2.8	6.6	V	
DSI operating voltage	VDDAM	-	1.65	1.8	3.6	V	
OTP Supply voltage	MTP_PWR	-	8.4	8.5	8.6	V	
Analog operating voltage	VSP	-	4.5		6.6	V	
Analog operating voltage	VSN	-	-6.6		-4.5	V	
Logic High level input voltage	VIH	-	0.7*VDDI		VDDI	V	Note1
Logic Low level input voltage	VIL	-	-0.3		0.3*VDDI	V	Note1
Logic High level output voltage TE , LEDPWM	VOH	IOH = -1.0mA	0.8*VDDI		VDDI	V	Note1
Logic Low level output voltage TE , LEDPWM	VOL	IOL = +1.0mA	0		0.2*VDDI	V	Note1
Gate Driver High Voltage	VGH	-	8.0	-	18	V	
Gate Driver Low Voltage	VGL	-	-18.0	-	-7.0	V	
Driver Supply Voltage	-	|VGH-VGL|	15	-	32	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-4.0	-	0	V	Note3
Source Driver							
Source Output Range	VSOUT(+)	-	0.3	-	VREG1OUT-0.1	V	Note4
	VSOUT(-)	-	VREG2OUT +0.1	-	-0.3	V	Note4
Positive Gamma Reference Voltage	VREG1OUT	-	3.5	-	VSP-0.5 (VSP<=6.1) 5.6 (VSP>6.1)	V	
Negative Gamma Reference Voltage	VREG2OUT	-	VSN+0.5 (VSN>=-6.1) -5.6 (VSN<-6.1)	-	-3.5	V	
Source Output Setting Time	Tr	Below with 99% precision	-	10	-	uS	Note3.4
Output Deviation Voltage (Source Output channel)	Vdev	Sout>=4.2V Sout<=0.8V	-	-	20	mV	Note3
		4.2V>Sout>0.8V	-	-	15	mV	
Output Offset Voltage	VOFFSET	-	-	-	35	mV	Note3
Standby mode current consumption							
Sleep In mode	I(VDDI SLP IN)	Ta = 25 °C VCI=2.8V VDDI=1.8V	-	35	-	uA	
	I(VCI SLP IN)		-	25	-	uA	

Notes:

1. Ta = -30 to 70 °C (to 85 °C no damage) , VCI = 2.5V to 6.6V, VDDI = 1.65V to 3.6V

2. Supply digital VDDI voltage equal or less than analog VCI voltage.

3. Source channel loading = 9KΩ,70pF/channel

4. The maximum value is between with Note 3 and Gamma setting value

7. Backlight Characteristics

Item	syb	Min	Typ	Max	Unit	Condition
Voltage	Vin	16.8	18	19.8	V	-
Led current	Iled	-	40	-	mA	

8. AC Electrical Characteristics

18.4.2. High Speed Mode – Clock Channel Timing

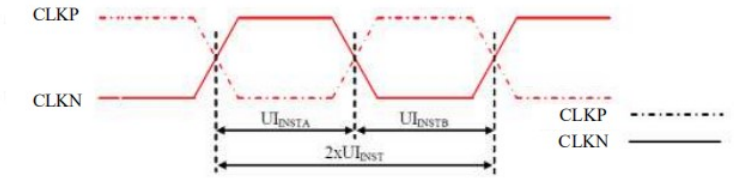


Figure 116: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

18.4.3. High Speed Mode – Data Clock Channel Timing

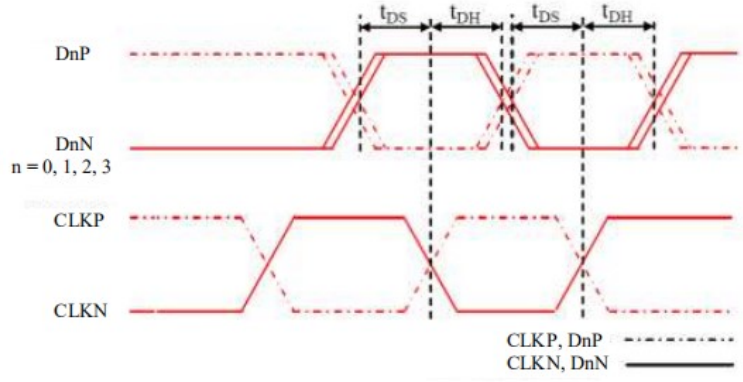


Figure 117: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

18.4.4. High Speed Mode – Rising and Falling Timings

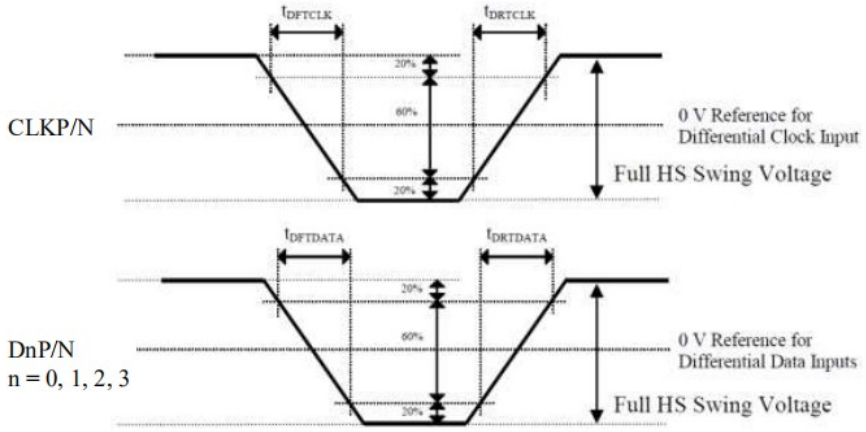


Figure 118: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

18.4.5. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

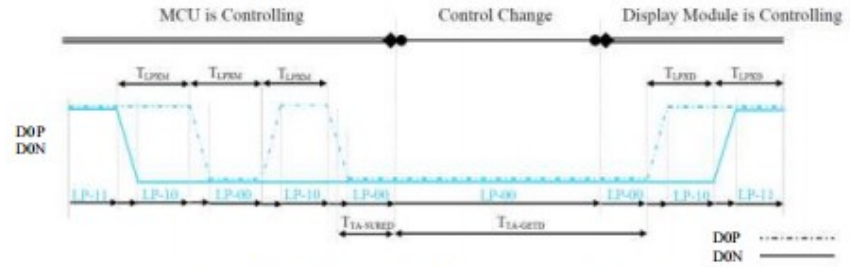


Figure 119: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

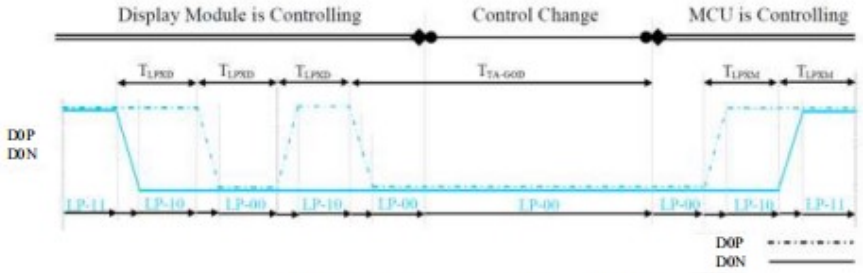


Figure 120: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

18.4.6. Data Lanes from Low Power Mode to High Speed Mode

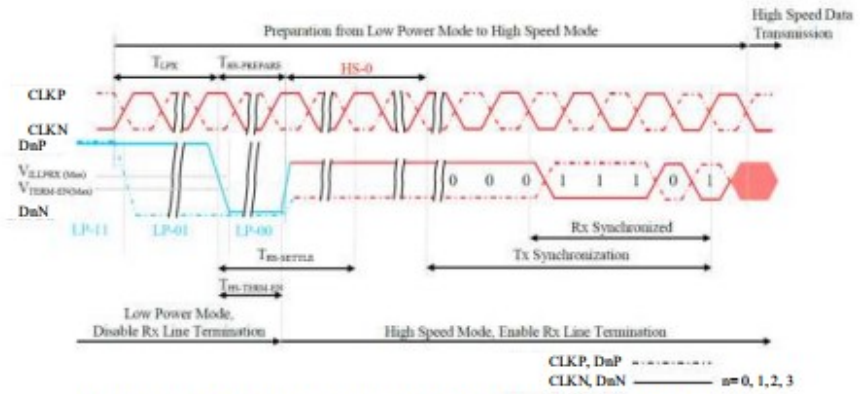
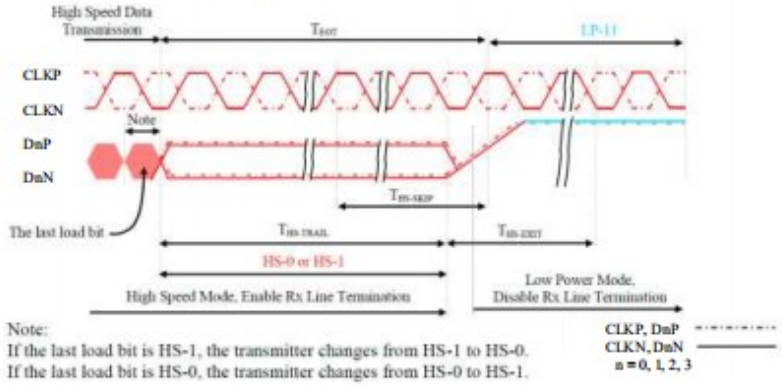


Figure 121: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

18.4.7. Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Figure 122: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

18.4.8. DSI Clock Burst – High Speed Mode to/from Low Power Mode

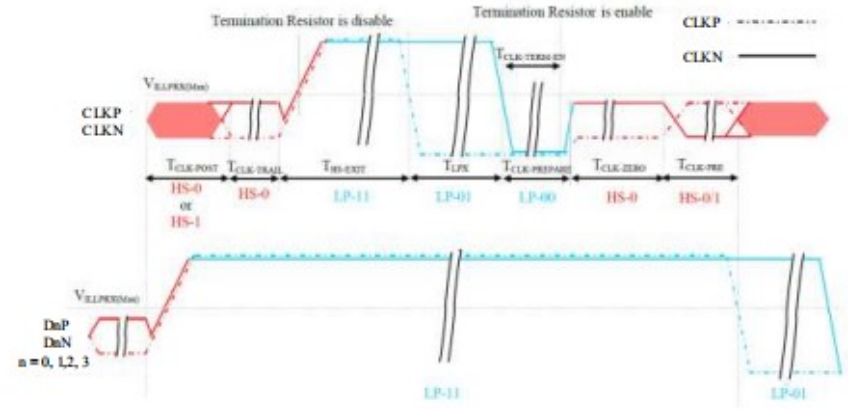
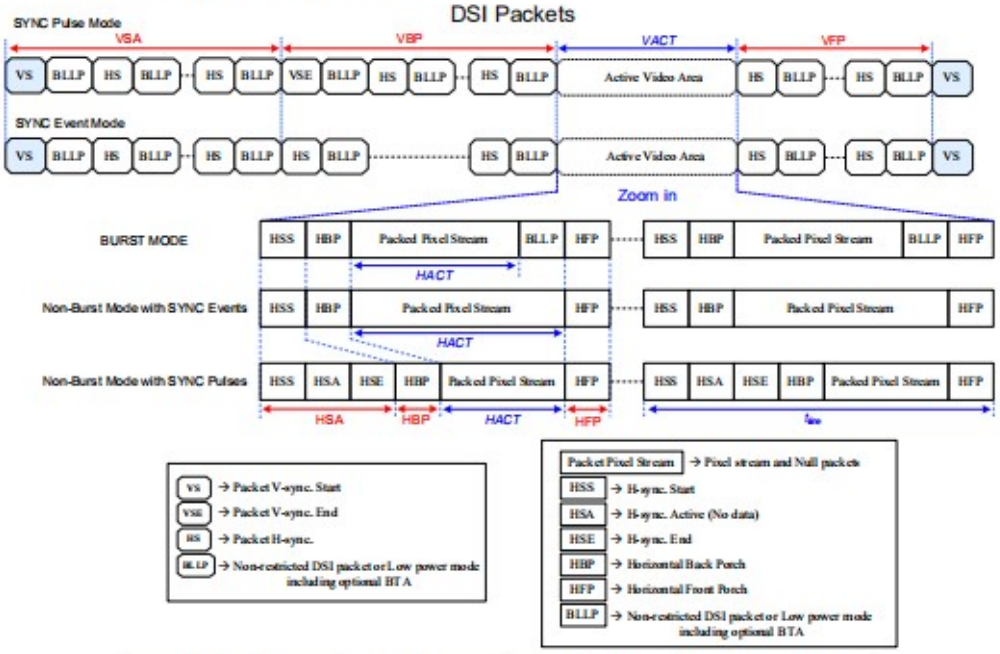


Figure 123: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

18.4.9. Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example : BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

18.4.10. Reset Timing

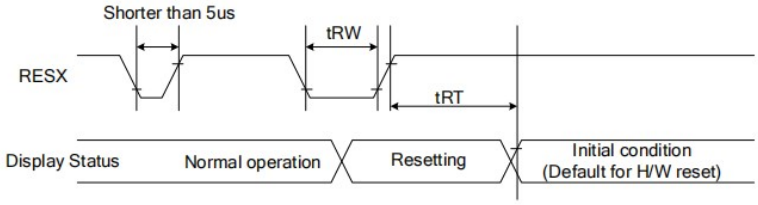


Figure 124: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

9. Electro-Optical Characteristics

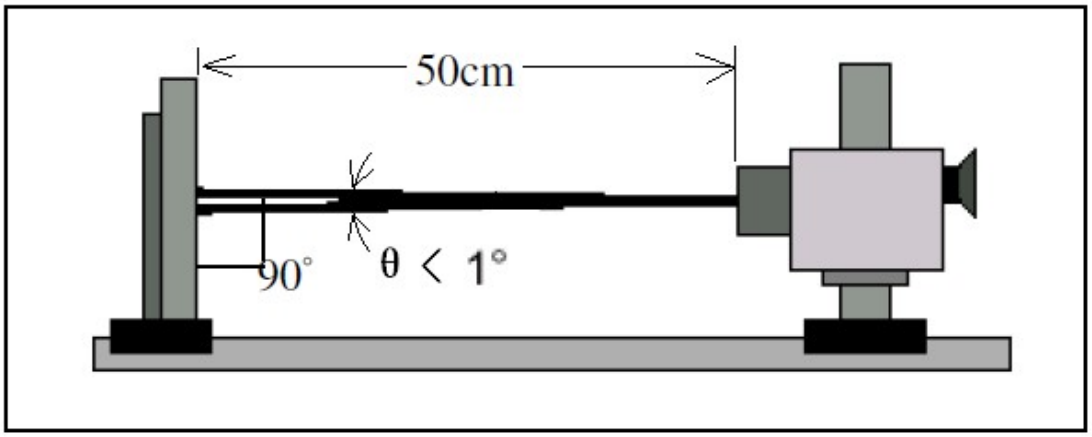
Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Response time		Tr+Tf	θ =0° ∅=0° Ta=25℃	-	25	35	ms	4
Uniformity （Five point）		δ WHITE		80	-	-	%	7
Contrast ratio		Cr		600	1000	-	-	3 ,5
Surface Luminance		Lv		-	300	-	-	3 ,7
Viewing angle range		θ	∅ = 90°	-	80	-	deg	6
			∅ = 270°	-	80	-	deg	
			∅ = 0°	-	80	-	deg	
			∅ = 180°	-	80	-	deg	
	White	X	θ = ϕ =	-	TBD	-	–	7

Color filter chromaticity (x, y)		Y	0°	-	TBD	-		
	Red	X	θ = ϕ = 0°	-	TBD	-		
		Y		-	TBD	-		
	Green	X	θ = ϕ = 0°	-	TBD	-		
		Y		-	TBD	-		
	Blue	X	θ = ϕ = 0°	-	TBD	-		
		Y		-	TBD	-		

Note 1: Ambient temperature=25℃±2℃

Note 2: To be measured in the dark room with backlight unit.

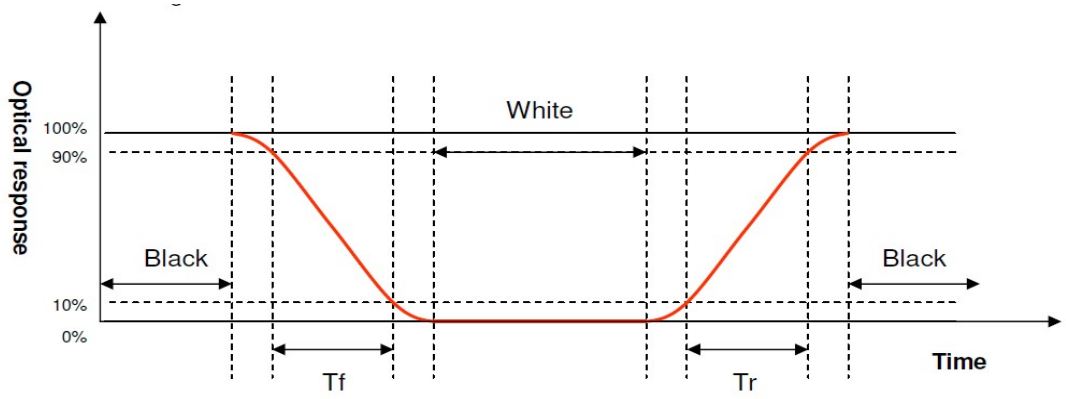
Note 3: To be measured at the center area of panel with a viewing cone of 1 by Topcon luminance meter BM-7A, after 10 minutes operation (module).



Note 4: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (rising time) and from "white" to "black" (falling time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.

Refer to figure as below.



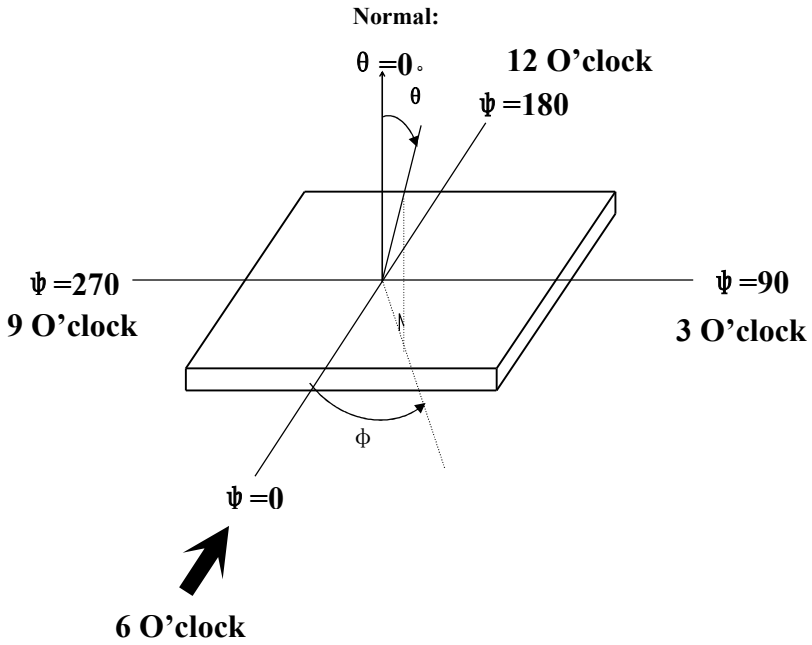
Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. Definition of viewing angle

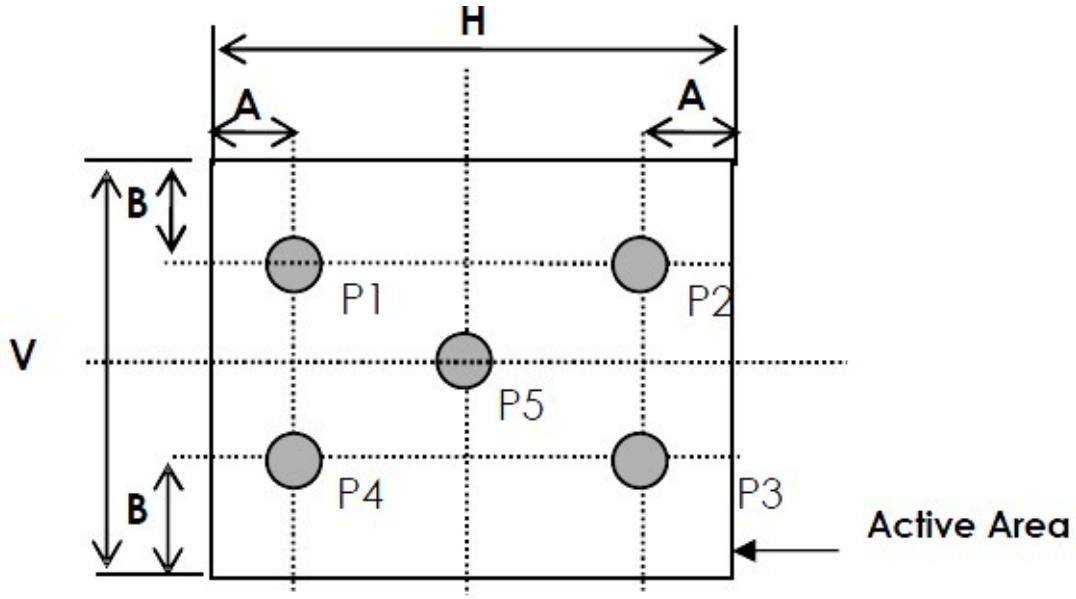
Viewing angle is the angle at which the contrast ratio is greater than 2, for TFT module the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.



Note 7. Surface luminance is the LCD surface from the surface with all pixels

displaying white. Refer to figure as below.

Measuring method for Contrast ratio, surface luminance, Luminance uniformity，CIE (x, y) chromaticity



A : 5 mm B : 5 mm H,V : Active Area

Light spot size Æ=7mm, 500mm distance from the LCD surface to detector lens

measurement instrument is TOPCON’s luminance meter BM-7A

Uniformity definition= [min of 5point/max of 5points]x100%

Lv = Average Surface Luminance with all white pixels (P_1, P_2, P_3, P4, P_5)

10．Reliability Test

This standard reliability test is done only for the first lot of MP products. Customer and supplier must hold a discussion if other reliability test is requested by customer.

No.	Test Item	Test Condition	Remarks
1	High temperature storage	80℃，240H	Note1 IEC60068-2-1:2007,GB2423.2-2008
2	Low temperature storage	-30℃，240H	IEC60068-2-1:2007 GB2423.1-2008

3	Hight temperature operation	70℃，240H	IEC60068-2-1:2007 GB2423.2-2008
4	Low temperature operation	-20℃，240H	IEC60068-2-1:2007 GB2423.1-2008
5	Hight temperature /humidity storage	60℃，90%RH 240H	Note2 IEC60068-2-78 :2001 GB/T2423.3—2006
6	Temperature Cycle (Non-operation)	-30℃-25℃-80℃ 30min-5min-30min 50 cycles	Start with cold temperature, End with high temperature, IEC60068-2-14:1984,GB2423.22-2002
7	Drop Test (package)	Height:1 m, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32:1990 GB/T2423.8—1995
8	Vibration test (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (3 hours for total)(Package condition)	IEC60068-2-6:1982 GB/T2423.10—1995
9	Electro Static Discharge (Operation)	C=150pF, R=330Ω， 5points/panel Air:± 15KV, 5 times; Contact:±8KV, 5 times; （Environment: 15℃～35℃, 30%～60%, 86Kpa～106Kpa）	IEC61000-4-2:2001 GB/T17626.2-2006

Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

11. Precautions for Operation and Storage

1. Precautions for Operation

(1)Since LCD panel made of glass,in order to prevent from glass broken or color tone change,please do not apply any mechanical shock or impact or excessive force to it when installing the LCD module.

(2)If LCD panel is broken and liquid crystal substance leaks out and contact your

skin or clothes,please immediately wash it off by using soap and water.

(3)The polarizer on the LCD surface is soft and easily scratched.Please be careful when handling.

(4)If LCD surface becomes contaminated,please wipe it off gently by using moisten soft cloth with normal hexane,do not use acetone,ketone,ethanol, alcohol or water.If there is saliva or water on the LCD surface,please wipe it off immediately.

(5)When handing LCD module,please be sure that the body and the tools are properly grounded.And do not touch I/F pins with bare hands or contaminate I/F pins.

(6)Do not attempt to disassemble or process the LCD module.

(7)LCD module should be used under recommended operating conditions shown in chapter 6 and 7.

(8)Response time will be extremely slower at lower temperature than at specified temperature and LCD will show different color when at higher temperature.The phenomenon will disappear when returning to specified condition.

(9)Foggy dew,moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage,the deteriorated display quality and electrochemical reaction then leads to the shorter life time and permanent damage to the module probably.Please pay attention to the environmental temperature and humidity.

2. Precautions for Storage

(1)Please store LCD module in a dark place,avoid exposure to sunlight,the light of fluorescent lamp or any ultraviolet ray.

(2)Keep the environment temperature at between 10℃and 35 ℃ and at normal humidity.Avoid high temperature,high humidity or temperature below 0℃.

(3)That keeps the LCD modules stored in the container shipped from supplier before using them is recommended.

(4)Do not leave any article on the LCD module surface for an extended period of time.

3. Warranty period

Warrants for a period of 12 Months from the shipping data when stored or used under normal condition.

12. Package Specification

TBD