SPECIFICATION

PRODUCT NO. : **TCXD070IBLMA-1184**
VERSION : **Ver 1.0**
ISSUED DATE : **2022-10-25**

This module uses ROHS material

FOR CUSTOMER：

□：APPROVAL FOR SPECIFICATION
■：APPROVAL FOR SAMPLE

DATE	APPROVED BY

Xinli Optoelectronics ：

Presented by	Reviewed by	Organized by

Note:

1.Xinli Optronics reserves the right to make changes without further notice to any products herein to improve reliability, function or design.

1. Record of Revision

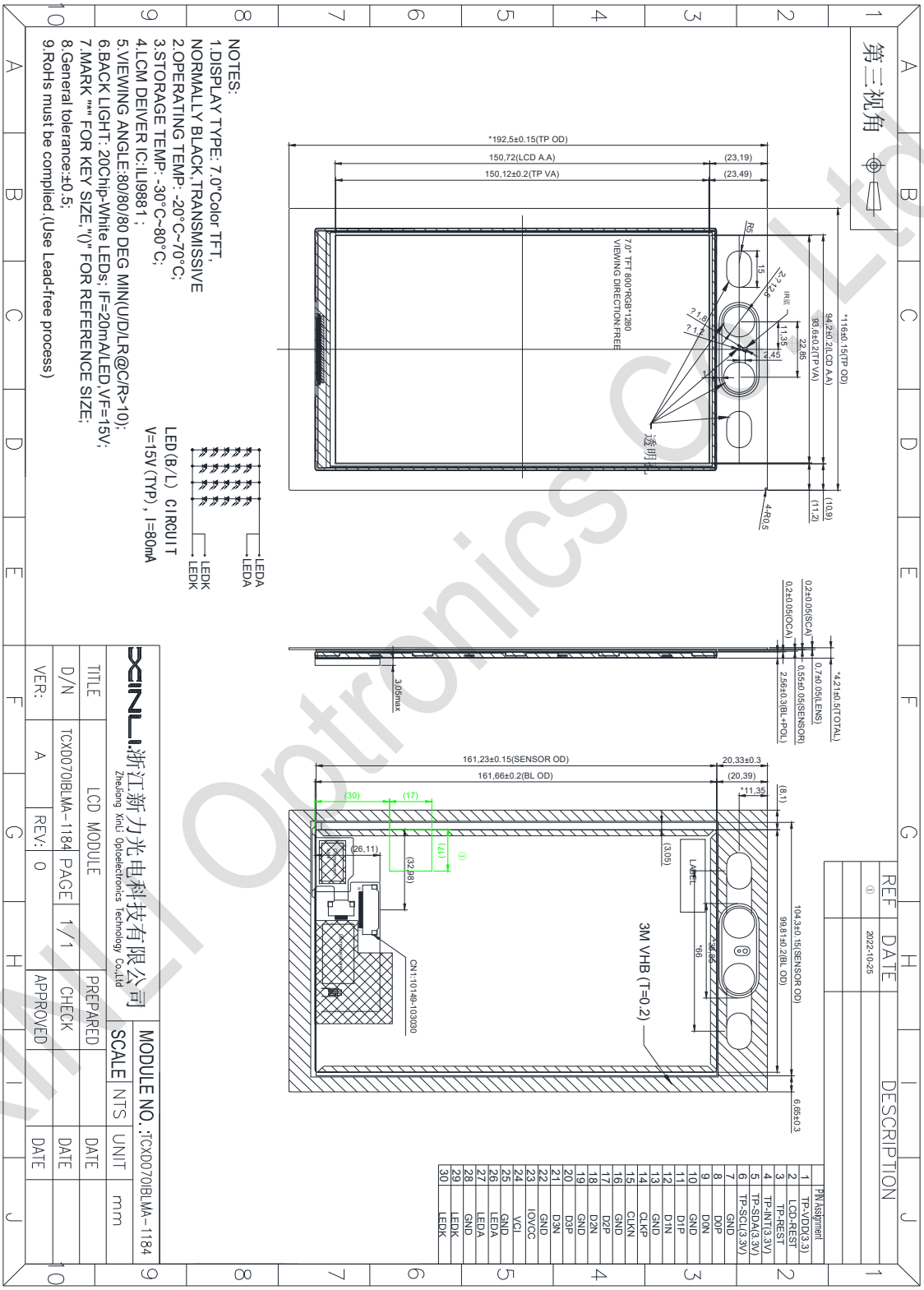
Revision	Description	Date
1.0	Initial Release	2022/10/25

2. General Description and Features

The 7.0 inch Module named TCXD070IBLMA-1184 is a-Si TFT-LCD module, which is the type of transmissive. It is consisted of TFT-LCD Panel, one Driver IC, FPC, one Back-Light . Features of this product are listed in the following table.

NO	Item	Contents	Unit
(1)	Module Outline	116.00(H)*192.5*4.21(V)	mm
(2)	LCD Active area	94.2(H)*150.72(V)	mm
(3)	Dot Number	800 RGB*1280	/
(4)	Dot size	0.0945*0.0945	mm
(5)	LCD type	TFT Transmissive	/
(6)	Display Color	16.7M	/
(7)	Viewing direction	Free	/
(8)	Backlight Type	20Chip-White LEDs	/
(9)	Power Supply	3.3(TYP)	V
(10)	Drive IC	ILI9881C-04	/
(11)	Interface	FPC 0. 5mm_Pitch 30pin	/
(12)	Interface type	MIPI interface	/
(13)	Sensor ID	1	/

3.Mechanical Dimension



4.Interface Pin Connection

Connectors required: 30S_ST-0.5-H2.0 掀盖式

No.	Symbol	I/O	Function
1	TP-VDD	-	TP Power Supply
2	LCD-RES	I	Reset pin
3	TP-RES	-	TP System reset signal input, active low
4	TP-INT	-	TP Indicate coor dinate ready
5	TP-SDA	-	TP I2C:serial data
6	TP-CL	-	TP I2C:serial clock
7	GND	P	Ground
8	DOP	I/O	Positive MIPI differential data input
9	DON	I/O	Negative MIPI differential data input
10	GND	P	Ground
11	D1P	I	Positive MIPI differential data input
12	D1N	I	Negative MIPI differential data input
13	GND	P	Ground
14	CLKP	I	Positive MIPI differential clock input
15	CLKN	I	Negative MIPI differential clock input
16	GND	P	Ground
17	D2P	I	Positive MIPI differential data input
18	D2N	I	Negative MIPI differential data input
19	GND	P	Ground
20	D3P	I	Positive MIPI differential data input
21	D3N	I	Negative MIPI differential data input
22	GND	P	Ground
23	IOVCC	P	Power Supply(3.3V)
24	VCI	P	Power Supply(3.3V)
25	GND	P	Ground
26	LEDA	P	Backlight+
27	LEDA	P	Backlight+
28	GND	P	Ground
29	LEDK	P	Backlight-
30	LEDK	P	Backlight-

5. Maximum Rating

Item	Symbol	Rating	Unit
Operating temperature	Top	-30 to 80	℃
Storage temperature	Tst	-20 to 70	℃
Power supply for analog circuit	VDD	-0.3~ 7.0	V

6. Electrical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply		VCI	-	2.5	3.3	6.6	V
Logic input signal Voltage	H level	V_{IH1}	-	0.7*VCI	-	VCI	V
	L level	V_{IL1}		-0.3	-	0.3*VCI	V

7. Backlight Characteristics

Item	syb	Min	Typ	Max	Unit	Condition
Voltage（LED A）	Vf	13.5	15	16.5	V	IF=80mA(20mA/LED)
Luminance(module)	Lv	-	300	-	cd/m2	
Number of LED	-	20			pcs	-
LED life-span	-	(20000)	-	-	Hrs	-

8.Timing Characteristics

8.1 AC Characteristics

8.1.1 high speed mode – clock timing

CLKP/N lanes can be driven to the High Speed Clock Mode (HSCM) when CLK lanes start to function between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM). This sequence is illustrated below.

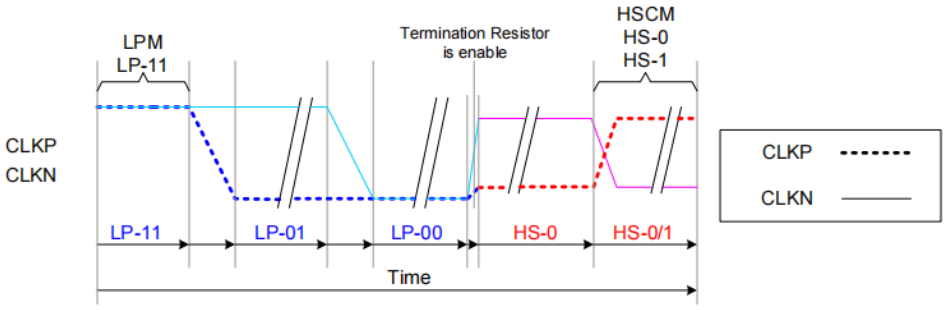


Figure 9: From LPM to HSCM

The mode change is also illustrated below.

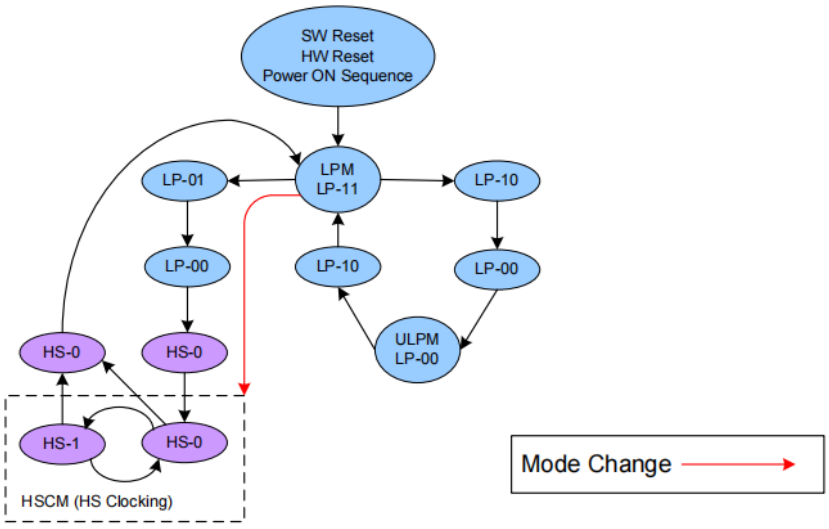


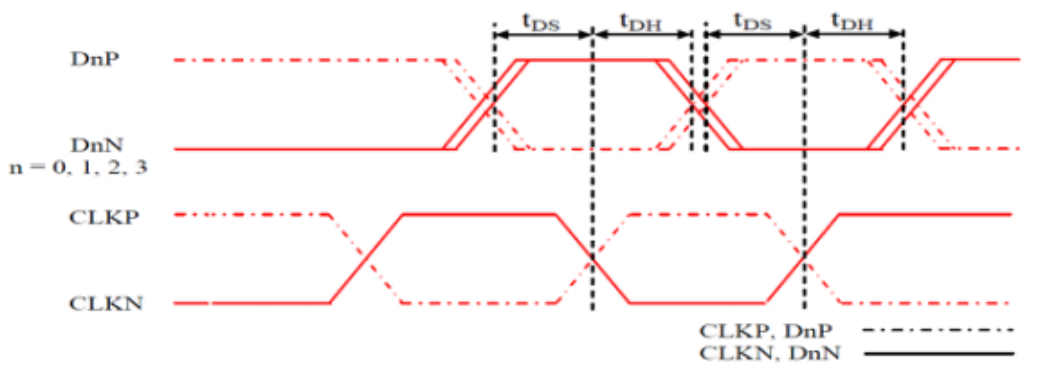
Figure 10: Mode Change from LPM to HSCM

The high speed clock (CLKP/N) starts before high speed data is sent via data lanes. The high speed clock continues clocking after the high speed data sending is stopped.

The burst of the high speed clock consists of:

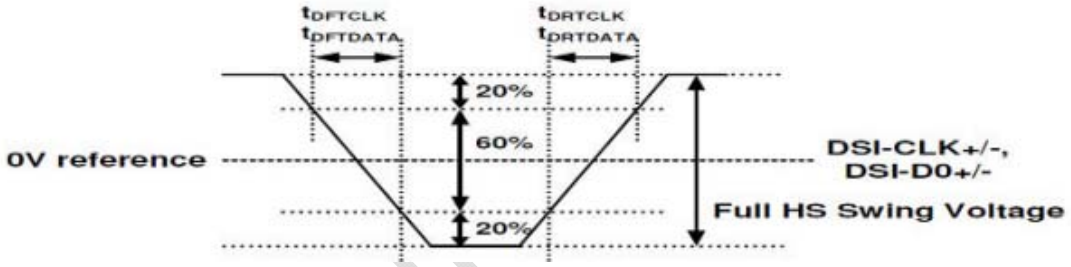
- Even number of transitions
- Start state is HS-0
- End state is HS-0

8.1.2 high speed mode – clock/data timing



Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
Dn P/N (n=0,1,2 and 3)	tDS	Data to Clock Setup time	0.15*UI			UI	
	tDH	Clock to Data Hold time	0.15*UI			UI	

8.1.3 high speed mode – rising and falling timing



Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Differential Rise Time for Clock	tDRTCLK	CLKP/N	150pS		0.3*UI		2,3
Differential Rise Time for Data	tDRTDATA	DnP/N	150pS		0.3*UI		1,2,3
Differential Fall Time for Clock	tDFTCLK	CLKP/N	150pS		0.3*UI		2,3
Differential Fall Time for Data	tDFTDATA	DnP/N	150pS		0.3*UI		1,23

Note 1: Dn =0,1,2 and 3

Note2: The display module has to meet timing requriements,which are defined for the transmitter (MCU) on MIPI D-PHY standard.

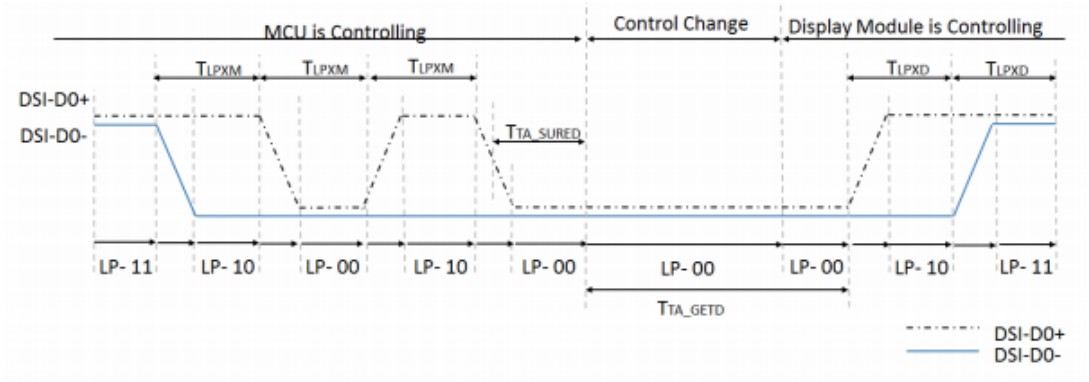
Note3: DSI-CLK+ = CLKP

DSI-CLK- =CLKN

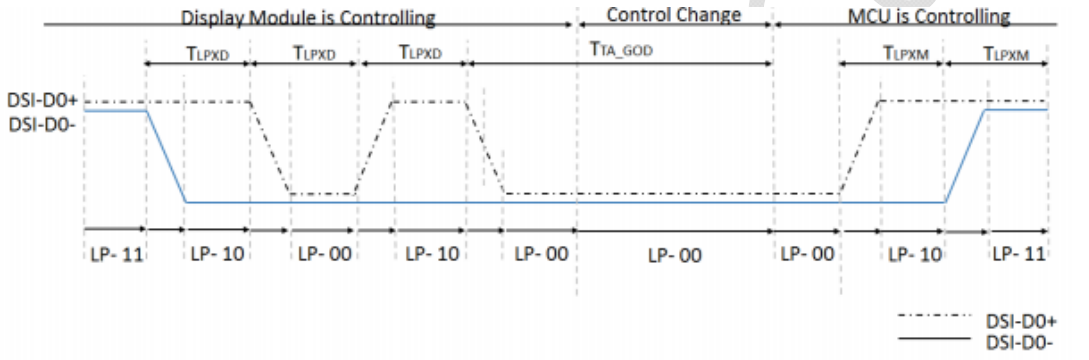
DSI-D0+ =D0P

DSI-D0- =D0N

8.1.4 Low Speed Mode - Bus Turn Around



Bus Turnaround (BTA) from MCU to display module Timing

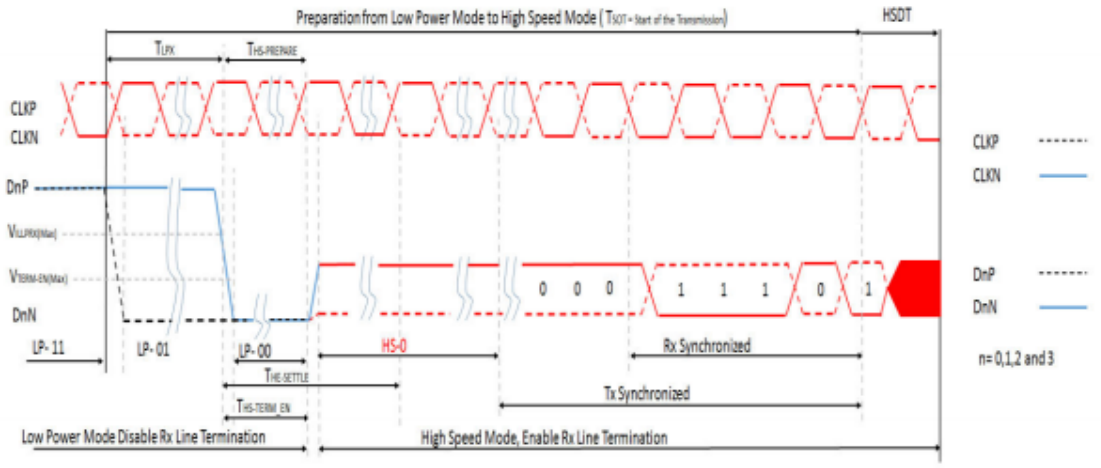


Bus Turnaround (BTA) from Display module to MCU Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	T_{LPXM}	Length of LP-00,LP-01,LP-10 or LP11 periods MCU to Display Module	50		75	nS	1
D0P/N	T_{LPXD}	Length of LP-00,LP-01,LP-10 or LP11 periods Display Module to MCU	50		75	nS	1
D0P/N	T_{TA_SURED}	Time-out before the Display Module starts driving	T_{LPXD}		2* T_{LPXD}	nS	1
D0P/N	T_{TA_GETD}	Time to drive LP-00 by Display Module	5* T_{LPXD}			nS	1
D0P/N	T_{TA_GOD}	Time to drive LP-00 after turnaround request -MCU	4 * T_{LPXD}			nS	1

Note 1: D0P = DSI-D0+, D0N = DSI-D0-

8.1.5 Data Lanes from Low Power Mode to High Speed Mode

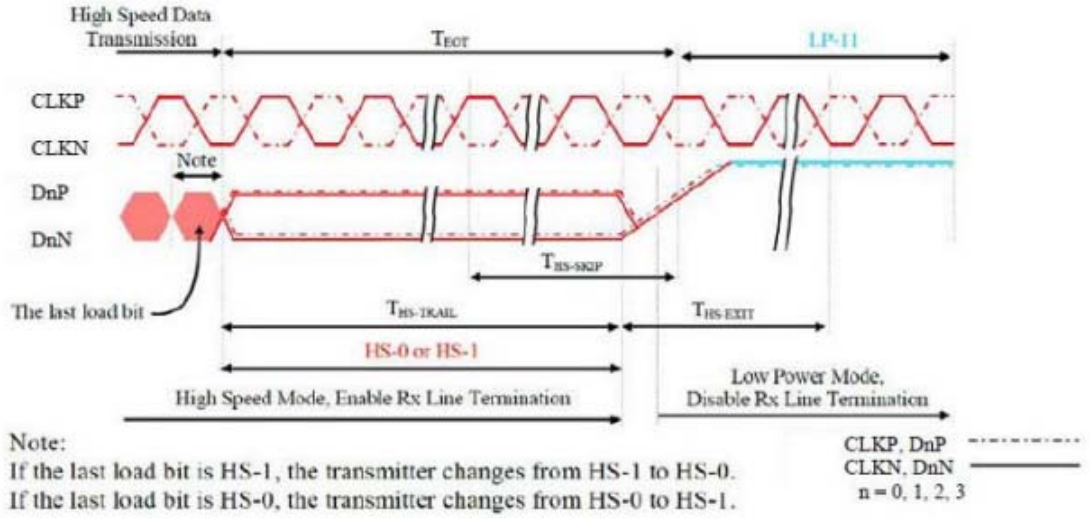


Data Lanes from Low Power Mode to High Speed Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	TLPX	Length of any Low Power State Period	50			nS	1
D0P/N	THS-PREPARE	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
D0P/N	THS-TREM-EN	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

Note 1: Dn =0,1,2 and 3

8.1.6 Data Lanes from High Speed Mode to Low Power Mode

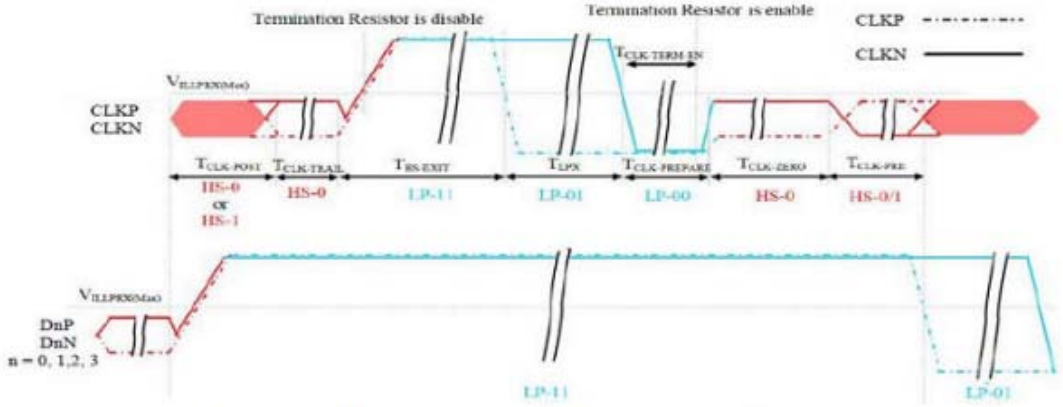


Data Lanes from High Speed Mode to Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	$T_{HS-SKIP}$	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
D0P/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			nS	1

Note 1: Dn =0,1,2 and 3

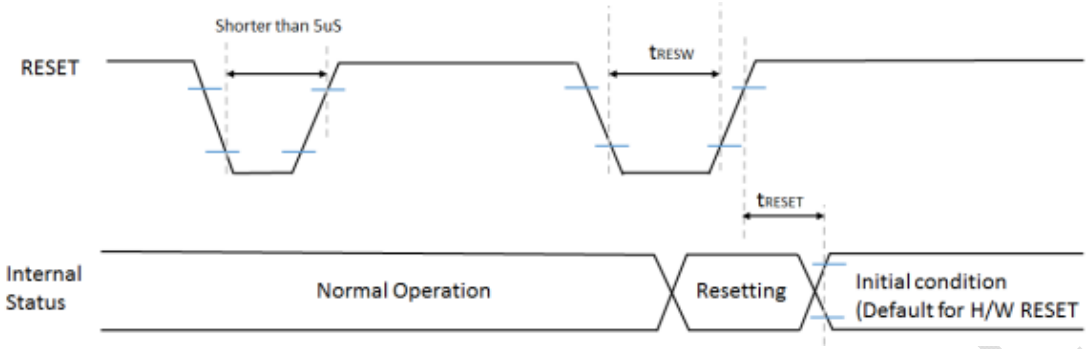
8.1.7 DSI Clock Burst – High speed mode to /from Low Power Mode



Clock Lane –High speed mode to / from Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CKP/N	$T_{CK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52*UI			nS	
CKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			nS	
CKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination			38	nS	
CKP/N	$T_{CLK-PREPARE}+T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300			nS	
CKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8*UI			nS	

8.2 Reset timing



Condition : Ta =25℃

Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	tRESW	Reset "L" pulse width		10			uS	1
	tRESET	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	5

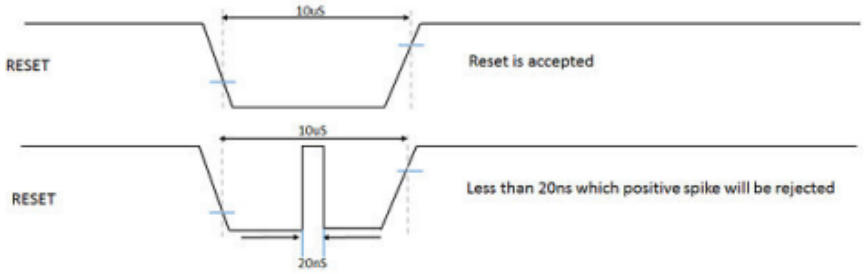
Note 1: Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.

RESET Pulse	Action
Short than 5us	Reset Rejected
Long than 10uS	Reset
Between 5us and 10uS	Reset Start

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

Note3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time(tRESET) within 5ms after a rising edge of RESET.

Note4: Spike Rejection also applies during a valid reset pulse as shown below:



Note5: It is necessary to wait 5msec after releasing RESET before sending commands. Also Sleep Out command can not be sent for 120msec.

9. Initial Code

Please consult our technical department for detail information.

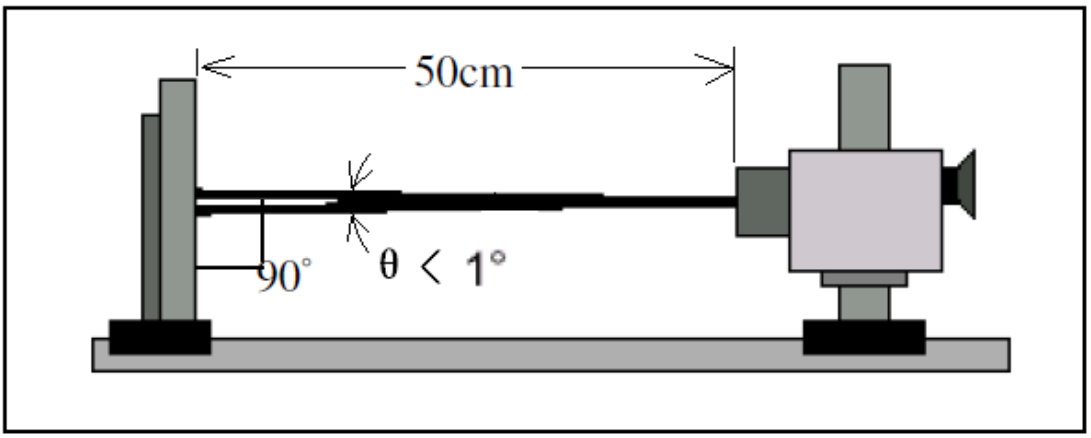
10. Electro-Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Response time	Tr+Tf	θ =0° ∅=0° Ta=25℃	-	30	40	ms	4
Uniformity （Five point）	δ WHITE		-	80	-	%	7
Contrast ratio	Cr		600	800	-	-	3 ,5
Surface Luminance (Without CTP)	Lv		-	300	-	-	3 ,7
Viewing angle range	θ	∅ = 90°	70	80	-	deg	6
		∅ = 270°	70	80	-	deg	
		∅ = 0°	70	80	-	deg	
		∅ = 180°	70	80	-	deg	
Color chromaticity (CF only, light source is C light, CIE 1931)	R_X	θ = ϕ = 0°	TBD.	TBD.	TBD.		7
	R_Y		TBD.	TBD.	TBD.		
	G_X		TBD.	TBD.	TBD.		
	G_Y		TBD.	TBD.	TBD.		
	B_X		TBD.	TBD.	TBD.		
	B_Y		TBD.	TBD.	TBD.		
	Wx		TBD.	TBD.	TBD.		
	Wy		TBD.	TBD.	TBD.		

Note 1: Ambient temperature=25℃±2℃

Note 2: To be measured in the dark room with backlight unit.

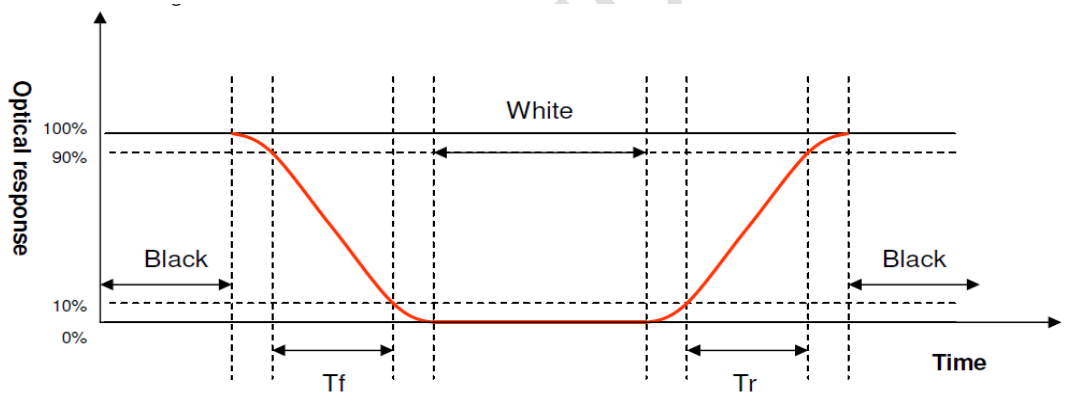
Note 3: To be measured at the center area of panel with a viewing cone of 1 by Topcon luminance meter BM-7A, after 10 minutes operation (module).



Note 4: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (rising time) and from "white" to "black" (falling time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.

Refer to figure as below.



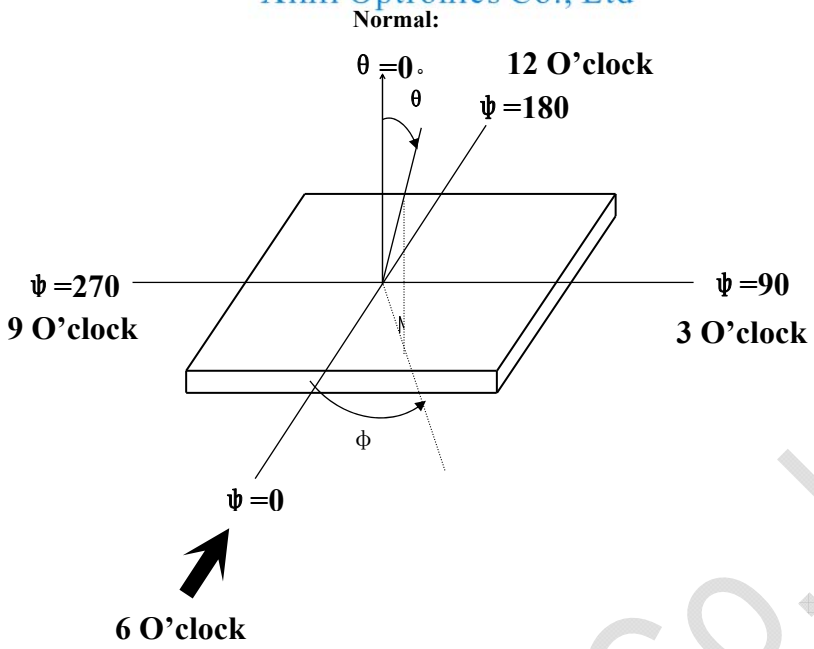
Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

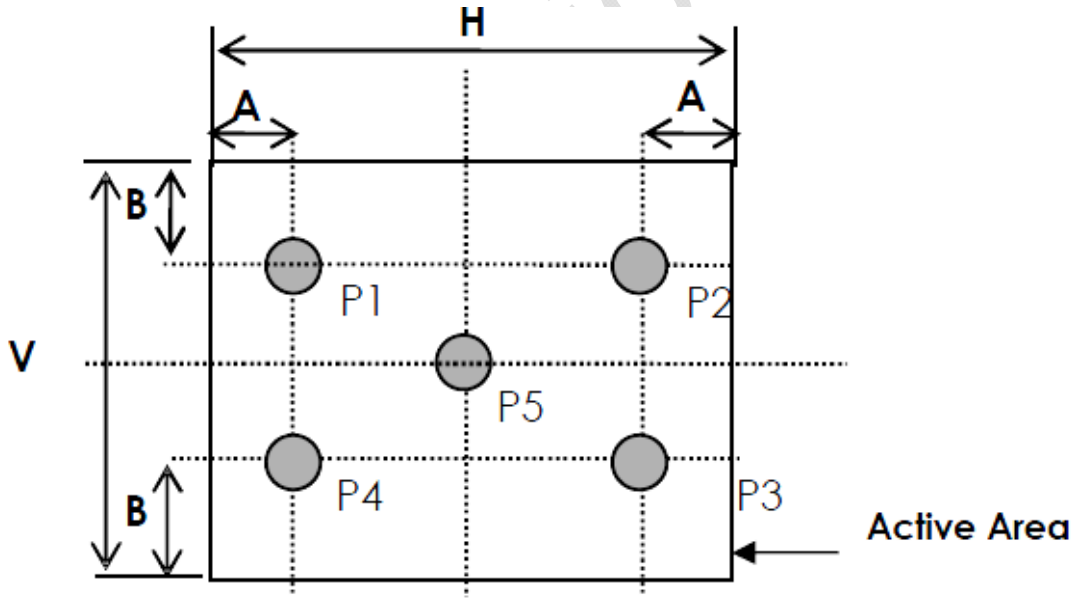
Note 6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10 for TFT module. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.



Note 7. Surface luminance is the LCD surface from the surface with all pixels displaying white. Refer to figure as below.

Measuring method for Contrast ratio, surface luminance, Luminance uniformity，CIE (x, y) chromaticity



A : 5 mm B : 5 mm H,V : Active Area

Light spot size Æ=7mm, 500mm distance from the LCD surface to detector lens

measurement instrument is TOPCON's luminance meter BM-7A

Uniformity definition= [min of 5point/max of 5points]x100%

Lv = Surface Luminance with all white pixels (P5)

11. Quality Assurance

TBD.

12. Reliability Test

This standard reliability test is done only for the first lot of MP products.
Customer and supplier must hold a discussion if other reliability test is requested by customer.

NO.	Test Item	Description	Test Condition
1	High temperature storage	Endurance test applying the high storage temperature for a long time	80℃,240H
2	Low temperature storage	Endurance test applying the low storage temperature for a long time	-30℃,240H
3	High temperature operation	Endurance test applying the electric stress under high temperature for a long time	70℃,240H
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time	-20℃,240H
5	High temperature /humidity storage	Endurance test applying the high temperature and high humidity storage for a long time	60℃,90% RH, 240H

13. Precautions for Operation and Storage

1. Precautions for Operation

(1)Since LCD panel made of glass,in order to prevent from glass broken or color tone change,please do not apply any mechanical shock or impact or excessive force to it when installing the LCD module.

(2)If LCD panel is broken and liquid crystal substance leaks out and contact your skin or clothes,please immediately wash it off by using soap and water.

(3)The polarizer on the LCD surface is soft and easily scratched.Please be careful when handling.

(4)If LCD surface becomes contaminated,please wipe it off gently by using moisten soft cloth with normal hexane,do not use acetone,ketone,ethanol, alcohol or water.If there is saliva or water on the LCD surface,please wipe it off immediately.

(5)When handing LCD module,please be sure that the body and the tools are properly grounded.And do not touch I/F pins with bare hands or contaminate I/F pins.

(6)Do not attempt to disassemble or process the LCD module.

(7)LCD module should be used under recommended operating conditions shown in chapter 6 and 7.

(8)Response time will be extremely slower at lower temperature than at specified temperature and LCD will show different color when at higher temperature.The phenomenon will disappear when returning to specified condition.

(9)Foggy dew,moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage,the deteriorated display quality and electrochemical reaction then leads to the shorter life time and permanent damage to the module probably.Please pay attention to the environmental temperature and humidity.

2.Precautions for Storage

(1)Please store LCD module in a dark place,avoid exposure to sunlight,the light of fluorescent lamp or any ultraviolet ray.

(2)Keep the environment temperature at between 10℃and 35 ℃ and at normal humidity.Avoid high temperature,high humidity or temperature below 0℃.

(3)That keeps the LCD modules stored in the container shipped from supplier before using them is recommended.

(4)Do not leave any article on the LCD module surface for an extended period of time.

3.Warranty period

Warrants for a period of 12 Months from the shipping date when stored or used under normal condition.

14.Package Specification

TBD.