SPECIFICATION

PRODUCT NO. :**TCXD070IBLON-140**
VERSION : **Ver 1.0**
ISSUED DATE : **2023-02-03**

This module uses ROHS material

FOR CUSTOMER: _____
□: APPROVAL FOR SPECIFICATION
■: APPROVAL FOR SAMPLE

DATE	APPROVED BY

Xinli Optronics :

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1.Record of Revision

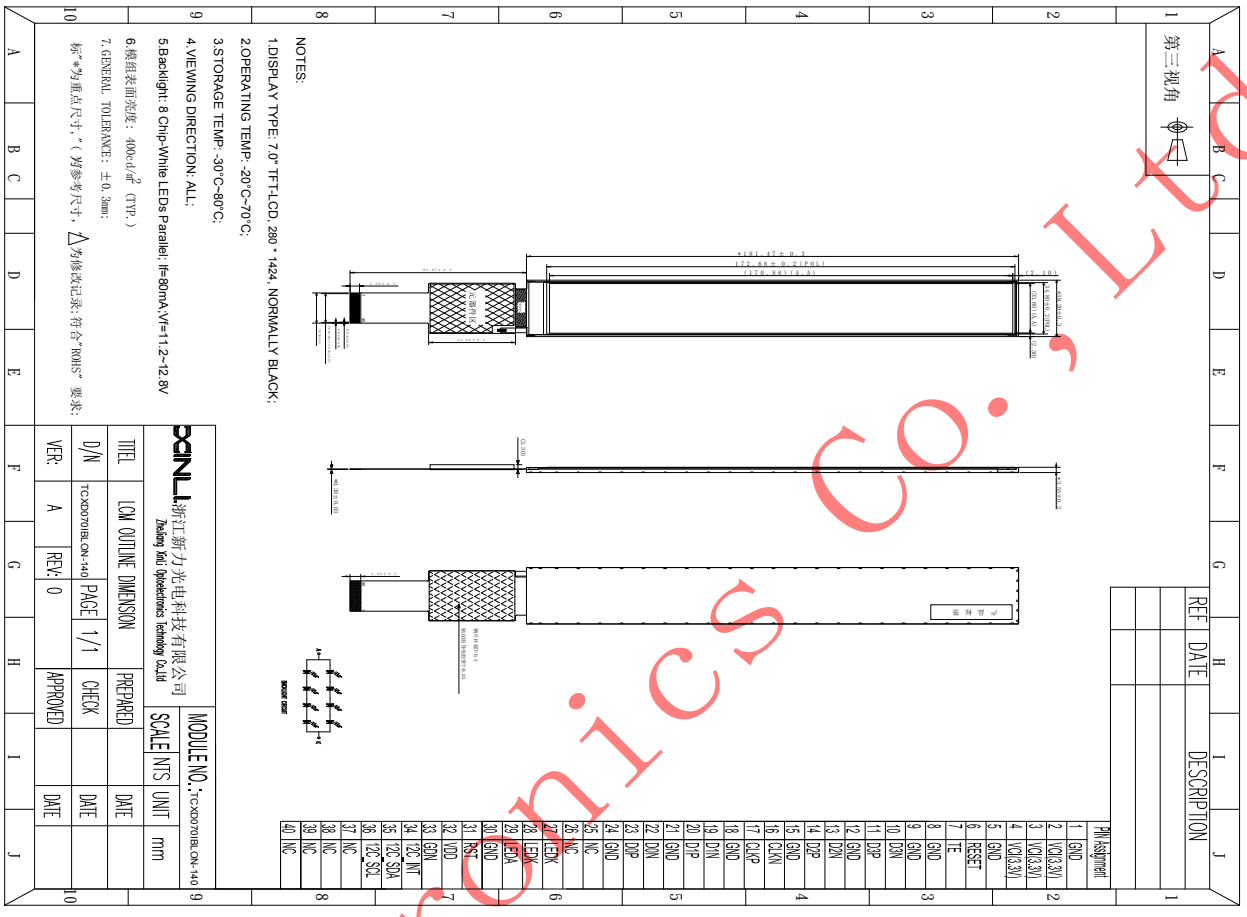
Revision	Description	Date
1.0	Initial Release	2023-02-03

2.General Description and Features

The 7.0 inch Module named TCXD070IBLON-140 is a-Si TFT-LCD module,It is consisted of TFT-LCD Panel, Driver IC, one FPC and one Back-Light unit. Features of this product are listed in the following table.

NO	Item	Contents	Unit
(1)	Module Outline	38.2 x 181.47 x 3.55	mm
(2)	LCD Active area	33.6 x 170.88	mm
(3)	Dot Number	280 x 3(RGB) x 1424	/
(4)	Dot size	0.12(RGB)(H)x 0.12(V)	mm
(5)	LCD type	TFT Transmissive, Normal Black	/
(6)	Display Color	16.7M	/
(7)	Viewing direction	ALL	O'clock
(8)	Backlight Type	8-chip LED	/
(9)	Power Supply	3.3 (TYP)	V
(10)	Interface	40 pin	/
(11)	Interface type	MIPI interface	/
(12)	Module weight	Typ	g

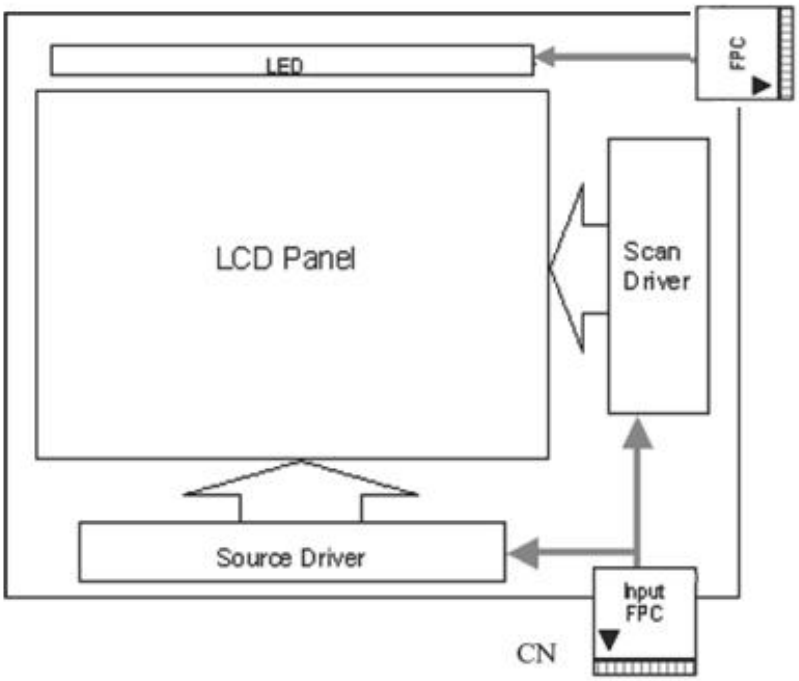
3.Mechanical Dimension



4.Interface Pin Connection

NO	Symbol	Level	Description
1	GND	P	Ground.
2	VCI(3.3)	P	Power Supply.
3	VCI(3.3)	P	Power Supply.
4	VCI(3.3)	P	Power Supply.
5	GND	P	Ground.
6	RESET	I	Global Reset pin.
7	TE	O	Sync signal for touch panel.
8	GND	P	Ground.
9	GND	P	Ground.
10	D3N	I	MIPI data input pins.
11	D3P	I	MIPI data input pins.
12	GND	P	Ground.
13	D2N	I	MIPI data input pins.
14	D2P	I	MIPI data input pins.
15	GND	P	Ground.
16	CLKN	I	MIPI clock input pins.
17	CLKP	I	MIPI clock input pins.
18	GND	P	Ground
19	D1N	I	MIPI data input pins.
20	D1P	I	MIPI data input pins.
21	GND	P	Ground.
22	D0P	I	MIPI data input pins.
23	D0N	I	MIPI data input pins.
24	GND	P	Ground.
25	NC	-	No connection.
26	NC	-	No connection.
27	LEDK	P	LED cathode power supply.
28	LEDK	P	LED cathode power supply.
29	LEDA	P	LED Anode power supply.
30	GND	P	Ground.
31	RST	I	No connection.
32	VDD	P	No connection.
33	GND	P	No connection.
34	I2C_INT	I	No connection.
35	I2C_SDA	I	No connection.
36	I2C_SCL	I	No connection.
37	NC	-	No connection.
38	NC	-	No connection.
39	NC	-	No connection.
40	NC	-	No connection.

5.Block Diagram



6. Maximum Rating

Item	Symbol	Rating	Unit
Operating temperature	Top	-20 to 70	℃
Storage temperature	Tst	-30 to 80	℃
Power Supply Voltage	VCI	-0.3~3.6	V

NOTE:

1.If the module was used these absolute maximum ratings as above, it may be damaged permanently. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability. VCI>GND must be maintained.

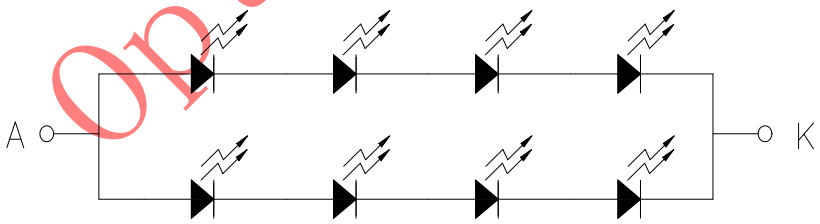
7. Electrical Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Power supply		VCI	2.7	3.3	3.6	V	-
Logic input signal Voltage	H level	V_{IH}	0.7*VCI	-	VCI	V	-
	L level	V_{IL}	0	-	0.3*VCI	V	-

8. Backlight Characteristics

Backlight Driving Conditions

Item	syb	Min	Typ	Max	Unit	Condition
Number of LED	-		8		pcs	-
LED life-span	-	10000	20000	-	Hrs	-
VLED	Vf	11.2	12	12.8	V	IF=80mA



BACKLIGHT CIRCUIT

9. Timing Characteristics

9.1 DC Characteristics

9.1.1 System characteristics

(VCC=1.5V, VDD=3.3V,AVDD=12V, VSS=VSSA=0V, TA=-20 to +85℃)

Parameter	Symbol	MIN.	Typ.	MAX.	UNIT	Conditions
VDD Input low voltage level	Vil1	0	-	0.3*VDD	V	For the VDD domain inputs.
VDD Input high voltage level	Vih1	0.7*VDD	-	VDD	V	For the VDD domain inputs.
VCC Input low voltage level	Vil2	0	-	0.2*VCC	V	For the VCC domain inputs.
VCC Input high voltage level	Vih2	0.8*VCC	-	VCC	V	For the VCC domain inputs.
I2C Low level input voltage	Vil3	1.65		VDD	V	For SDA/SCL inputs
I2C High level input voltage	Vih3	0		0.2	V	For SDA/SCL inputs
Input leakage current	Ii	-	-	+/- 1	μA	For the digital, I/O circuit (Not include the pull-up/down current)
Output high voltage level	Voh	0.8*VDD	-	-	V	For VDD domain outputs, Ioh = 400uA
Output low voltage level	Vol	-	-	0.2*VDD	V	For VDD domain outputs, Iol = 400uA
Differential input leakage Current	I_{DIFFI}	-10		+10	uA	For DxP, DxN, CLKP, CLKN (With steady state inputs)
Pull low/high resistor	Ri	100K	250K	500K	ohm	For the digital Input pin VDD=3.3, VCC=1.5
Output Voltage deviation	VOD1		±20	±35	mV	Vo = AGND+0.2V ~ AGND+1.5V Vo = HAVDD-0.2V ~ HAVDD-1.5V Vo = HAVDD+0.2V ~ HAVDD+1.5V Vo = AGND+0.2V ~ AGND+1.5V
Output Voltage deviation	VOD2		±15	±20	mV	Vo = AGND+1.5V ~ HAVDD-1.5V Vo = HAVDD+1.5V ~ AVDD-1.5V
Output Voltage Offset between Chips	VOC			±20		Vo = AGND+1.5V ~ HAVDD-1.5V Vo = HAVDD+1.5V ~ AVDD-1.5V
Input level of V1 ~ V7	Vref1	HAVDD+0.2	-	AVDD-0.2	V	Gamma positive voltage input
Input level of V8 ~ V14	Vref2	0.2	-	HAVDD-0.2	V	Gamma negative voltage input
Dynamic Range of Output	Vdr	0.2	-	AVDD-0.2	V	S0 ~ S1802
Sinking Current of Outputs	IOLy	80	-	-	μA	S0 ~ S1802
Driving Current of Outputs	IOHy	80	-	-	μA	S0 ~ S1802
Digital Operation current	Idd	-	TBD	-	mA	
Digital Stand-by current	Ist1	-	TBD	-	μA	
Analog Operation current	Idda	-	TBD	-	mA	
Analog Stand-by current	Ist2	-	TBD	-	μA	

VDD=VCI.

9.1.2 MIPI DC Characteristics

HS Receiver DC Specification

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Operation Voltage	VDD	1.5-10%	1.5	1.5+10%	mV	
Differential Input Voltage	|VID|	70	200	260	mV	
Common Mode Voltage	$V_{CMRX(DC)}$	70	-	330	mV	
Differential Input High Threshold Voltage	VTH	-	-	70	mV	
Differential Input Low Threshold Voltage	VTL	-70	-	-	mV	
Singled-ended input high voltage	V_{IHHS}	-	-	460	mV	
Singled-ended input low voltage	V_{ILHS}	-40	-	-	mV	
Singled-ended threshold for HS termination enable	$V_{TERM-EN}$	-	-	450	mV	
Differential input impedance	Z_{ID}	80	100	125	ohm	
Pin leakage current	I_{LEAK}	-10	-	10	uA	
Common-mode interference beyond 450MHz	$\Delta V_{CMRX(HF)}$	-	-	100	mV	
Common-mode interference 50MHz - 450MHz	$\Delta V_{CMRX(LF)}$	-50	-	50	mV	
Common-mode termination	C_{CM}	-	-	60	pF	
Embedded Termination	R_T	90	100	110	ohm	2bits RT_SEL[1: 0] for termination resistor selection 00 → 200ohm 10 , 01→ 150ohm 11 → 100ohm (default) 1bit ERMR_EN for termination resistor enable TERMR_EN=0, termr disable R=(OPEN) TERMR_EN=1, termr enable

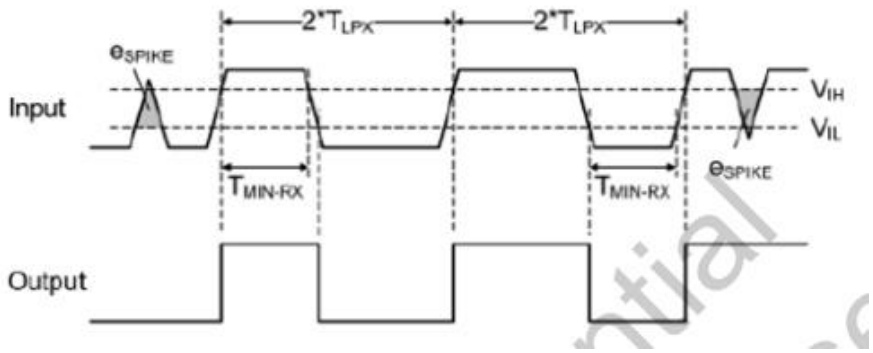
Note:

(1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.

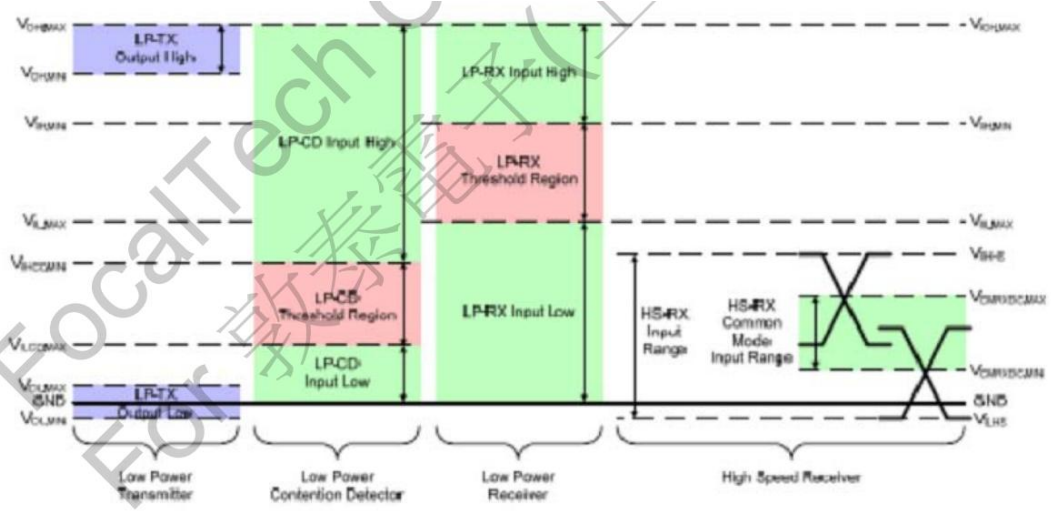
LP Receiver DC Specification

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Logic 1 input voltage	V_{IH}	880	-	-	mV	
Logic 0 input voltage, not in ULP State	V_{IL}	-	-	550	mV	
Input hysteresis	V_{HYST}	25	-	-	mV	



Line Contention Detection

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV	
Logic 0 contention threshold	VILCD	-	-	200	mV	



Input Characteristics

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Pin signal voltage range	V_{PIN}	-50		1350	mV	
Pin leakage current	I_{LEAK}	-10		10	uA	
Ground shift	V_{GNDSH}	-50		50	mV	
Transient pin voltage level	$V_{PIN(absmax)}$	-0.15		1.45	V	
Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$	$TV_{PIN(absmax)}$			20	ns	

Note:

(1) When the pad voltage is in the signal voltage range from VGNDSH, MIN to VOH + VGNDSH, MAX and the Lane Module is in LP receive mode.

(2) The voltage overshoot and undershoot beyond the VPIN is only allowed during a single 20ns window after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the VPIN range.

(3) This value includes ground shift.

9.2 AC Characteristics

9.2.1 System AC Characteristics

(VDD=3.3V, AVDD=12V, VSS=VSSA=0V, TA=-20 to +85℃)

Parameter	Symbol	MIN.	Typ.	MAX.	UNIT	Conditions
VDD Power On Slew rate	T	-	-	20	ms	From VSS to 90% VDD
RSTB pulse width	T	10	-	-	us	

9.2.2 MIPI AC Characteristics

HS Receiver AC Timing Characteristics

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Bandwidth per lane	-	-	-	1000	Mbps	Bandwidth selected by register 'speedup' Speedup=0 → Max=550Mbps Speedup=1→ Max=1000Mbps
Operation frequency	-	-	-	500	MHz	
UI instantaneous	UI_{INST}	1	-	12.5	ns	1
Data to Clock Skew	Tskew	-0.15	-	0.15	UI_{INST}	
Inter-lane static skew	Tskew-lane	-	-	$UI_{INST}/50$	UI_{INST}	
Data to Clock Setup Time	T_{SETUP}	0.25	-	-	UI_{INST}	2
Data to Clock Hold Time	T_{HOLD}	0.25	-	-	UI_{INST}	
Common-mode interference beyond 450MHz	$\Delta V_{CMRX(HF)}$	-	-	100	mV	4
Common-mode interference 50MHz- 450MHz	$\Delta V_{CMRX(LF)}$	-50	-	50	mV	3,6
Common-mode termination	C_{CM}	-	-	60	pF	5

Note:

(1) Total silicon and package delay budget of 0.3*UINST

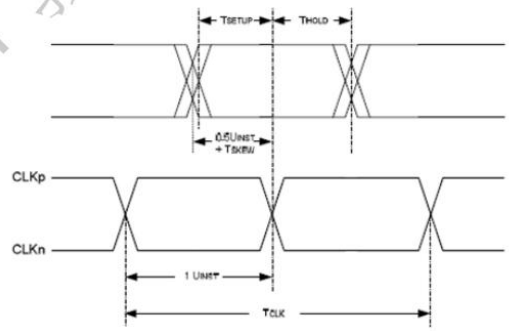
(2) Total setup and hold window for receiver of 0.3*UINST

(3) Excluding 'static' ground shift of 50mV

(4) =VCMRX (HF) is the peak amplitude of a sine wave superimposed on the receiver input

(5) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

(6) Voltage difference compared to the DC average common-mode potential.



LP Receiver AC Timing Characteristics

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Input pulse rejection	e_{SPIKE}	-	-	300	V·ps	1,2,3
Minimum pulse width response	T_{MIN-RX}	20	-	-	ns	
Peak interference amplitude	V_{INT}	-	-	200	mV	
Interference frequency	f_{INT}	450	-	-	MHz	
Logic 1 input voltage	V_{IH}	880	-	-	mV	
Logic 0 input voltage, not in ULP State	V_{IL}	-	-	550	mV	
Logic 0 input voltage, ULP State	$V_{IL-ULPS}$	-	-	300	mV	
Input Hysteresis	V_{HYST}	25	-	-	mV	
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV	
Logic 0 contention threshold	V_{ILCD}	-	-	200	mV	

Note:

(1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1state.

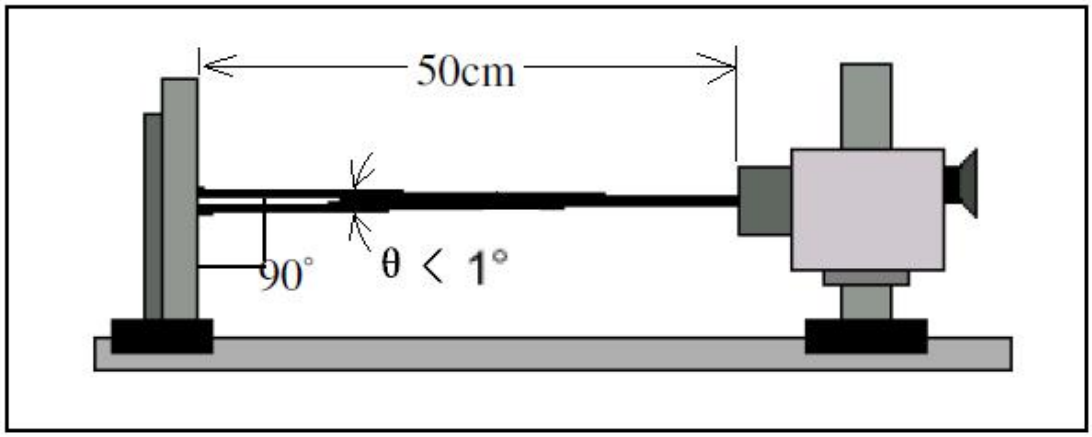
(2) An impulse less than this will not change the receiver state.

(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

10. Electro-Optical Characteristics

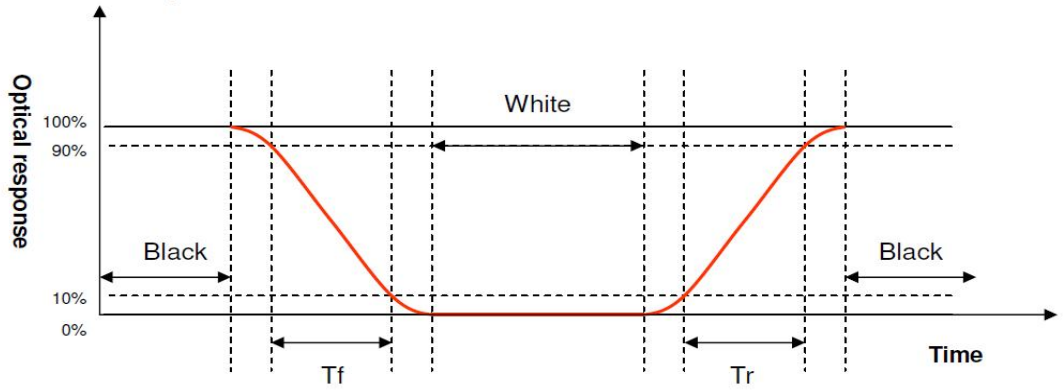
Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Response time		Tr+Tf	25℃	-	30	**40**	ms	**4**
Contrast ratio		Cr	θ =0° ∅=0° Ta=25℃	800	1000	-	-	**3 ,5**
Surface Luminance		Lv		-	400	-	-	**3 ,7**
Viewing angle range		θ	∅ = 90°	75	80	-	deg	**6**
			∅ = 270°	75	80	-	deg	
			∅ = 0°	75	80	-	deg	
			∅ = 180°	75	80	-	deg	
Color filter chromaticity (x, y)	White	X	θ = ϕ = 0°	-0.02	-	+0.02	deg	**7**
		Y			-			
	Red	X			-		deg	
		Y			-			
	Green	X			-		deg	
		Y			-			
	Blue	X			-		deg	
		Y			-			

Note 1: Ambient temperature=25℃±2℃
Note 2: To be measured in the dark room with backlight unit.
Note 3: To be measured at the center area of panel with a viewing cone of 1 by Topcon luminance meter BM-7A, after 10 minutes operation (module).



Note 4: Definition of response time:
The output signals of photo detector are measured when the input signals are changed from "black" to "white" (rising time) and from "white" to "black" (falling time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.

Refer to figure as below.



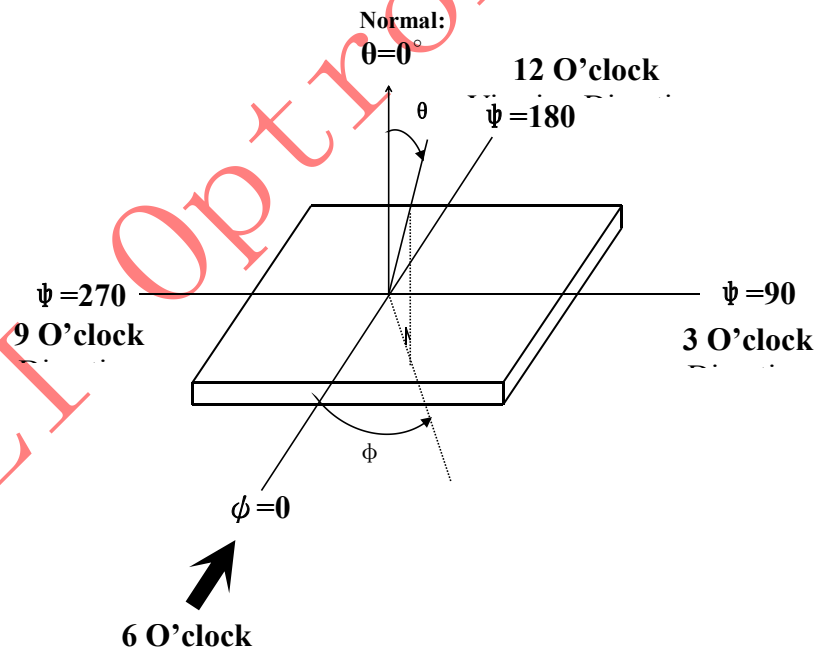
Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

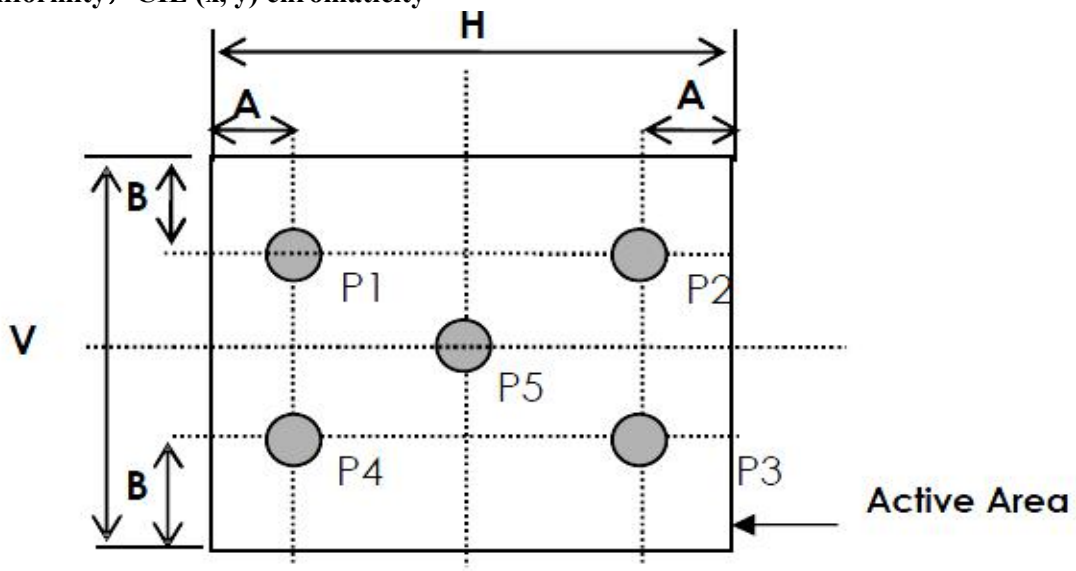
Note 6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 2, for TFT module the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.



Note 7. Surface luminance is the LCD surface from the surface with all pixels displaying white. Refer to figure as below.

Measuring method for Contrast ratio, surface luminance, Luminance uniformity，CIE (x, y) chromaticity



A : 5 mm B : 5 mm H,V : Active Area
Light spot size Æ=7mm, 500mm distance from the LCD surface to detector lens measurement instrument is TOPCON's luminance meter BM-7A

Uniformity definition= [min of 5point/max of 5points]x100%
Lv = Average Surface Luminance with all white pixels (P_5)

11. Reliability Test

This standard reliability test is done only for the first lot of MP products. Customer and supplier must hold a discussion if other reliability test is requested by customer.

No.	Test Item	Description	Test Condition
1	High temperature storage	Endurance test applying the high storage temperature for a long time	80℃,500 H
2	Low temperature storage	Endurance test applying the low storage temperature for a long time	-30℃,500H
3	High temperature operation	Endurance test applying the electric stress under high temperature for a long time	70℃,500H
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time	-20℃,500H
5	High temperature /humidity storage	Endurance test applying the high temperature and high humidity storage for a long time	60℃,90% RH, 500H
6	Temperature Cycle (Non operation)	Endurance test applying the low and high temperature cycle -20℃←→25℃←→70℃ 30min←→5min←→30min one cycle	-20℃/70℃, 500 cycles

12. Precautions for Operation and Storage

1. Precautions for Operation

(1) Since LCD panel made of glass,in order to prevent from glass broken or color tone change,please do not apply any mechanical shock or impact or excessive force to it when installing the LCD module.
(2) If LCD panel is broken and liquid crystal substance leaks out and contact your skin or clothes,please immediately wash it off by using soap and water.
(3) The polarizer on the LCD surface is soft and easily scratched.Please be careful when handling.
(4) If LCD surface becomes contaminated,please wipe it off gently by using moisten soft cloth with normal hexane,do not use acetone,ketone,ethanol, alcohol or water.If there is saliva or water on the LCD surface,please wipe it off immediately.
(5) When handing LCD module,please be sure that the body and the tools are properly grounded.And do not touch I/F pins with bare hands or contaminate I/F pins.
(6) Do not attempt to disassemble or process the LCD module.
(7) LCD module should be used under recommended operating conditions shown in chapter 6 and 7.
(8) Response time will be extremely slower at lower temperature than at specified temperature and LCD will show different color when at higher temperature.The phenomenon will disappear when returning to specified condition.
(9) Foggy dew,moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage, the deteriorated display quality and electrochemical reaction then leads to the shorter life time and permanent damage to the module probably.Please pay attention to the environmental temperature and humidity.

2. Precautions for Storage

(1) Please store LCD module in a dark place,avoid exposure to sunlight,the light of fluorescent lamp or any ultraviolet ray.
(2) Keep the environment temperature at between 10℃and 35 ℃and at normal humidity.Avoid high temperature,high humidity or temperature below 0℃.
(3) That keeps the LCD modules stored in the container shipped from supplier before using them is recommended.
(4) Do not leave any article on the LCD module surface for an extended period of time.

3. Warranty period

Warrants for a period of 12 Months from the shipping date when stored or used under normal condition.

13. Package Specification

TBD