SPECIFICATION

RODUCT NO. : TCXD078IBLMA-211B
VERSION : Ver 1.0
ISSUED DATE : 2023-3-20

This modue is RoHS compliant

FOR CUSTOMER : _____

☐: APPROVAL FOR SPECIFICATION
■ : APPROVAL FOR SAMPLE

DATE	APPROVED BY

Xinli Optoelectronics :

Presented by	Reviewed by	Organized by

Note:

1. Xinli Optronics reserves the right to make changes without further notice to any products herein to improve reliability, function or design.
2. All rights are reserved. No one is permitted to reproduce or duplicate the whole or part of this document without Xinli Optronics' permission.

1. Record of Revision

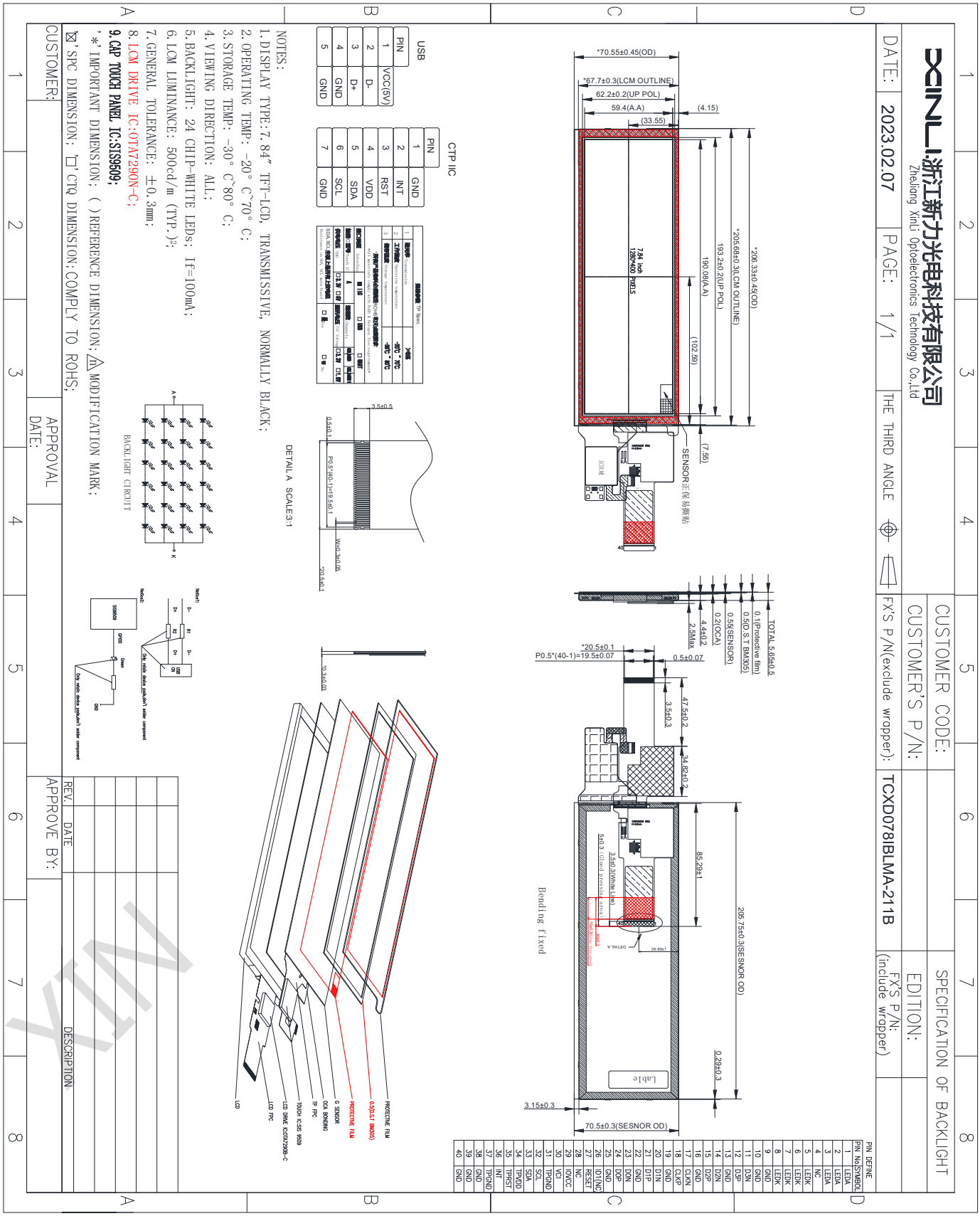
Revision	Description	Date
1.0	Initial Release	2023/3/20

2. General Description and Features

The 7.8 inch Module named TCXD078IBLMT-211 is a-Si TFT-LCD module, which is the type of transmissive. It is consisted of TFT-LCD Panel, Driver IC, FPC, Back-Light a Touch Panel unit and plastic shell. Features of this product are listed in the following table.

NO	Item	Contents	Unit
(1)	Module Outline	206.33(H)*70. 55(V)*5.65(T)	mm
(2)	LCD Active area	59.40(H)*190.08(V)	mm
(3)	Dot Number	400*3(RGB)*1280	/
(4)	Dot size	0.0495(H) ×0.1485 (V)	mm
(5)	LCD type	TFT Transmissive	/
(6)	Display Mode	Normally Black(IPS)	/
(7)	Display Color	16.7M	/
(8)	Viewing direction	ALL	O'clock
(9)	Backlight Type	24 Chip	/
(10)	Power Supply	3.3(TYP)	V
(11)	Interface	FPC 0. 5mm_Pitch 40pin	/
(12)	Interface type	MIPI interface	/
(13)	With /Without TSP	Only G-Sensor	/
(14)	Driver IC	TFT:OTA7290N-C CTP:SIS9509	/

3. Mechanical Dimension



4. Interface Pin Connection

FPC Connector is used for the module electronics interface. The recommended model is FPC0.5G-WTX-40P.

No.	Symbol	I/O	Function
1	LEDA	P	Led anode
2	LEDA	P	Led anode
3	LEDA	P	Led anode
4	NC	-	No connection
5	LEDK	P	LED Cathode
6	LEDK	P	LED Cathode
7	LEDK	P	LED Cathode
8	LEDK	P	LED Cathode
9	GND	P	Ground
10	GND	P	Ground
11	D3N	I	MIPI data Input
12	D3P	I	MIPI data Input
13	GND	P	Ground
14	D2N	I	MIPI data Input
15	D2P	I	MIPI data Input
16	GND	P	Ground
17	CLKN	I	MIPI data Input
18	CLKP	I	MIPI data Input
19	GND	P	Ground
20	D1N	I	MIPI data Input
21	D1P	I	MIPI data Input
22	GND	P	Ground
23	D0N	I/O	MIPI data Input
24	D0P	I/O	MIPI data Input
25	GND	P	Ground
26	ID1(NC)	-	No connection
27	RESET	I	Global reset pin , active Low. High voltage level : VCI
28	NC	-	No connection

29	IOVCC	P	I/O voltage. Not used within display and can be left unconnected
30	VCI	P	A power supply for DC/DC circuit.
31	TPGND	P	TP Ground
32	SCL	I/O	TP I2C:serial clock
33	SDA	I/O	TP I2C:serial data
34	TPVDD	P	TP Power Supply
35	TPRST	I	TP System reset signal input, active low
36	INT	O	TP Indicate coor dinate ready
37	TPGND	P	TP Ground
38	GND	P	Ground
39	GND	P	Ground
40	GND	P	Ground

5. Maximum Rating

Item	Symbol	Rating	Unit
Operating temperature	Top	-20 to 70	℃
Storage temperature	Tst	-30 to 80	℃
Power input	VCI	-0.5~ 4	V
Operating Humidity	HOP	10 to 80	%RH
Storage Humidity	HST	10 to 90	%RH

6. Electrical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply		VCI	-	2.7	3.3	3.6	V
VCI input voltage level	H level	V_{IH1}	-	0.7*VCI	-	VCI	V
	L level	V_{IL1}		0	-	0.3*VCI	V

7. Backlight Characteristics

Item	syb	Min	Typ	Max	Unit	Condition
Voltage	Vf	16.2	18	19.8	V	IF=100mA
Number of LED	-	24			pcs	-
Power Consumption	PWF	-	1800	-	mW	-
LED life-span	-	(25000)	-	-	Hrs	-

8. Touch Panel characteristics

Item	Symbol	Condition
Structure	Only G-Sensor	-
Interface	IIC	-
Transmission	≥85%	Haze meter
Channels	TX:11 RX:33	-
Touch Count Max	10	-

9. Timing Characteristics

9.1 MIPI AC characteristics

HS Receiver AC Timing Characteristics

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Bandwidth per lane	-	-	-	1000	Mbps	Bandwidth selected by register 'speedup' Speedup=0 → Max=550Mbps Speedup=1→ Max=1000Mbps
Operation frequency	-	-	-	500	MHz	
UI instantaneous	UI_{INST}	1	-	12.5	ns	1
Data to Clock Skew	Tskew	-0.15	-	0.15	UI_{INST}	
Inter-lane static skew	Tskew-lane	-	-	$UI_{INST}/50$	UI_{INST}	
Data to Clock Setup Time	T_{SETUP}	0.25	-	-	UI_{INST}	2
Data to Clock Hold Time	T_{HOLD}	0.25	-	-	UI_{INST}	
Common-mode interference beyond 450MHz	$\Delta V_{CMRX(HF)}$	-	-	100	mV	4
Common-mode interference 50MHz- 450MHz	$\Delta V_{CMRX(LF)}$	-50	-	50	mV	3,6
Common-mode termination	C_{CM}	-	-	60	pF	5

Note:

(1) Total silicon and package delay budget of 0.3*UINST

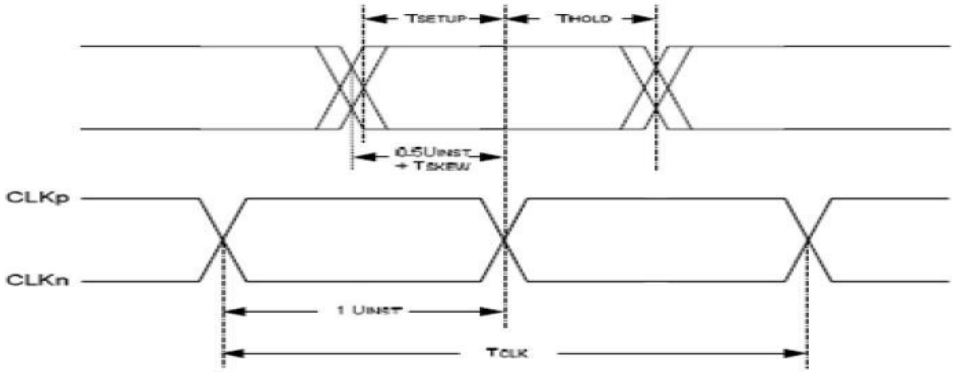
(2) Total setup and hold window for receiver of 0.3*UINST

(3) Excluding 'static' ground shift of 50mV

(4) =VCMRX (HF) is the peak amplitude of a sine wave superimposed on the receiver input

(5) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

(6) Voltage difference compared to the DC average common-mode potential.



LP Receiver AC Timing Characteristics

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Input pulse rejection	e_{SPIKE}	-	-	300	V·ps	1,2,3
Minimum pulse width response	T_{MIN-RX}	20	-	-	ns	
Peak interference amplitude	V_{INT}	-	-	200	mV	
Interference frequency	f_{INT}	450	-	-	MHz	
Logic 1 input voltage	V_{IH}	880	-	-	mV	
Logic 0 input voltage, not in ULP State	V_{IL}	-	-	550	mV	
Logic 0 input voltage, ULP State	$V_{IL-ULPS}$	-	-	300	mV	
Input Hysteresis	V_{HYST}	25	-	-	mV	
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV	
Logic 0 contention threshold	V_{ILCD}	-	-	200	mV	

Note:

(1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1state.

(2) An impulse less than this will not change the receiver state.

(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

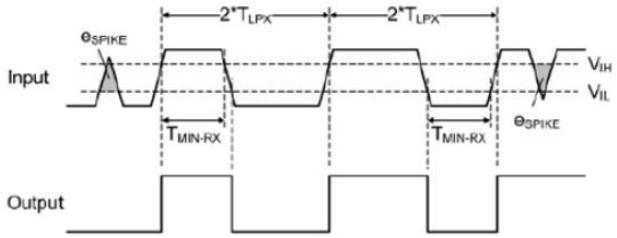
9.2 MIPI DC characteristics

(VCC=1.5V, VDD=3.3V,AVDD=12V, VSS=VSSA=0V, TA=-20 to +85℃)

Parameter	Symbol	MIN.	Typ.	MAX.	UNIT	Conditions
VDD Input low voltage level	Vil1	0	-	0.3*VDD	V	For the VDD domain inputs.
VDD Input high voltage level	Vih1	0.7*VDD	-	VDD	V	For the VDD domain inputs.
VCC Input low voltage level	Vil2	0	-	0.2*VCC	V	For the VCC domain inputs.
VCC Input high voltage level	Vih2	0.8*VCC	-	VCC	V	For the VCC domain inputs.
I2C Low level input voltage	Vil3	1.65		VDD	V	For SDA/SCL inputs
I2C High level input voltage	Vih3	0		0.2	V	For SDA/SCL inputs
Input leakage current	Ii	-	-	+/- 1	μA	For the digital, I/O circuit (Not include the pull-up/down current)
Output high voltage level	Voh	0.8*VDD	-	-	V	For VDD domain outputs, Ioh = 400uA
Output low voltage level	Vol	-	-	0.2*VDD	V	For VDD domain outputs, Iol = 400uA
Differential input leakage Current	I_{DIFFI}	-10		+10	uA	For DxP, DxN, CLKP, CLKN (With steady state inputs)
Pull low/high resistor	Ri	100K	250K	500K	ohm	For the digital Input pin VDD=3.3, VCC=1.5
Output Voltage deviation	VOD1		±20	±35	mV	Vo = AGND+0.2V ~ AGND+1.5V Vo = HAVDD-0.2V ~ HAVDD-1.5V Vo = HAVDD+0.2V ~ HAVDD+1.5V Vo = AGND+0.2V ~ AGND+1.5V
Output Voltage deviation	VOD2		±15	±20	mV	Vo = AGND+1.5V ~ HAVDD-1.5V Vo = HAVDD+1.5V ~ AVDD-1.5V
Output Voltage Offset between Chips	VOC			±20		Vo = AGND+1.5V ~ HAVDD-1.5V Vo = HAVDD+1.5V ~ AVDD-1.5V
Input level of V1 ~ V7	Vref1	HAVDD+0.2	-	AVDD-0.2	V	Gamma positive voltage input
Input level of V8 ~ V14	Vref2	0.2	-	HAVDD-0.2	V	Gamma negative voltage input
Dynamic Range of Output	Vdr	0.2	-	AVDD-0.2	V	S0 ~ S1802
Sinking Current of Outputs	IOLy	80	-	-	μA	S0 ~ S1802
Driving Current of Outputs	IOHy	80	-	-	μA	S0 ~ S1802
Digital Operation current	Idd	-	TBD	-	mA	
Digital Stand-by current	Ist1	-	TBD	-	μA	
Analog Operation current	Idda	-	TBD	-	mA	
Analog Stand-by current	Ist2	-	TBD	-	μA	

LP Receiver DC Specification

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Logic 1 input voltage	V_{IH}	880	-	-	mV	
Logic 0 input voltage, not in ULP State	V_{IL}	-	-	550	mV	
Input hysteresis	V_{HYST}	25	-	-	mV	



Line Contention Detection

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV	
Logic 0 contention threshold	VILCD	-	-	200	mV	

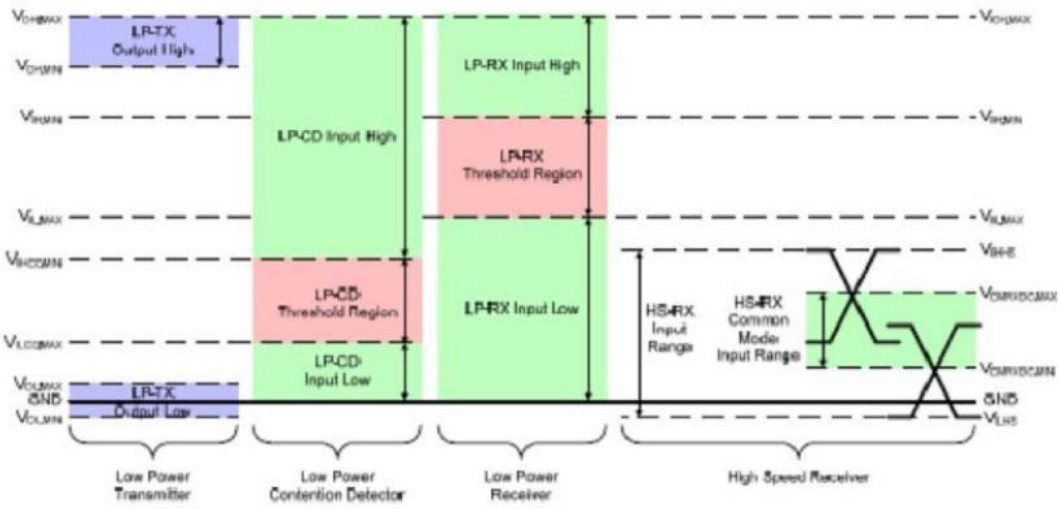
HS Receiver DC Specification

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Operation Voltage	VDD	1.5-10%	1.5	1.5+10%	mV	
Differential Input Voltage	|VID|	70	200	260	mV	
Common Mode Voltage	$V_{CMRX(DC)}$	70	-	330	mV	
Differential Input High Threshold Voltage	VTH	-	-	70	mV	
Differential Input Low Threshold Voltage	VTL	-70	-	-	mV	
Singled-ended input high voltage	V_{IHHS}	-	-	460	mV	
Singled-ended input low voltage	V_{ILHS}	-40	-	-	mV	
Singled-ended threshold for HS termination enable	$V_{TERM-EN}$	-	-	450	mV	
Differential input impedance	Z_{ID}	80	100	125	ohm	
Pin leakage current	I_{LEAK}	-10	-	10	uA	
Common-mode interference beyond 450MHz	$\Delta V_{CMRX(HF)}$	-	-	100	mV	
Common-mode interference 50MHz - 450MHz	$\Delta V_{CMRX(LF)}$	-50	-	50	mV	
Common-mode termination	C_{CM}	-	-	60	pF	
Embedded Termination	R_T	90	100	110	ohm	2bits RT_SEL[1: 0] for termination resistor selection 00 → 200ohm 10 , 01→ 150ohm 11 → 100ohm (default) 1bit ERMR_EN for termination resistor enable TERMR_EN=0, termr disable R=(OPEN) TERMR_EN=1, termr enable

Note:

(1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

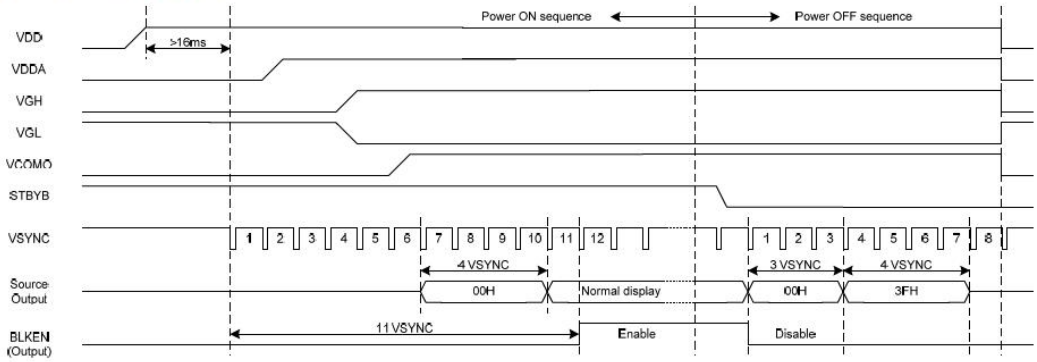
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.



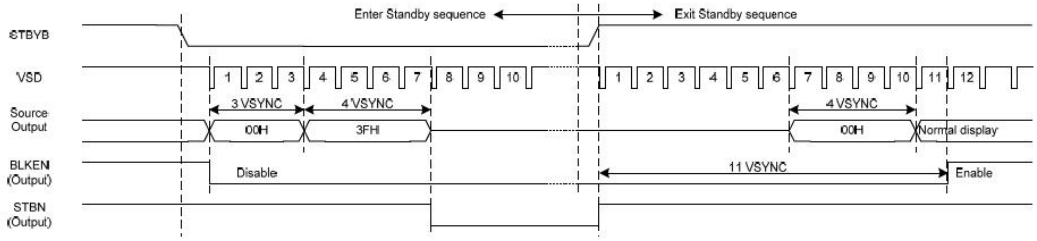
9.3 Power On/Off sequence

In order to prevent IC from power on reset fail, the rising time (T_{POR}) of the digital power supply VDD should be maintained within the given specifications. Refer to "AC Characteristics" for more detail on timing.

Power-On/Off Timing Sequence:



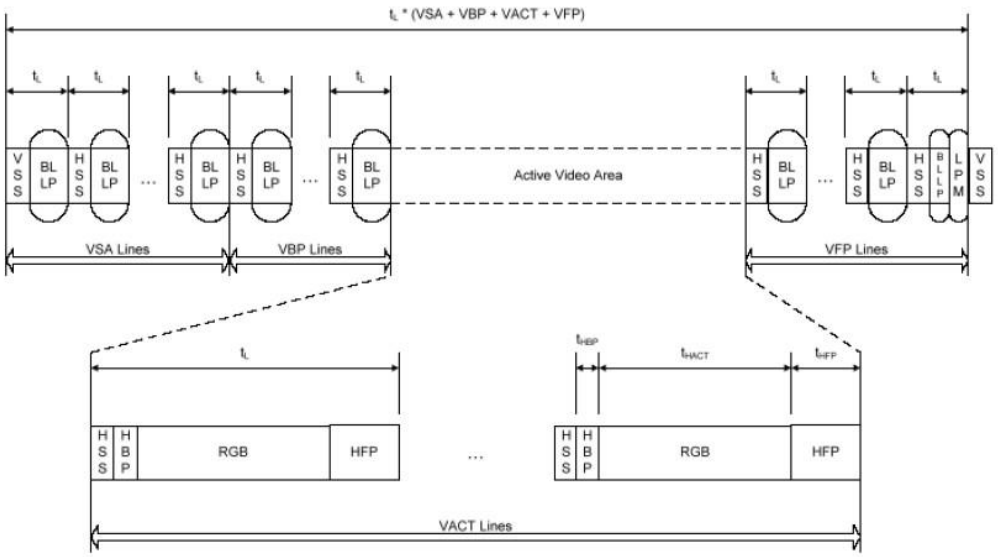
Enter and Exit Standby Mode Sequence:



9.4 MIPI Interface

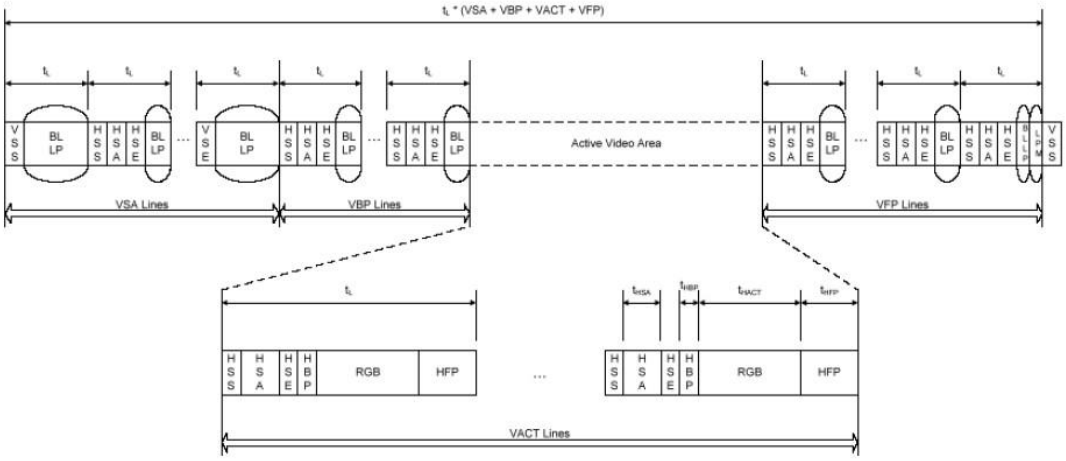
Non-Burst Mode with Sync Event

This mode is a simplification of Non-Burst Mode with Sync Pulse. Only the start of each synchronization pulse is transmitted. The peripheral may regenerated Sync as needed from each Sync Event packet received.



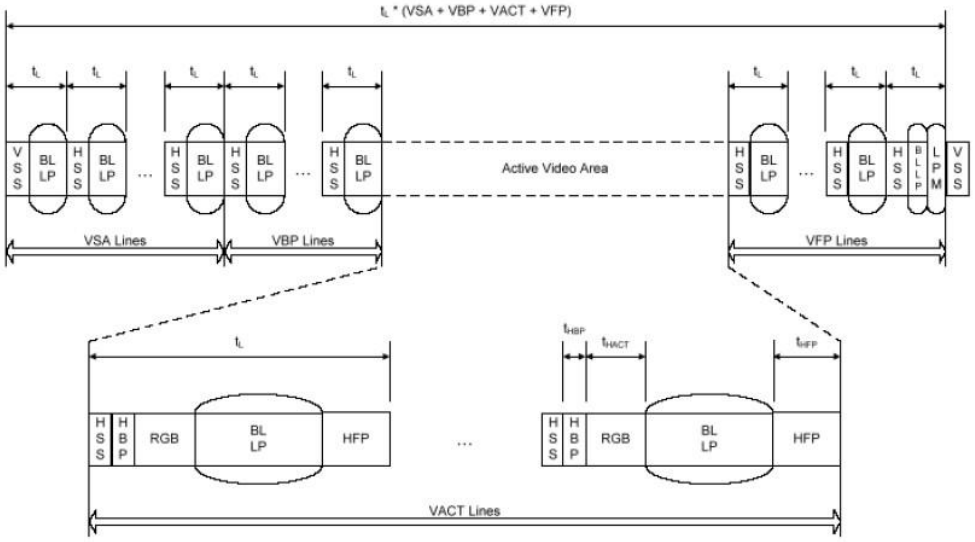
Non-Burst Mode with Sync Pulse

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel transmission rates, and width of timing events like sync pulse.



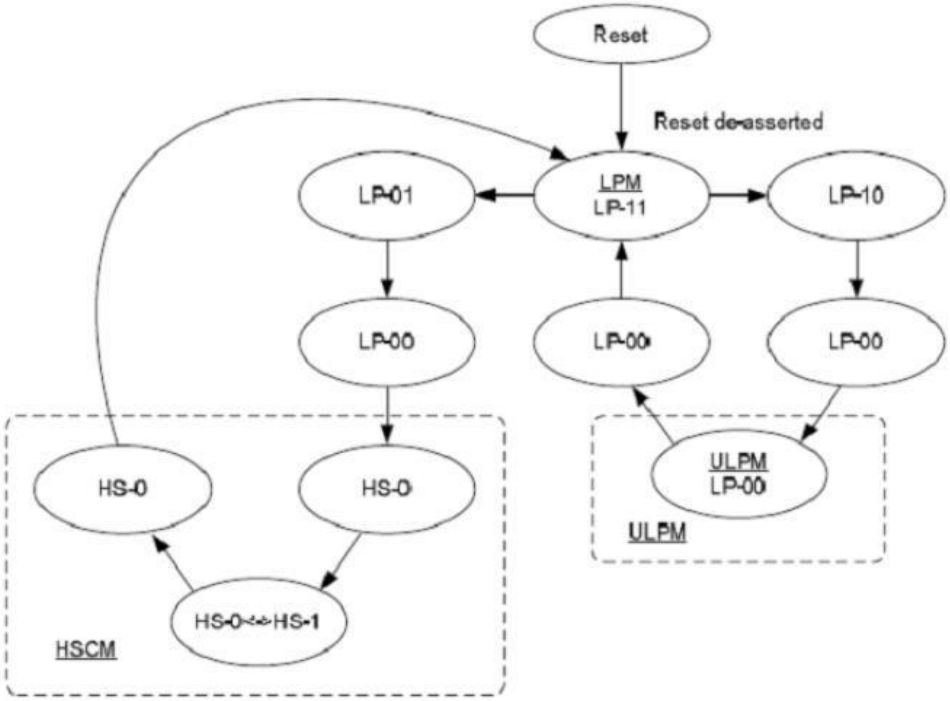
Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format.



Power Management

DSI-CLK_P/M can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM) and High Speed Clock Mode (HSCM). When LPM, ULPM, enter in LPM/ULPM and Leaving out HSCM case, the DSI-CLK_P/M is single end mode.

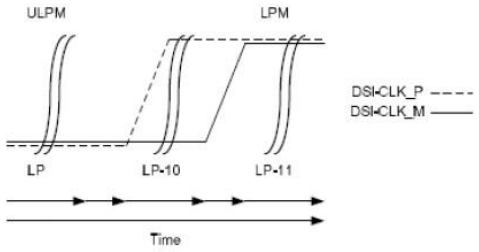


Low Power Mode (LPM)

DSI-CLK_P/M lanes are driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 state code, in three different ways:

(1) After Reset, => LP-11

(2) After DSI-CLK_P/M lanes are leaving ULPM (LP-00) => LP-10 => LP-11 (LPM)

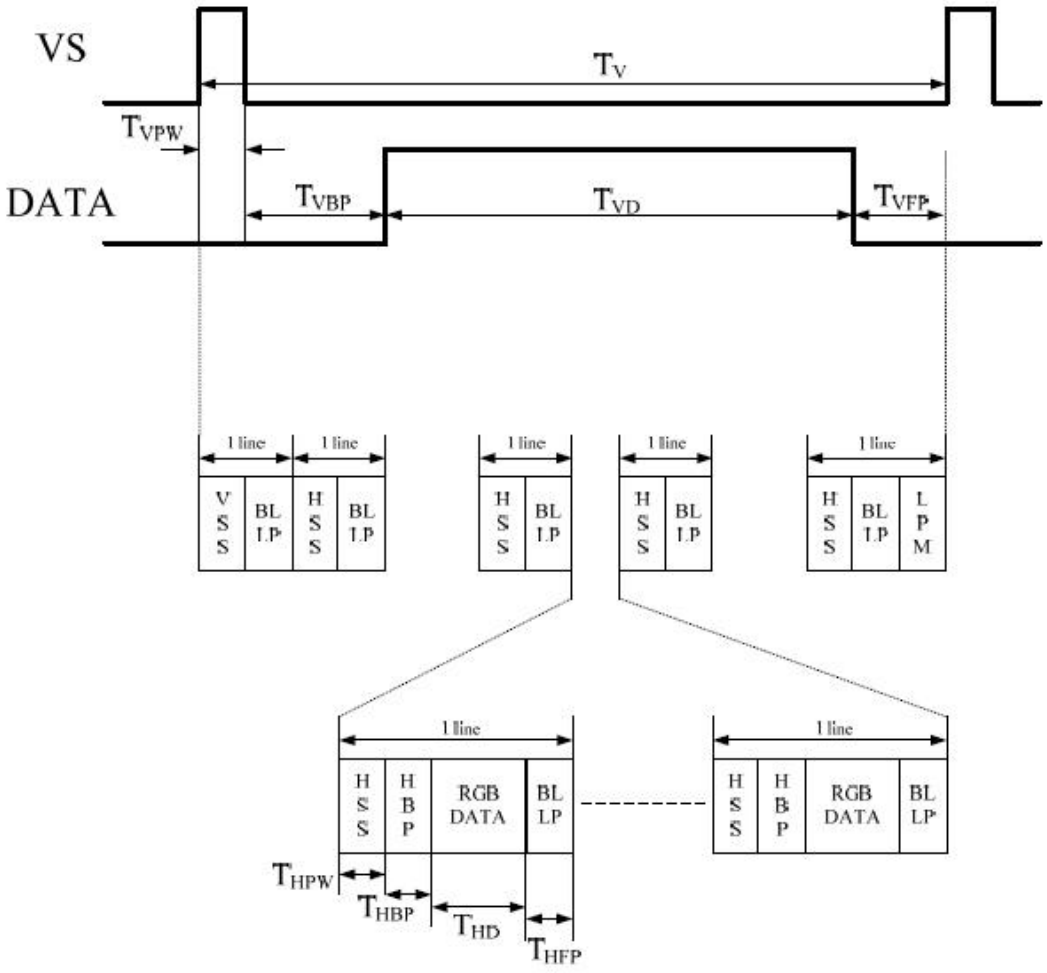


From ULPM to LPM

(3) After DSI-CLK_P/M lanes are leaving HSCM (HS-0 or HS-1) => HS-0 => LP-11 (LPM)

SS

9.5 Data Input Format for MIPI



10. Initial Code

Please consult our technical department for detail information.

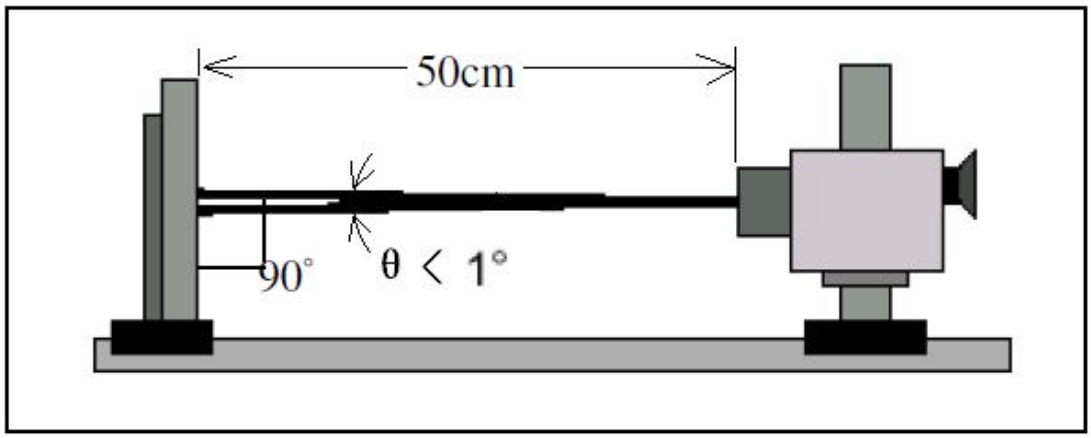
11. Electro-Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Response time	Tr+Tf	θ =0° ∅=0° Ta=25℃	-	35	-	ms	4
Uniformity （Five point）	δ WHITE		-	80	-	%	7
Contrast ratio	Cr		-	900	-	-	3 ,5
Surface Luminance (w/o CTP)	Lv		-	500	-	-	3 ,7
Viewing angle range	θ	∅ = 90°	80	85	-	deg	6
		∅ = 270°	80	85	-	deg	
		∅ = 0°	80	85	-	deg	
		∅ = 180°	80	85	-	deg	
Color filter chromaticity (x, y)	R_X	θ = ϕ = 0°	TBD	TBD	TBD	-	7
	R_Y		TBD	TBD	TBD		
	G_X		TBD	TBD	TBD		
	G_Y		TBD	TBD	TBD		
	B_X		TBD	TBD	TBD		
	B_Y		TBD	TBD	TBD		
	Wx		TBD	TBD	TBD	-	-
	Wy		TBD	TBD	TBD	-	-
NTSC	%	θ = ϕ = 0	-	60	-	%	-

Note 1: Ambient temperature=25℃±2 ℃

Note 2: To be measured in the dark room with backlight unit.

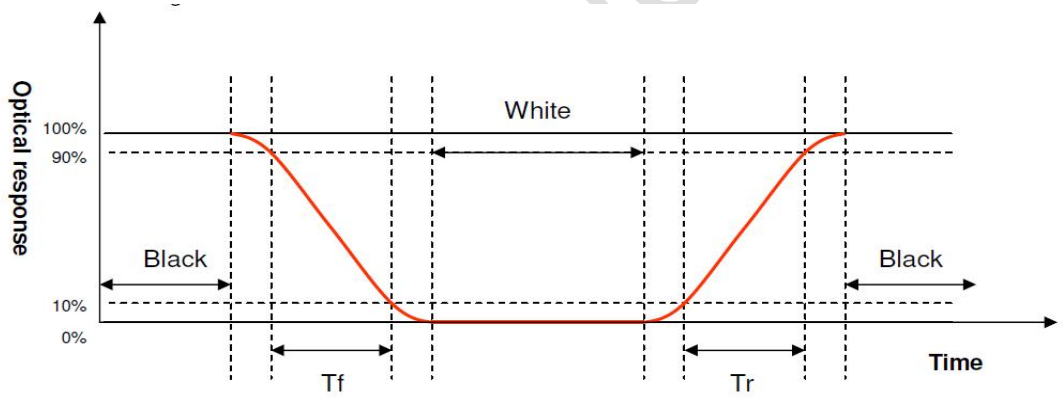
Note 3: To be measured at the center area of panel with a viewing cone of 1 by Topcon luminance meter BM-7A, after 10 minutes operation (module).



Note 4: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (rising time) and from "white" to "black" (falling time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.

Refer to figure as below.



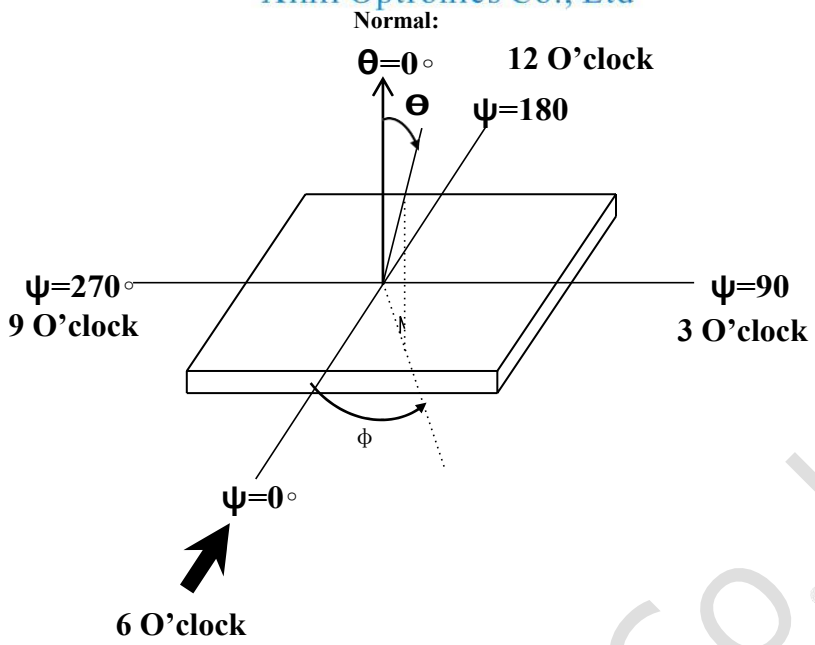
Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

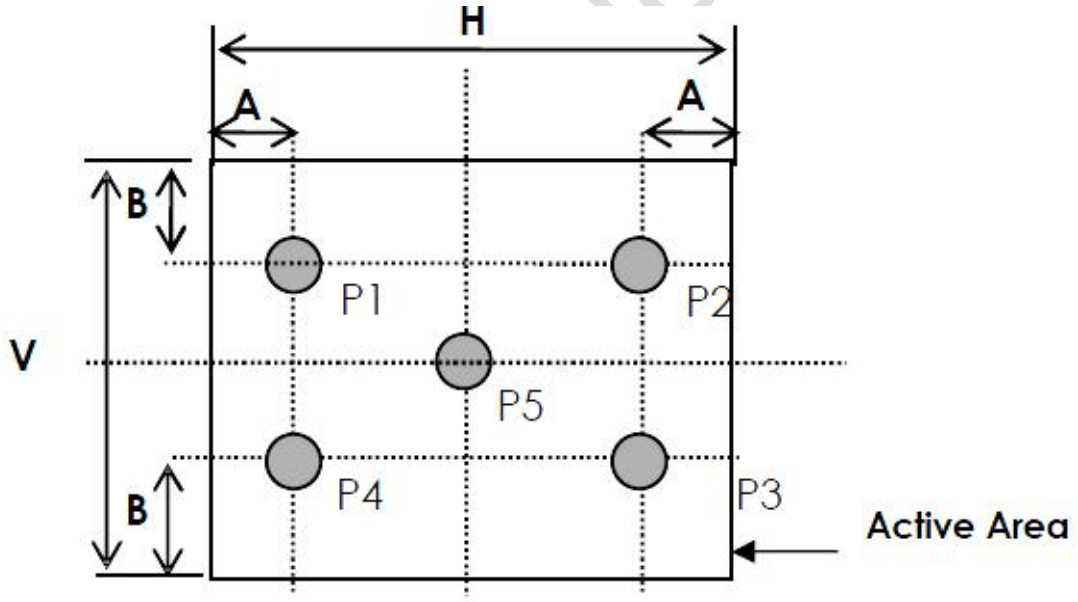
Note 6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10 for TFT module. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.



Note 7. Surface luminance is the LCD surface from the surface with all pixels displaying white. Refer to figure as below.

Measuring method for Contrast ratio, surface luminance, Luminance uniformity，CIE (x, y) chromaticity



A : 5 mm B : 5 mm H,V : Active Area

Light spot size Æ =7mm, 500mm distance from the LCD surface to detector lens

measurement instrument is TOPCON's luminance meter BM-7A

Uniformity definition= [min of 5point/max of 5points]x100%

Lv = Surface Luminance with all white pixels (P5)

12. Reliability Test

			℃,
			℃,
			℃,
			℃,
			℃, %
		-30℃← →25℃ ← →80℃ 30min←→5min←→30min ◄——————————► one cycle	℃ ℃,
			—
			—

13. Precautions for Operation and Storage

1. Precautions for Operation

e that all conductive parts on the complete unit, where the LCD is integrated, are not floated.

2. Precautions for Storage

℃ ℃

℃

3. Warranty period

13. Package Specification

TBD.

****Declaration：Products are guaranteed halogen-free and meet ROHS requirements.**