SPECIFICATION

PRODUCT NO. : **TCXD101IBLMA-816**
VERSION : **Ver 2.1**
ISSUED DATE : **2022-11-28**

This module uses ROHS material

FOR CUSTOMER： _____

■：APPROVAL FOR SPECIFICATION
□：APPROVAL FOR SAMPLE

DATE	APPROVED BY

Xinli Optoelectronics ：

Presented by	Reviewed by	Organized by
王漢鋒	趙春曉	王俊傑

Note:

1.Xinli Optoelectronics reserves the right to make changes without further notice to any products herein to improve reliability, function or design.

1. Revision Recode

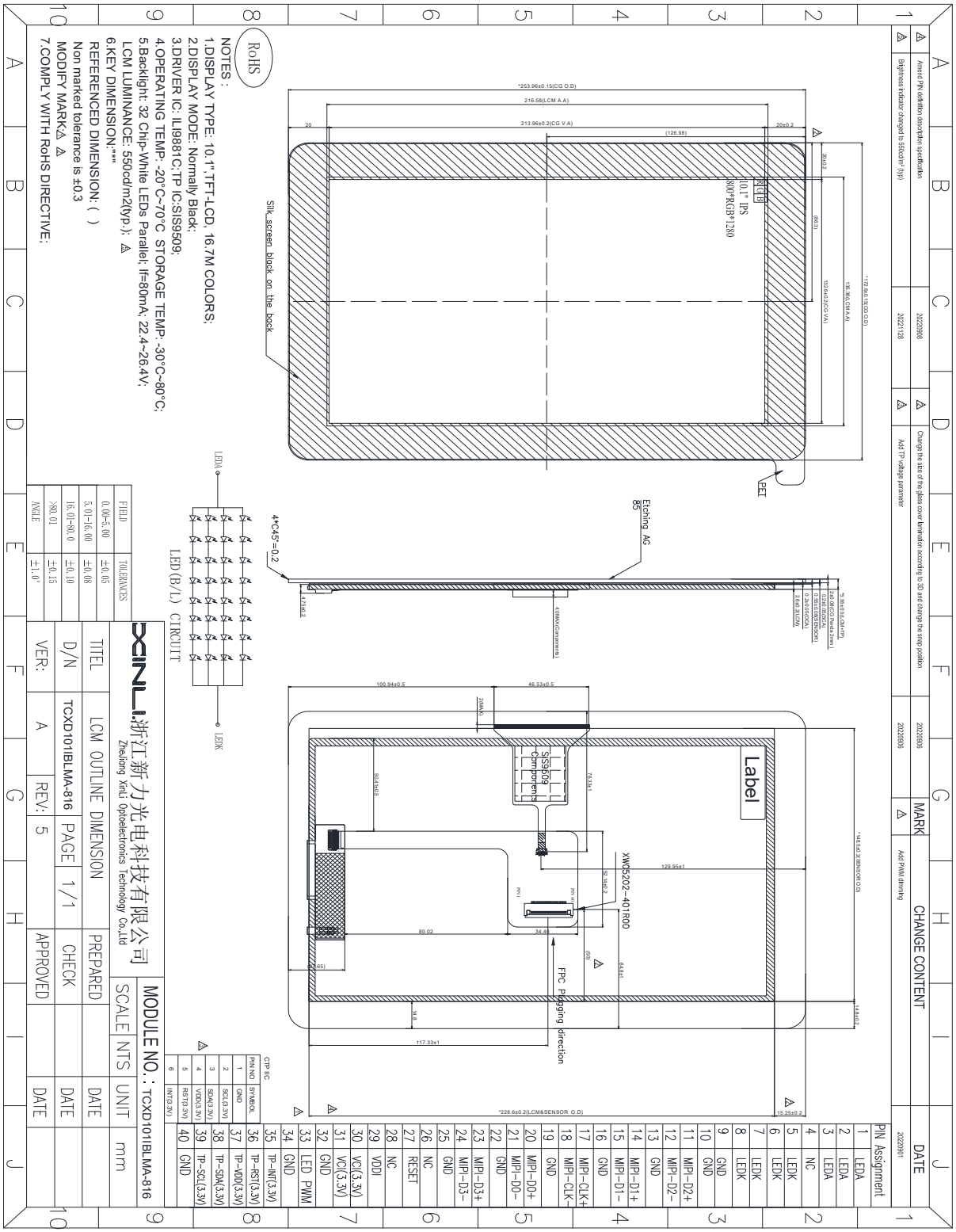
Revision	Description	Date
1.0	Initial Release	2022/08/30
1.1	Update the datasheet	2022/8/31
1.2	Add PWM dimming	2022/9/1
1.3	Change the size of the glass cover lamination according to 3D and change the snap position	2022/9/7
1.4	Add TP voltage parameter	2022/9/7
1.5	Update the datasheet	2022/9/8
1.6	Adding IIS standards	2022/9/21
1.7	7.0 Increase LCD and TP power consumption	2022/10/13
1.8	LED PWM notes	2022/10/25
1.9	Added description and definition of RESET	2022/10/25
2.0	Update Capacitive Touch Specifications	2022/11/14
2.1	Brightness indicator changed to 550cd/m^2 (typ)	2022/11/28

2. General Description and Features

The 10.1 inch Module named TCXD101IBLMA-816 is a-Si TFT-LCD module, which is the type of transmissive. It is consisted of TFT-LCD Panel, one Driver IC ,one FPC and one Back-Light one TP unit. Features of this product are listed in the following table.

NO	Item	Contents	Unit
(1)	Module Outline	172.6(H)*253.96(V)*5.55(T)	mm
(2)	LCD Active area	135.36(H)*216.58(V)	mm
(3)	CG Active area	132.6(H)*213.96(V)	mm
(4)	Dot Number	800*3(RGB)*1280	/
(5)	Dot size	0.1692*0.1692	mm
(6)	LCD type	TFT Transmissive,Normal Black	/
(7)	Display Color	16.7M	/
(8)	Viewing direction	ALL	O'clock
(10)	Power Supply	3.3(TYP)	V
(12)	Interface	0.5mm 40pin	/
(13)	Interface type	MIPI	/
(14)	Module weight	TBD	g
(15)	Structure type	TP+OCA+LCM	/
(16)	Touch control chip	SIS9509	/
(17)	Interface Type	IIC	/
(18)	Touch points	10 point touch	/
(19)	The first layer	2.0 mm Cover Lens	/
(20)	The second floor	0.2 mm OCA	/
(21)	Third layer	0.55 SENSOR	/
(22)	Cover lens surface treatment	Etching AG 9%±3%; Ra≤0.08; Gloss 85±10。	/
(23)	Surface strength	7H,750g.	H

3. Mechanical Dimension



4. Interface Pin Connection

4.1.Recommended connector model XW05202-401R00(40PIN)

No.	Symbol	I/O	Function
1	LEDA	P	Backlight anode
2	LEDA	P	Backlight anode
3	LEDA	P	Backlight anode
4	NC	-	No connect
5	LEDK	P	Backlight ground
6	LEDK	P	Backlight ground
7	LEDK	P	Backlight ground
8	LEDK	P	Backlight ground
9	GND	P	Ground
10	GND	P	Ground
11	MIPI-D2+	I	MIPI-DSI data Lane 2 positive-end input/output pin
12	MIPI-D2-	I	MIPI-DSI data Lane 2 negative-end input/output pin
13	GND	P	Ground
14	MIPI-D1+	I	MIPI-DSI data Lane 1 positive-end input/output pin
15	MIPI-D1-	I	MIPI-DSI data Lane 1 negative-end input/output pin
16	GND	P	Ground
17	MIPI-CLK+	I	MIPI-DSI clock Lane positive-end input pin
18	MIPI-CLK-	I	MIPI-DSI clock Lane negative-end input pin
19	GND	P	Ground
20	MIPI-D0+	I	MIPI-DSI data Lane 0 positive-end input/output pin
21	MIPI-D0-	I	MIPI-DSI data Lane 0 negative-end input/output pin
22	GND	P	Ground
23	MIPI-D3+	I	MIPI-DSI data Lane 3 positive-end input/output pin
24	MIPI-D3-	I	MIPI-DSI data Lane 3 negative-end input/output pin
25	GND	P	Ground
26	NC	-	No connect
27	RESET	I	- The external reset input Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.
28	NC	-	No connect

29	VDDI	P	POWER(1.8V/3.3V)
30	VCI(3.3V)	P	POWER(3.3V)
31	VCI(3.3V)	P	POWER(3.3V)
32	GND	P	Ground
33	LED PWM	O	LCD backlight control PWM output pin. （NOTE 1）
34	GND	P	Ground
35	TP-INT	I	TP Indicate coor dinate ready(3.3V)
36	TP-RST	P	TP Reset pin(3.3V) Low active power on reset signal
37	TP-VDD	P	TP Power Supply(3.3V)
38	TP-SDA	I	TP I2C:serial data(3.3V)
39	TP-SCL	I	TP I2C:serial clock(3.3V)
40	GND	P	Ground

NOTE 1:

The backlight brightness and LED_PWM output are controlled through the following four registers.

5.3.29. Write Display Brightness Value (51h)

Command Page			Page 0								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
51h	1st	W	0	0	0	0	DBV[11:8]				00h
	2nd	W	DBV[7:0]								00h

Description

51h: WRDISBV (Write Display Brightness).

This command is used to adjust the brightness value of the display.

DBV[11:0]: 12 bit, for display brightness of manual brightness setting and the CABC in the ILI9881C. PWM output signal and LEDPWM pin will control the LED driver IC in order to control the display brightness. In principle relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness.

Restriction

None

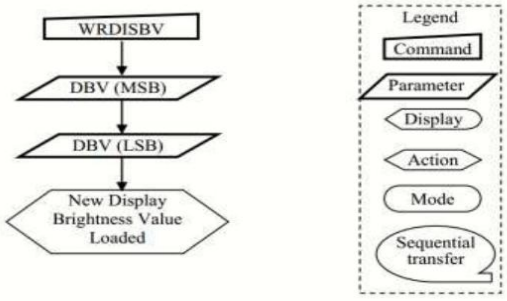
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart



5.3.30. Read Display Brightness Value (52h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
52h	1st	R	0	0	0	0	DBV[11:8]				00h
	2nd	R	DBV[7:0]								00h

Description

52h: RDDISBV (Read Display Brightness Value).

This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.

In principle the relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness.

DBV[11:0] is reset when display is in sleep-in mode.

DBV[11:0] is '0' when bit BCTRL of "5.3.31Write CTRL Display Value (53h)" command is '0'.

DBV[11:0] is manual set brightness specified with "5.3.31Write CTRL Display Value (53h)" command when bit BCTRL is '1'.

Restriction

None

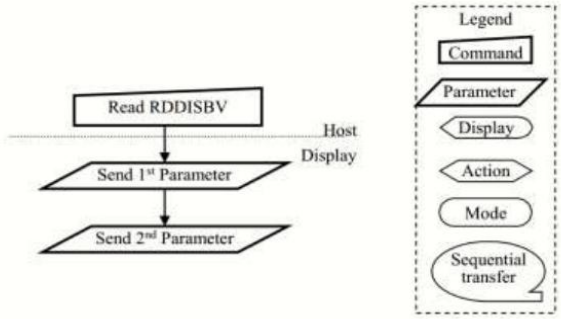
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart



5.3.31. Write CTRL Display Value (53h)

Command Page			Page 0								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
53h	1st	W	0	0	BCTRL	0	DD	BL	0	0	00h

Description

53h: WRCTRLD (Write Control Display).

This command is used to control the display brightness.

BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block Off (DBV[11:0] = 0000h)
1	Brightness Control Block On (DBV[11:0] is active)

DD: Display Dimming Control.

DD	Description
0	Display Dimming Off
1	Display Dimming On

BL: Backlight Control On/Off

BL	Description
0	Backlight Control Off
1	Backlight Control On

Dimming function is adapted to the brightness registers for display when the bit BCTRL is changed at DD = 1, e.g.

BCTRL: 0-> 1 or 1-> 0.

When the BL bit changes from 'ON' to 'OFF', backlight is turned off without gradual dimming, even if Display Dimming On (DD = 1) are selected.

Restriction

None

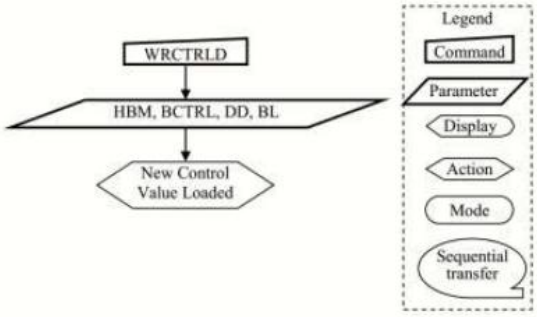
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.3.32. Read CTRL Display Value (54h)

Command Page			Page 0								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
54h	1st	R	0	0	BCTRL	0	DD	BL	0	0	00h

Description

54h: RDCTRLD (Read Control Value Display).

This command returns the display brightness control values.

BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block Off (DBV[11:0] = 0000h)
1	Brightness Control Block On (DBV[11:0] is active)

DD: Display Dimming Control.

DD	Description
0	Display Dimming Off
1	Display Dimming On

BL: Backlight Control On/Off

BL	Description
0	Backlight Control Off
1	Backlight Control On

Dimming function is adapted to the brightness registers for display when the bit BCTRL is changed at DD = 1, e.g. BCTRL: 0-> 1 or 1-> 0.

When the BL bit changes from 'ON' to 'OFF', backlight is turned off without gradual dimming, even if Display Dimming On (DD = 1) are selected.

Restriction: None

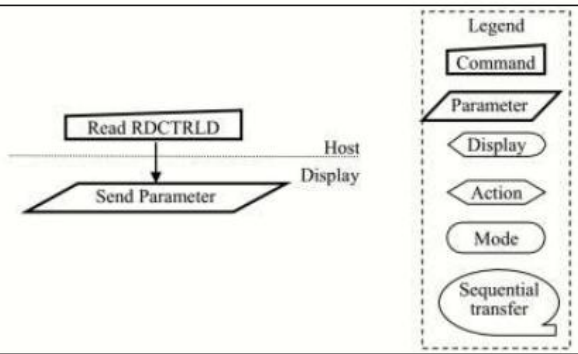
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5. Maximum Rating

Item	Symbol	Rating	Unit
Operating temperature	Top	-20 to 70	℃
Storage temperature	Tst	-30 to 80	℃
power supply	VCI	0.3 ~ 7.0V	V

NOTE:

If the module was used these absolute maximum ratings as above, it may be damaged permanently. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability. VCI>GND must be maintained.

6. Electrical Characteristics

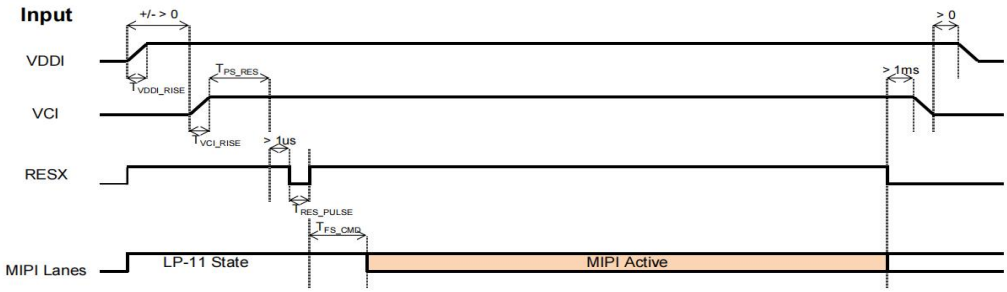
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Analog power supply		VCI	-	2.5	3.3	3.6	V
Digital operating voltage		VDDI	-	1.65	1.8	3.6	
Logic input signal Voltage	H level	V_{IH}		0.7*VDDI	-	VDDI	V
	L level	V_{IL}		GND	-	0.3*VDDI	V
Logic output signal Voltage	H level	V_{OH}		0.8*VDDI	-	VDDI	V
	L level	V_{OL}		GND	-	0.2*VDDI	V

7. Characteristics

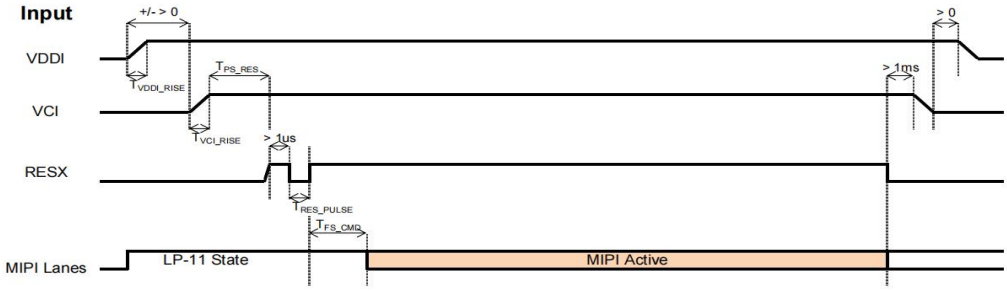
Item	syb	Min	Typ	Max	Unit	Condition
Backlight Voltage	Vin (Vin=LEDA -LEDK)	22.4	24	26.4	V	-
Backlight Led current	Iled	-	80	-	mA	
Backlight Number of LED	-	32		-	pcs	
Backlight Power Consumption	PWF	-	1920	-	mW	-
LED life-span	-	-	(50000)	-	Hrs	-
LCD Power Consumption	PWF	-	220	264	mW	-
TP Power Consumption	PWF	-	110	132	mW	-

8. Power on/off Sequence

Case A:



Case B:



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

9. AC Electrical Characteristics

18.4.2. High Speed Mode – Clock Channel Timing

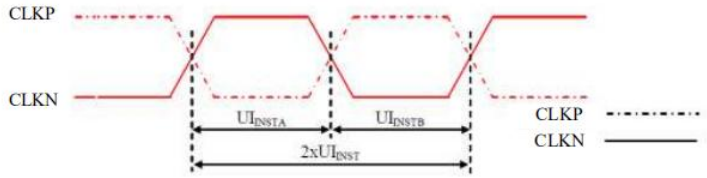


Figure 116: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

18.4.3. High Speed Mode – Data Clock Channel Timing

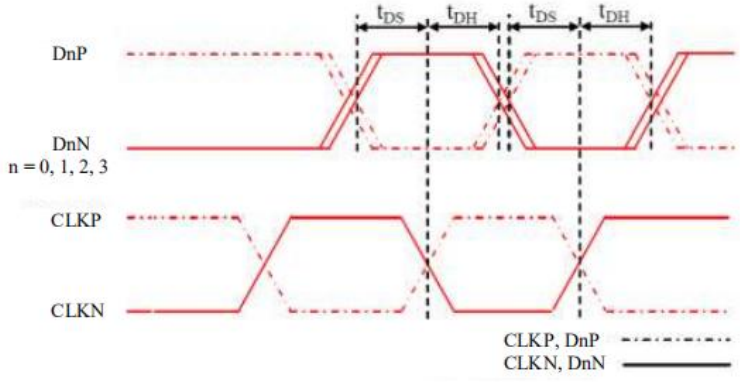


Figure 117: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

18.4.4. High Speed Mode – Rising and Falling Timings

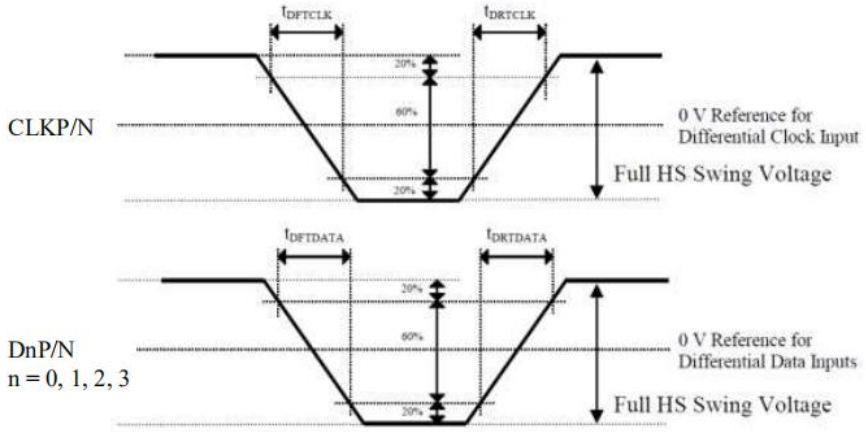


Figure 118: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

18.4.5. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

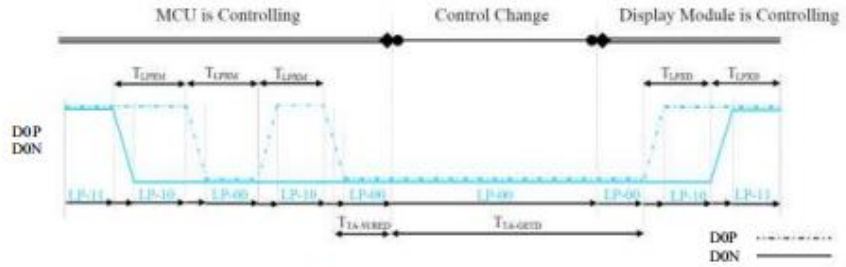


Figure 119: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

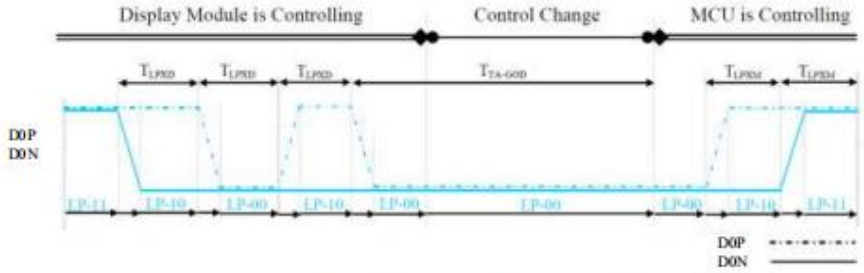


Figure 120: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

18.4.6. Data Lanes from Low Power Mode to High Speed Mode

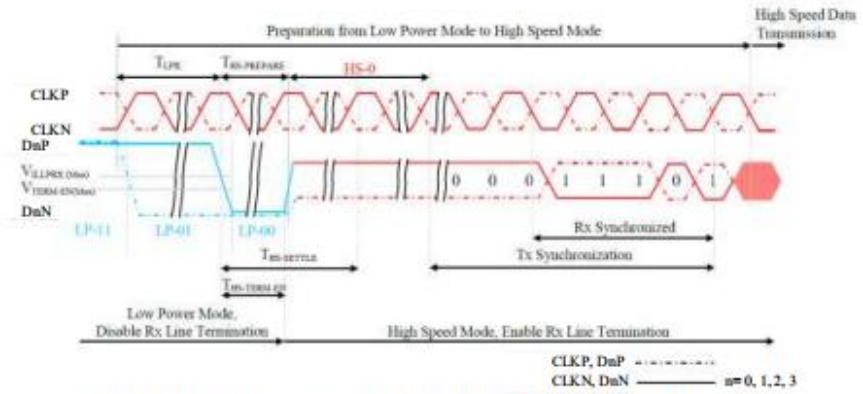


Figure 121: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

18.4.7. Data Lanes from High Speed Mode to Low Power Mode

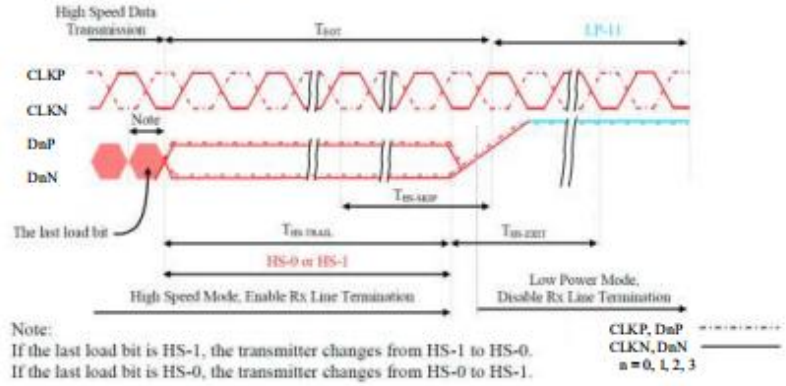


Figure 122: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

18.4.8. DSI Clock Burst – High Speed Mode to/from Low Power Mode

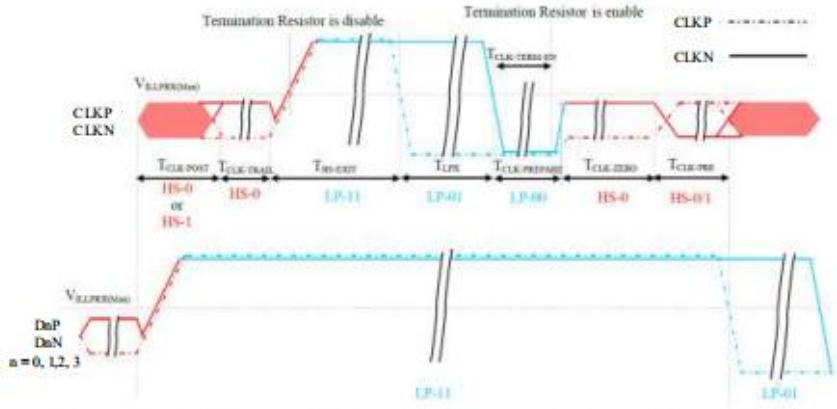
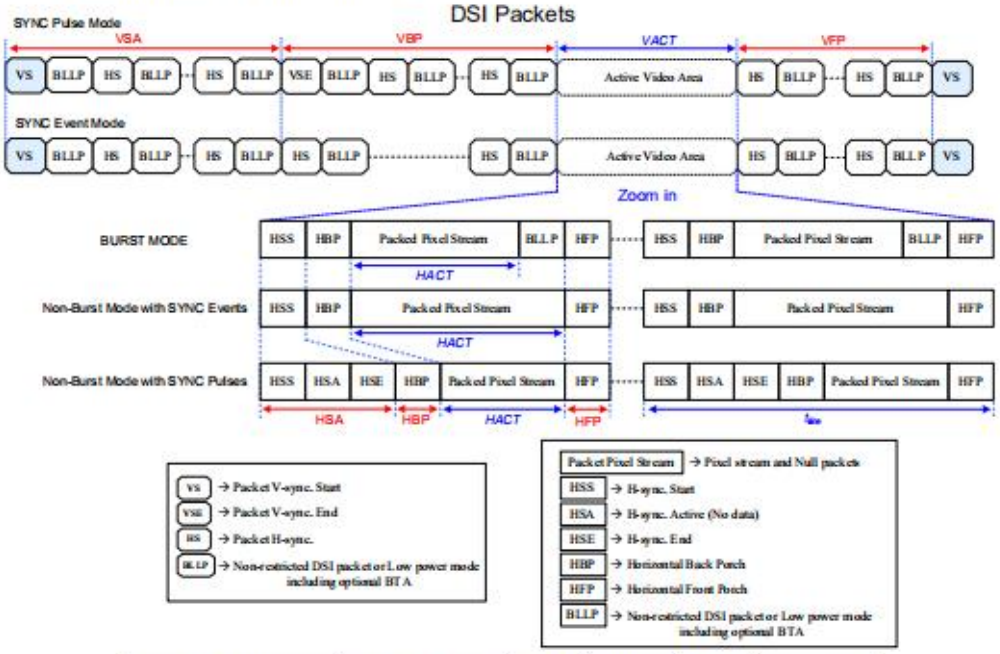


Figure 123: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

18.4.9. Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example : BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

18.4.10. Reset Timing

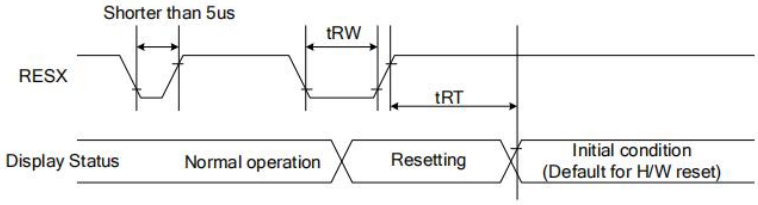


Figure 124: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

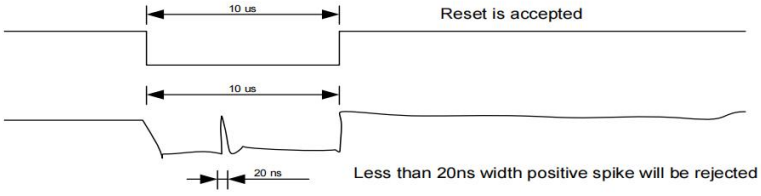


Figure 114: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

10. Touch Characteristics

10.1 Touch Spec

Item 项目	Specification 规格	Remark 备注
The operating system /操作系统	/	
Touch points /触摸点数	10 点触摸	
IC Working voltage/工作电压	3.3V	
响应时间 Chatting Times	<30ms	

10.2 Interface Pin Connection

Pin NO. pin 脚	Symbol 符号	I/O 输入/出	Description 描述	When not in use 未使用时的连接
1	GND		AGND	
2	SCL		I2C clock signal I2C 时钟信号	
3	SDA		I2C data signal I2C 数据信号	
4	VDD		Analog voltage input 模拟电压输入	
5	RST		Interrupt signal 中断信号	
6	INT		System reset pin Low level effective 系统复位脚 低电平有效	

10.3 I²C Communication

10.3.1 Absolute Maximun Ratings

Table 1 shows SIS9509 stress ratings only. Extended exposure to the maximum ratings might degrade device reliability. Although SIS9509 has protective circuitry to resist damage from electrostatic discharge (ESD), precautions should always be taken to avoid high voltage or electric field.

Table 1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
Tstorage	Storage Temperature	-65	150	°C	*1
Ta	Ambient Operating Temperature	-40	105	°C	
OVDD33 AVDD33	3.3V Supply Voltage	-0.3	3.6	V	

NOTES:

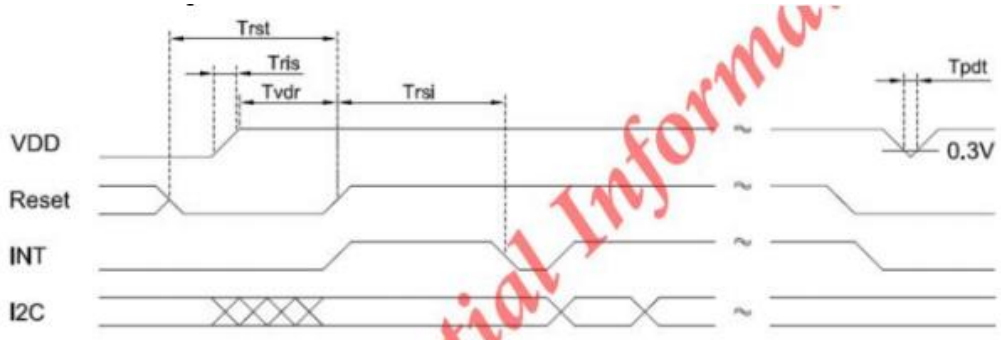
*1

A. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended period may affect reliability.

B. Higher temperature may be applied during reflow, and IC soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes.

C. Packing and Handling shall follow JEDEC J-STD-033 Moisture-Sensitivity Level 3.

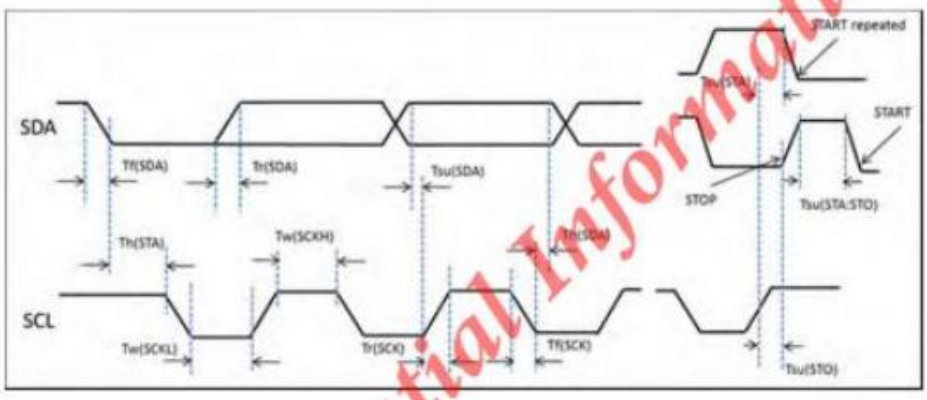
10.3.2 Power Sequence



Parameter	Description	Min	Max	Units
Tris	VDD power on Rise time from 0.1VDD to 0.9VDD	-	2	ms
Tpdt	VDD Power off lower than 0.3V Interval	5	-	ms
Tvdr	VDD power on at 3.3V to RESET# at 2.0V	5	-	ms
Trsi	Time of starting to report point after resetting	100	-	ms
Trst	Reset time	5	-	ms

10.3.3 12C Interface

Vendor	SiS
Slave Address	0x5c(7-bits addressing, programmable)
Clock rate	@400 kHz (fast mode)
Interrupt mode	Default active low, level trigger
_CID	PNP0C50
_DSM	3CDFF6F7-4267-4555-AD05-B30A3D8938DE
HID Descriptor address	0x0000



Symbol	Parameter	SCL=100KHz		SCL=400KHz		Unit
		Min	Max	Min	Max	
Tw(SCKH)	SCL clock high time	4.7		1.3		us
Tw(SCKL)	SCL clock low time	4.0		0.6		
Tsu(SDA)	SDA setup time	250		100		ns
Th(SDA)	SDA data hold time	0		0	900	
Tr(SDA) Tr(SCK)	SDA&SCL rise time		1000		300	
Tf(SDA) Tf(SCK)	SDA&SCL fall time		300		300	
Th(STA)	Start condition hold time	4.0		0.6		us
Tsu(STA)	Repeated Start condition setup time	4.7		0.6		
Tsu(STO)	Stop condition setup time	4.0		0.6		
Tw(STO:STA)	Stop to Start condition time(bus free)	4.7		1.3		

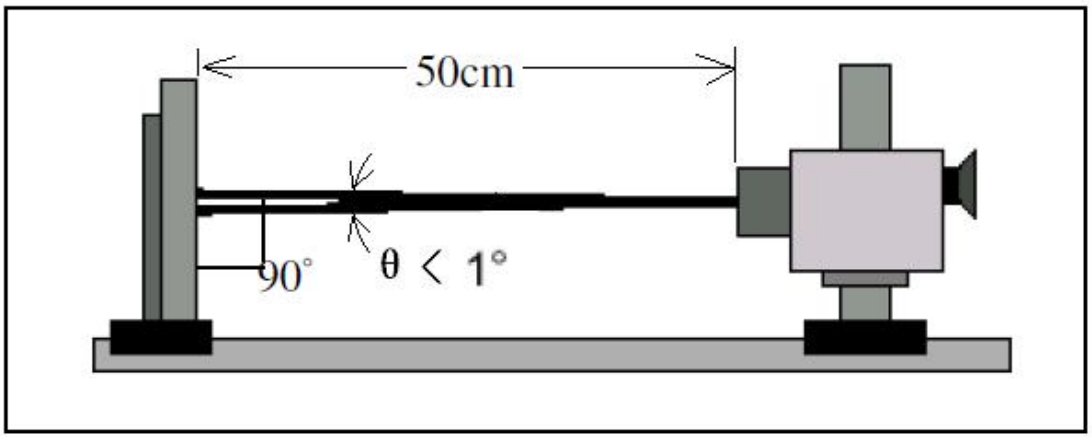
11. Electro-Optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Response time		Tr+Tf	θ =0° ∅=0° Ta=25℃	-	30	-	ms	4
Uniformity （Five point）		δ WHITE		80	-	-	%	7
Contrast ratio		Cr		600	1000	-	-	3 ,5
Surface Luminance		Lv		450	550	-	-	3 ,7
Viewing angle range		θ	∅ = 90°	-	80	-	deg	6
			∅ = 270°	-	80	-	deg	
			∅ = 0°	-	80	-	deg	
			∅ = 180°	-	80	-	deg	
Color filter chromaticity (x, y)	White	X	θ = ϕ = 0°	-	TBD	-	–	7
		Y		-	TBD	-		
	Red	X	θ = ϕ = 0°	-	TBD	-		
		Y		-	TBD	-		
	Green	X	θ = ϕ = 0°	-	TBD	-		
		Y		-	TBD	-		
	Blue	X	θ = ϕ = 0°	-	TBD	-		
		Y		-	TBD	-		

Note 1: Ambient temperature=25℃±2℃

Note 2: To be measured in the dark room with backlight unit.

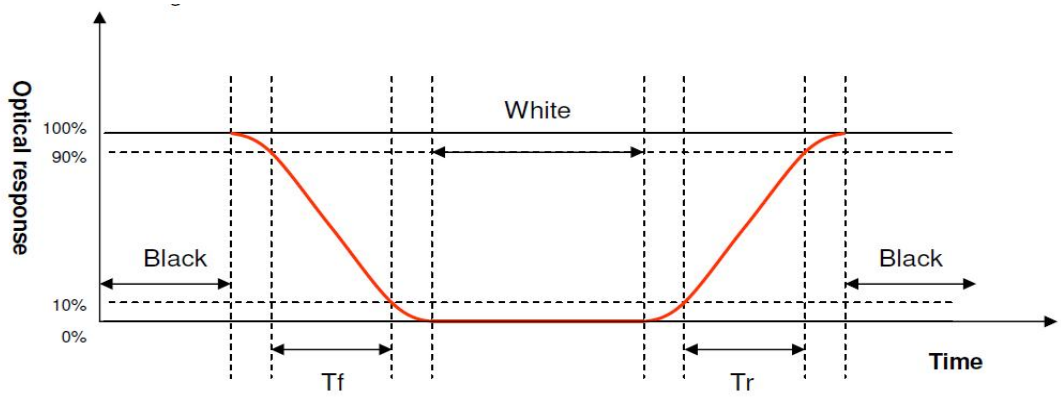
Note 3: To be measured at the center area of panel with a viewing cone of 1 by Topcon luminance meter BM-7A, after 10 minutes operation (module).



Note 4: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (rising time) and from "white" to "black" (falling time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.

Refer to figure as below.



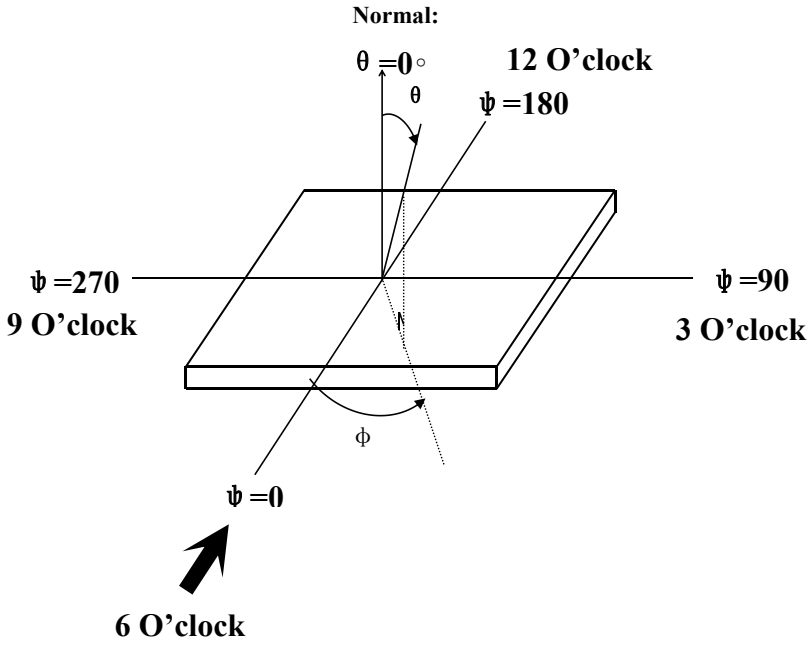
Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

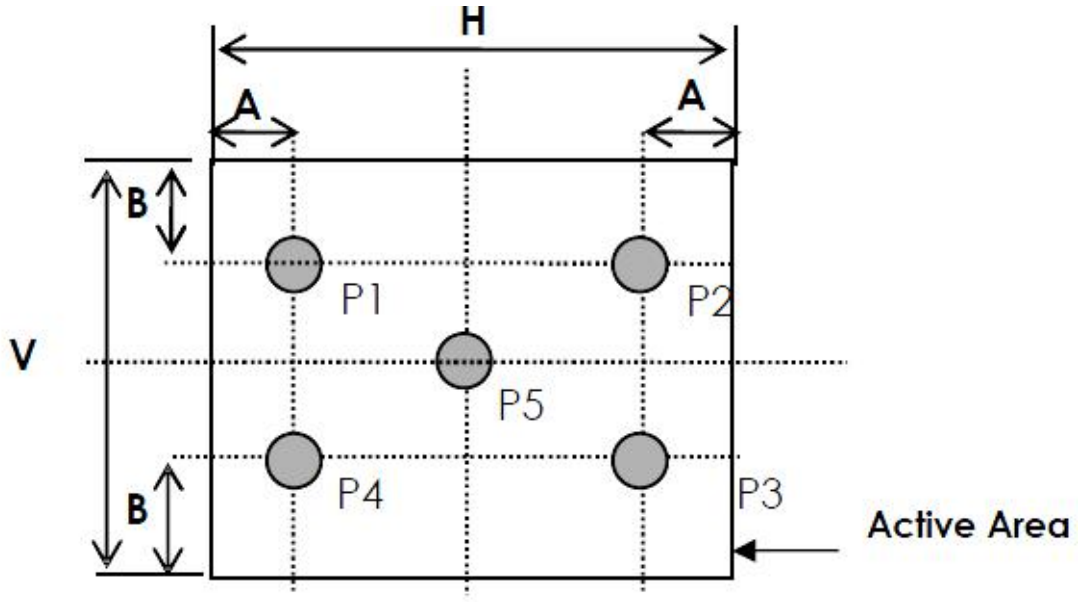
Note 6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 2, for TFT module the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.



Note 7. Surface luminance is the LCD surface from the surface with all pixels displaying white. Refer to figure as below.

Measuring method for Contrast ratio, surface luminance, Luminance uniformity，CIE (x, y) chromaticity



A : 5 mm B : 5 mm H,V : Active Area

Light spot size Æ=7mm, 500mm distance from the LCD surface to detector lens measurement instrument is TOPCON's luminance meter BM-7A

Uniformity definition= [min of 5point/max of 5points]x100%

Lv = Average Surface Luminance with all white pixels (P_1, P_2, P_3, P4, P_5)

12. Reliability Test

This standard reliability test is done only for the first lot of MP products. Customer and supplier must hold a discussion if other reliability test is requested by customer.

No.	Test Item	Test Condition	Remarks
1	High temperature storage	80℃，240H	Note1 IEC60068-2-1:2007,GB2423.2-2008
2	Low temperature storage	-30℃，240H	IEC60068-2-1:2007 GB2423.1-2008
3	Hight temperature operation	70℃，240H	IEC60068-2-1:2007 GB2423.2-2008
4	Low temperature operation	-20℃，240H	IEC60068-2-1:2007 GB2423.1-2008
5	Hight temperature /humidity storage	60℃，90%RH 240H	Note2 IEC60068-2-78 :2001 GB/T2423.3—2006
6	Temperature Cycle (Non-operation)	-20℃-25℃-70℃ 30min-5min-30min 50 cycles	Start with cold temperature, End with high temperature, IEC60068-2-14:1984,GB2423.22-2002
7	Drop Test (package)	Height:1 m, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32:1990 GB/T2423.8—1995
8	Vibration test (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (3 hours for total)(Package condition)	IEC60068-2-6:1982 GB/T2423.10—1995

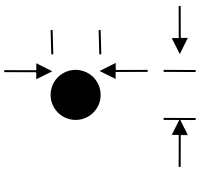
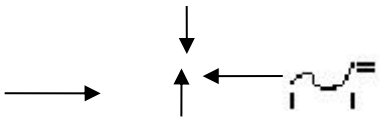
9	Electro Static Discharge (Operation)	C=150pF, R=330Ω， 5points/panel Air:± 4KV, 5 times; Contact:±2KV, 5 times; （Environment: 15℃～35℃, 30%～60%, 86Kpa～106Kpa）	IEC61000-4-2:2001 GB/T17626.2-2006

Note1: Ts is the temperature of panel's surface.

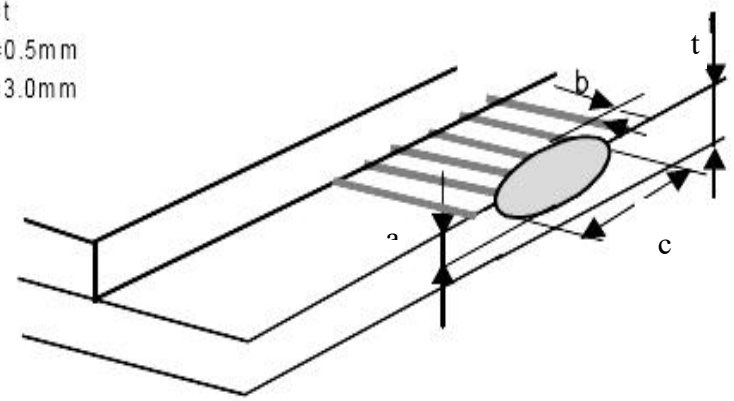
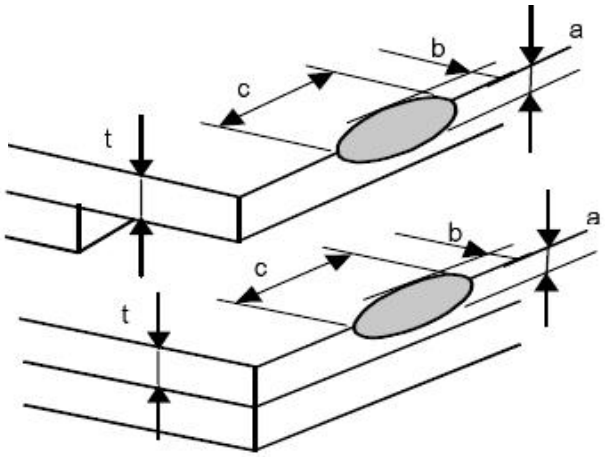
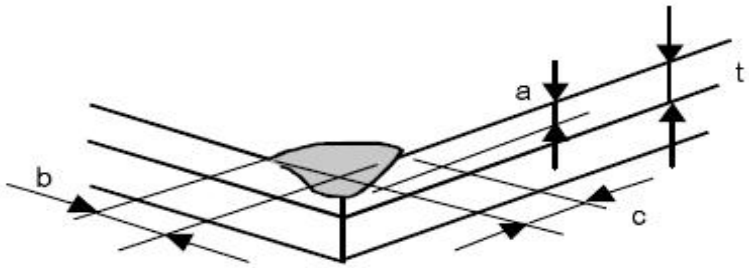
Note2: Ta is the ambient temperature of sample.

13. QUALITY LEVEL

<table>
<tr><th>Item No.</th><th>Items to be inspected</th><th>Inspection standard</th></tr>
<tr><td>12.1</td><td>LCD black spots, white spots, color spots</td><td>
<table>
<tr><td>Defect Type</td><td>Acceptable QTY</td></tr>
<tr><td>Bright Dots</td><td>2</td></tr>
<tr><td>Dark Dots</td><td>3</td></tr>
<tr><td>Total Bright and Dark Dots</td><td>4</td></tr>
</table>
The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.
Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
The bright dot defect must be visible through 2% ND filter
Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue pattern.
The size of a defective dot less than 1/2 dot is no count
</td></tr>
</table>

<table>
<tr>
<td>12.2</td>
<td>Spot Defect
（Including:
Black spot，
White spot，
Pinhole，Foreigh
particle，
Polarizer dirl）</td>
<td>Define：
φ=(x+y)/2
 
X
Y
<table>
<tr><th>Size φ (mm)</th><th>Acceptable QTY</th></tr>
<tr><td>φ≦0.20</td><td>Ignore</td></tr>
<tr><td>0.20≦φ≦0.50
Space between>5mm</td><td>5</td></tr>
<tr><td>0.50<φ</td><td>Not allowed</td></tr>
</table>
Ignore the spot distance while defect is in spec.
The distance between two spot should be larger than 20mm.</td>
</tr>
<tr>
<td>12.3</td>
<td>Line Defect
（Including:
Black spot，
White spot，
Pinhole，Foreigh
particle，
Polarizer dirl）</td>
<td>Define：
 
W
L
<table>
<tr><th>Length</th><th>Width</th><th colspan="2">Acceptable QTY</th><th>Remark</th></tr>
<tr><td></td><td></td><td>A.A</td><td>V.A</td><td></td></tr>
<tr><td>---</td><td>W≦0.1</td><td>Ignore</td><td>Ignore</td><td></td></tr>
<tr><td>L≦15</td><td>0.1＜
W≦0.2mm
且 L≦
15.0mm</td><td>3</td><td>3</td><td>No
more than
two lines
within
20mm</td></tr>
<tr><td>---</td><td>0.2< W</td><td>0</td><td>0</td><td></td></tr>
</table>
Ignore the spot distance while defect is in spec.</td>
</tr>
</table>

<table>
<tr><td></td><td></td><td colspan="3">The distance between two line should be larger than 20mm.</td></tr>
<tr><td>12.4</td><td>Polarizer bubbles</td><td colspan="3">If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.
<table>
<tr><td rowspan="2">Size</td><td colspan="2">Acceptable QTY</td></tr>
<tr><td>A.A</td><td>V.A</td></tr>
<tr><td>φ≦0.20</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.20<φ≦0.40</td><td>3</td><td>5</td></tr>
<tr><td>0.40<φ</td><td>0</td><td>0</td></tr>
</table>
Ignore the spot distance while defect is in spec.
The distance between two bubble should be larger than 20mm.</td></tr>
<tr><td>12.5</td><td>Mini Electrical Dot Defect</td><td colspan="3">Not accepted under 5% ND filter.</td></tr>
<tr><td>12.6</td><td>Mura (Non-uniformity)</td><td colspan="3">Not accepted under 5% ND filter,but a limits sample will be allowed.</td></tr>
<tr><td rowspan="2">12.7</td><td rowspan="2">FPC</td><td>Broken</td><td colspan="2">Not allowed</td></tr>
<tr><td>Crease</td><td colspan="2">Can't see the white crease</td></tr>
<tr><td rowspan="3">12.8</td><td rowspan="3">Bezel</td><td>Rust</td><td colspan="2" rowspan="3">NG</td></tr>
<tr><td>oil</td></tr>
<tr><td>Broken(Affect the assembly)</td></tr>
<tr><td>12.9</td><td>Chipped glass</td><td colspan="3">Symbols:
a: Chip length b: Chip width c: Chip thickness
t: Glass thickness
1 ITO electrode</td></tr>
</table>

		a<=t b<=0.5mm c<=3.0mm  2 General ,corner portion a<= t b<=1.0mm c<=5.0mm  *Effective width of seal area shall be more than 0.3mm. 
12.10	Cracked glass	The LCD with extensive crack is not acceptable.
12.11	Backlight elements	1 Illumination source flickers when lit. 2 Spots or scratches that appear when lit must be judged using LCD spot, lines and contamination standards. 3 Backlight doesn't light or color is wrong

12.12	Soldering	1 No unmelted solder paste may be present on the PCB. 2 No cold solder joints, missing solder connections, oxidation or icicle. 3 No residue or solder balls on PCB. 4 No short circuits in components on PCB.
12.13	General appearance	1 No oxidation, contamination, curves or, bends on interface pin (OLB) of TCP. 2 No cracks on interface pin(OLB) of TCP 3 NO contamination, solder residue or solder balls on product. 4 The IC on the TCP may not be damaged, circuits. 5 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. 6 Sealant on top of the ITO circuit has not hardened 7 Pin type must match type in specification sheet. 8 LCD pin loose or missing pins. 9 Product packaging must the same as specified on packaging specification sheet. 10 Product dimension and structure must conform to product specification sheet.
12.14	Mura (Non-uniformity)	Not accepted under 5% ND filter,but a limits sample will be allowed.
12.15	Mura (Light Leakage)	Light leakage from identifiable lamp counts, not allowed Remaining light leakage, 2% ND filter masking. Maskable or L≤10mm, not allowed.

		10 <L≤20mm, N≤3. L＞20mm, not allowed

14. Precautions for Operation and Storage

1. Precautions for Operation

(1)Since LCD panel made of glass,in order to prevent from glass broken or color tone change,please do not apply any mechanical shock or impact or excessive force to it when installing the LCD module.

(2)If LCD panel is broken and liquid crystal substance leaks out and contact your skin or clothes,please immediately wash it off by using soap and water.

(3)The polarizer on the LCD surface is soft and easily scratched.Please be careful when handling.

(4)If LCD surface becomes contaminated,please wipe it off gently by using moisten soft cloth with normal hexane,do not use acetone,ketone,ethanol, alcohol or water.If there is saliva or water on the LCD surface,please wipe it off immediately.

(5)When handing LCD module,please be sure that the body and the tools are properly grounded.And do not touch I/F pins with bare hands or contaminate I/F pins.

(6)Do not attempt to disassemble or process the LCD module.

(7)LCD module should be used under recommended operating conditions shown in chapter 6 and 7.

(8)Response time will be extremely slower at lower temperature than at specified temperature and LCD will show different color when at higher temperature.The phenomenon will disappear when returning to specified condition.

(9)Foggy dew,moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage,the deteriorated display quality and electrochemical reaction then leads to the shorter life time and permanent damage to the module probably.Please pay attention to the environmental temperature and humidity.

2. Precautions for Storage

(1)Please store LCD module in a dark place,avoid exposure to sunlight,the light of fluorescent lamp or any ultraviolet ray.

(2)Keep the environment temperature at between 10℃and 35 ℃

and at normal humidity.Avoid high temperature,high humidity or temperature below 0℃.

(3)That keeps the LCD modules stored in the container shipped from supplier before using them is recommended.

(4)Do not leave any article on the LCD module surface for an extended period of time.

3. Warranty period

Warrants for a period of 12 Months from the shipping data when stored or used under normal condition.

15.Package Specification

TBD