# SPECIFICATION

*PRODUCT NO.* : TCXD120IBLON-5610
*VERSION* : V1.0
*ISSUED DATE* : 2020-12-03

**This module uses ROHS material**

**FOR CUSTOMER：**

□：APPROVAL FOR SPECIFICATION
■：APPROVAL FOR SAMPLE

| DATE | APPROVED BY |
|---|---|
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Note:

1.Xinli Optoelectronics reserves the right to make changes without further notice to any products herein to improve reliability, function or design.

# 1. Revision Recode

| Revision | Description | Date |
|---|---|---|
| 1.0 | InitialRelease | 2020/12/03 |
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# 1.0 General Descriptions

## 1.1 Introduction

The TCXD120IBLON-5610 is a Color Active Matrix Liquid Crystal Display with a back light system. The matrix uses a-Si Thin Film Transistor as a switching device. This TFT LCD has a 12.0 inch diagonally measured active display area with WUXGA+ resolution (2,160horizontal by 1,440 vertical pixels array).

## 1.2 Features

- Supported WUXGA+ resolution
- eDP1.3 Interface
- Wide View Angle
- Compatible with RoHS Standard

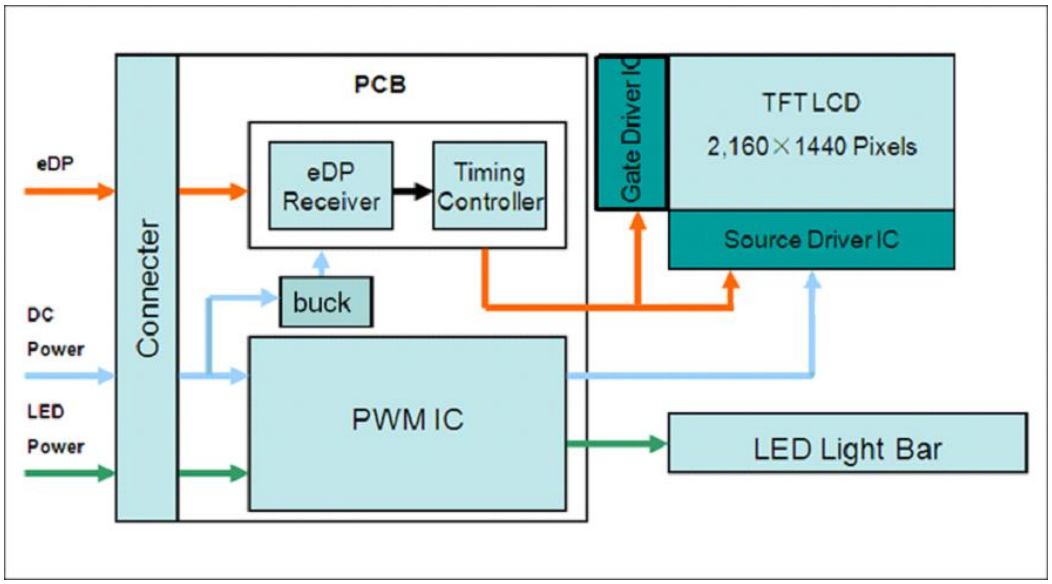
## 1.3 Product Summary

| Items | | Specifications | Unit |
|---|---|---|---|
| Screen Diagonal | | 12.0 | inch |
| Active Area (H x V) | | 254.02 x 169.34 | mm |
| Number of Pixels (H x V) | | 2,160 x 1,440 | - |
| Pixel Pitch (H x V) | | (0.1176) x (0.1176) | mm |
| Pixel Arrangement | | RGB Vertical Stripe | - |
| Display Mode | | Normally Black | - |
| White Luminance | | (400) (Typ.) | cd /m$^2$ |
| Contrast Ratio | | (1,000) (Typ.) | - |
| Response Time | | (30) (Typ.) | ms |
| Input Voltage | | (3.3) (Typ.) | V |
| Power Consumption | | (3.78) (Max.) @ Mosaic Pattern | W |
| Weight | | (175) (Max.) | g |
| Outline Dimension (H x V x D) | Without PCB | (263.12) (Typ.) x (181.91)(Typ.) x (2.15) (Max.) | mm |
| | With PCB | (263.12) (Typ.) x (181.91)(Typ.) x (4.4) (Max.) | |
| Electrical Interface (Logic) | | eDP 1.3 | - |
| Support Color | | 16.7 M | - |
| NTSC | | (69.6) (Typ.) | % |
| Viewing Direction | | All | - |
| Surface Treatment | | Glare，3H | - |

## 1.4 Functional Block Diagram

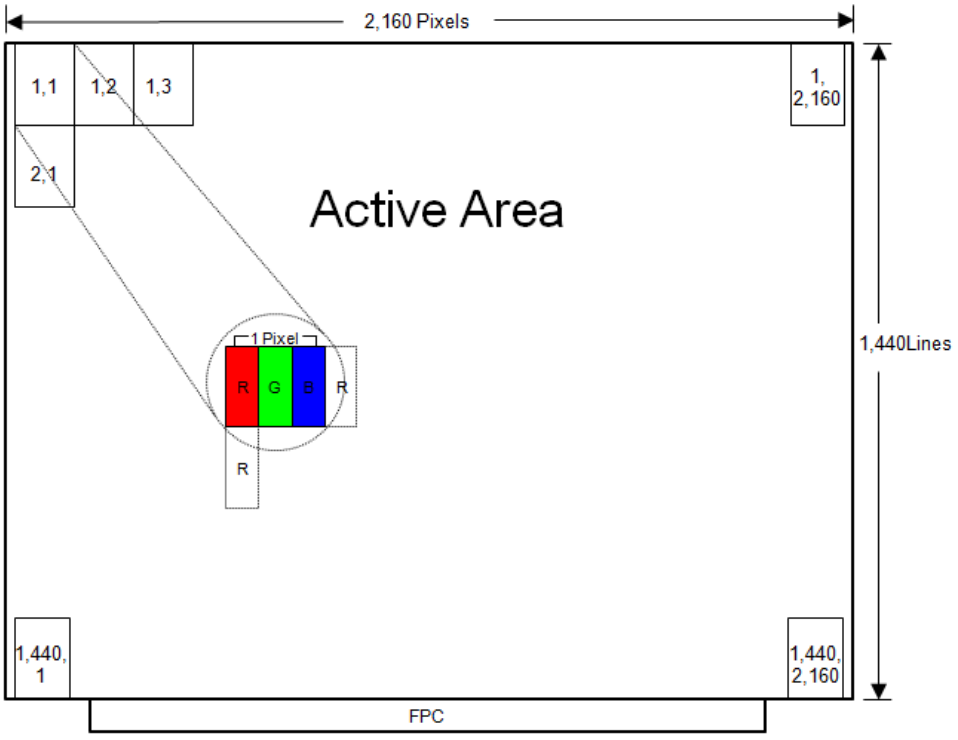
Figure 1 shows the functional block diagram of the LCD module.

**Figure 1 Block Diagram**




## 1.5 Pixel Mapping

**Figure 2 Pixel Mapping**



## 2.0 Absolute Maximum Ratings

**Table 1 Electrical & Environment Absolute Rating**

| Item | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Logic Supply Voltage | $V_{DD}$ | (-0.3) | (3.63) | V | (1)(2)(3)(4) |
| Logic Input Signal Voltage | $V_{Signal}$ | (-0.3) | (3.63) | V | |
| Operating Temperature | $T_{gs}$ | (0) | (50) | ℃ | |
| Storage Temperature | $T_a$ | (-20) | (60) | ℃ | |

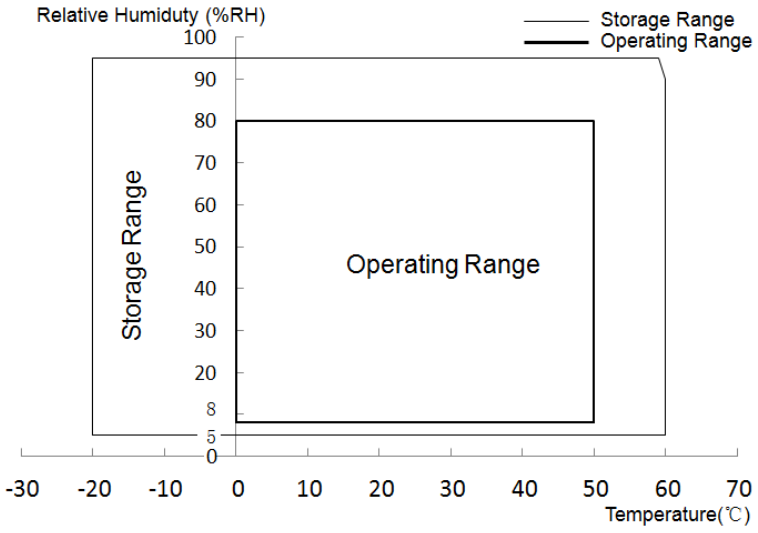
Note(1) All the parameters specified in the table are absolute maximum rating values that may cause faulty operation or unrecoverable damage, if exceeded. It is recommended to follow the typical value.

Note(2) All the contents of electro-optical specifications and display fineness are guaranteed under Normal Conditions. All the display fineness should be inspected under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH.

Note(3) Unpredictable results may occur when it was used in extreme conditions. Ta= Ambient Temperature, $T_{gs}$= Glass Surface Temperature. All the display fineness should be inspected under normal conditions.

Note(4) Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be lower than 46℃, and no condensation of water. Besides, protect the module from static electricity.

**Figure 3 Absolute Ratings of Environment of the LCD Module**



## 3.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

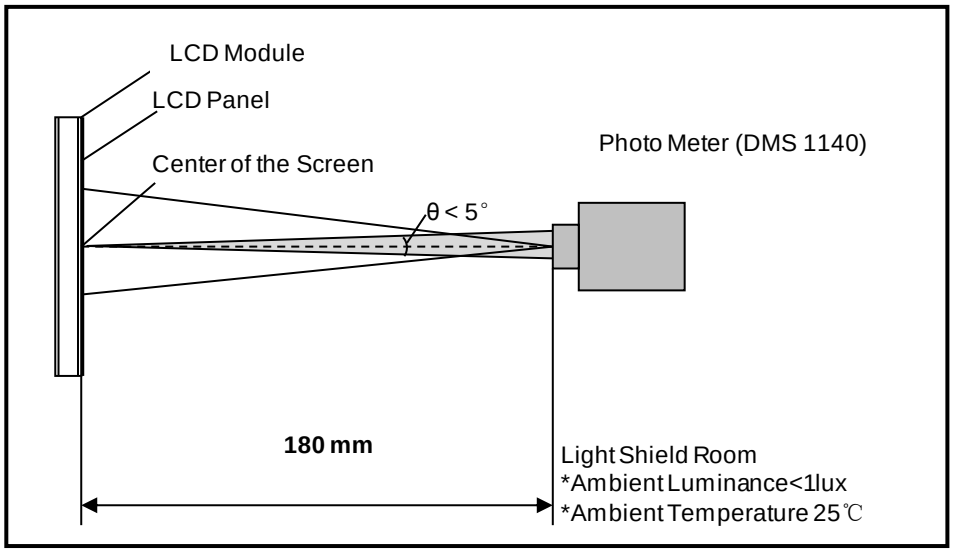
**Table 2 Optical Characteristics**

| Item | Conditions | | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| Viewing Angle （CR≥10） | Horizontal | $\theta_{x+}$ | (75) | (85) | - | degree | (1),(2),(3),(4),(8) |
| | | $\theta_{x-}$ | (75) | (85) | - | | |
| | Vertical | $\theta_{y+}$ | (75) | (85) | - | | |
| | | $\theta_{y-}$ | (75) | (85) | - | | |
| Contrast Ratio | Center | | (800) | (1,000) | - | - | (1),(2),(4),(8) θx=θy=0° |
| Response Time | Rising + Falling | | - | (30) | (35) | ms | (1),(2),(5),(8) θx=θy=0° |
| Color Chromaticity (CIE1931) | Red x | | Typ. (-0.03) | (0.640) | Typ. (+0.03) | - | (1),(2),(3),(8) θx=θy=0° |
| | Red y | | | (0.336) | | - | |
| | Green x | | | (0.317) | | - | |
| | Green y | | | (0.603) | | - | |
| | Blue x | | | (0.153) | | - | |
| | Blue y | | | (0.058) | | - | |
| | White x | | | (0.313) | | - | |
| | White y | | | (0.329) | | - | |
| NTSC | - | | (63) | (69.6) | - | % | (1),(2),(3),(8) θx=θy=0° |
| White Luminance | 5 Points Average | | (340) | (400) | (460) | $cd/m^2$ | (1),(2),(6),(8) θx=θy=0° |
| Luminance Uniformity | 5 Points | | (80) | - | - | % | (1),(2),(7),(8) θx=θy=0° |
| | 13 Points | | (60) | - | - | | |

Note(1) Measurement Setup:

The LCD module should be stabilized at given ambient temperature (25℃) for 30 minutes to avoid abrupt temperature changing during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 30 minutes in the windless room.

**Figure 4 Measurement Setup**



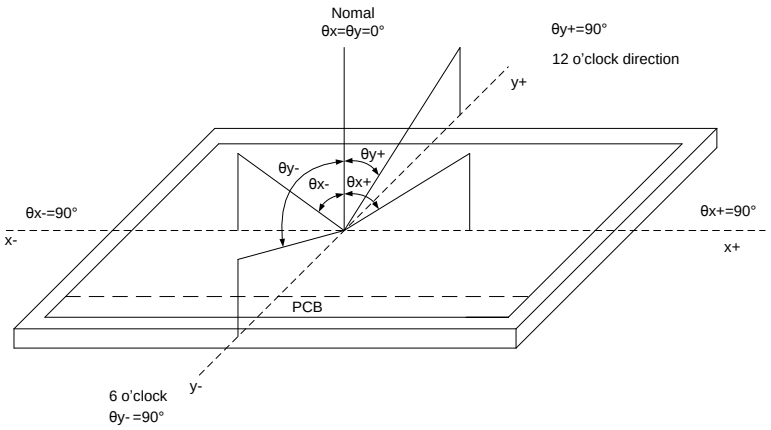

Note(2) The LED input parameter setting as:

V_LED: (12)V

PWM_LED: Duty 100 %

Note(3) Definition of Viewing Angle

**Figure 5 Definition of Viewing Angle**




Note(4) Definition of Contrast Ratio (CR)

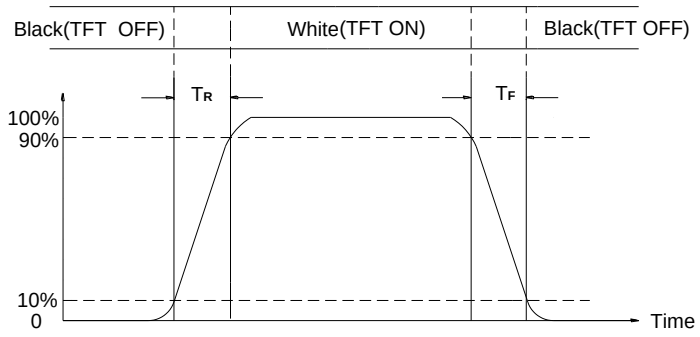
The contrast ratio can be calculated by the following expression:

Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255, L0: Luminance of gray level 0

Note(5) Definition of Response Time ($T_R$, $T_F$)

**Figure 6 Definition of Response Time**



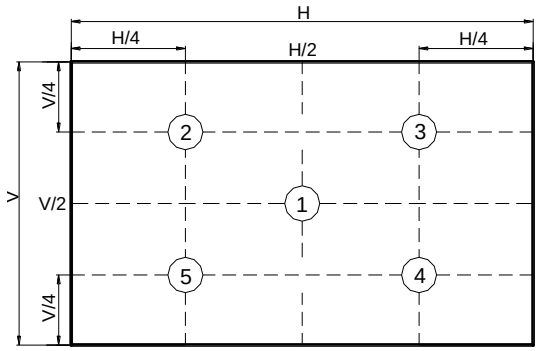

Note(6) Definition of Luminance White

Measure the luminance of gray level 255 (Ref.: Active Area)

Display Luminance=(L1+L2+L3+L4+L5) / 5

H—Active Area Width, V—Active Area Height, L—Luminance

**Figure 7 Measurement Locations of 5 Points**




Note(7) Definition of Luminance Uniformity (Ref.: Active Area)

Measure the luminance of gray level 255 at 5 points.

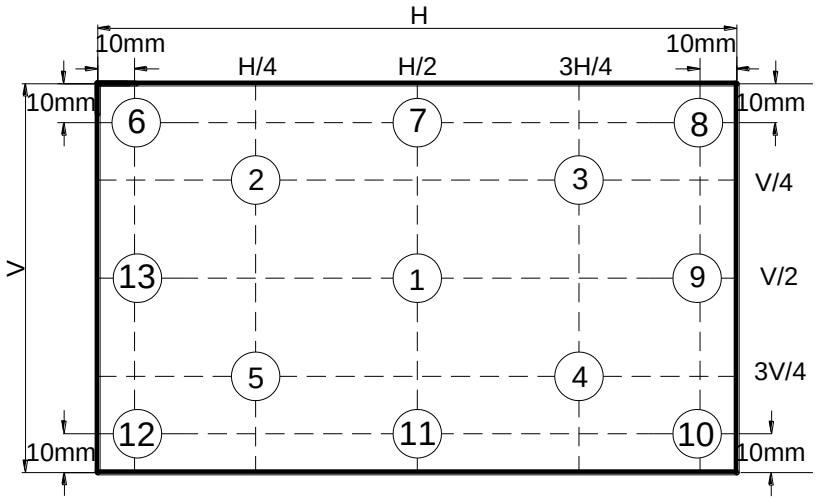
Luminance Uniformity= Min.(L1, L2, ... L5) / Max.(L1, L2, ... L5)

Measure the luminance of gray level 255 at 13 points.

Luminance Uniformity= Min.(L1, L2, ... L13) / Max.(L1, L2, ... L13)

H—Active Area Width, V—Active Area Height, L—Luminance

**Figure 8 Measurement Locations of 13 Points**




Note(8) All optical data are based on XL given system & nominal parameter & testing machine in this document.

# 4.0 Electrical Characteristics

## 4.1 Interface Connector

**Table 3 Signal Connector Type**

| Item | Description |
|---|---|
| Manufacturer / Type | IPEX / 20455-040E-66 |

**Table 4 Signal Connector Pin Assignment**

| Pin No. | Symbol | Description | Remarks |
|---|---|---|---|
| 1 | VBL | LED Power supply | - |
| 2 | VBL | LED Power supply | - |
| 3 | VBL | LED Power supply | - |
| 4 | VBL | LED Power supply | - |
| 5 | NC | No Connection | - |
| 6 | H-Sync | Horizontal SYNC signal | - |
| 7 | PWM | PWM signal For LED Driver | - |
| 8 | BL_EN | EN signal For LED Driver | - |
| 9 | GND | Ground | - |
| 10 | GND | Ground | - |
| 11 | GND | Ground | - |
| 12 | GND | Ground | - |
| 13 | HDP | HPD signal pin | - |
| 14 | GND | Ground | - |
| 15 | GND | Ground | - |
| 16 | GND | Ground | - |
| 17 | GND | Ground | - |
| 18 | GND | Ground | - |
| 19 | GND | Ground | - |
| 20 | VCC | LCD logic Power | - |
| 21 | VCC | LCD logic Power | - |
| 22 | VCC | LCD logic Power | - |
| 23 | VCC | LCD logic Power | - |
| 24 | BIST | BIST enable, Active High 3.3V，normal pull low | - |
| 25 | GND | Ground | - |
| 26 | DAUXN | Complement Signal Auxiliary Channel | - |
| 27 | DAUXP | True Signal Auxiliary Channel | - |
| 28 | GND | Ground | - |
| 29 | DRX0P | True Signal Link Lane 0 | - |

| | | | |
|---|---|---|---|
| 30 | DRX0N | Complement Signal Link Lane 0 | - |
| 31 | GND | Ground | - |
| 32 | DRX1P | True Signal Link Lane 1 | - |
| 33 | DRX1N | Complement Signal Link Lane 1 | - |
| 34 | GND | Ground | - |
| 35 | DRX2P | True Signal Link Lane 2 | - |
| 36 | DRX2N | Complement Signal Link Lane 2 | - |
| 37 | GND | Ground | - |
| 38 | DRX3P | True Signal Link Lane 3 | - |
| 39 | DRX3N | Complement Signal Link Lane 3 | - |
| 40 | GND | Ground | - |

## 4.2 Signal Electrical Characteristics

**Table 5 Display Port Main Link**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CM}$ | Differentia Common Mode Voltage | 0 | - | 2.0 | V |
| $V_{Diff\ P-P}$ Level 1 | Differential Peak to Peak Voltage Level 1 | 0.1 | 0.40 | 0.46 | V |
| $V_{Diff\ P-P}$ Level 2 | Differential Peak to Peak Voltage Level 2 | 0.51 | 0.60 | 0.68 | V |
| $V_{Diff\ P-P}$ Level 3 | Differential Peak to Peak Voltage Level 3 | 0.69 | 0.80 | 0.92 | V |
| $V_{Diff\ P-P}$ Level 4 | Differential Peak to Peak Voltage Level 4 | 1.02 | 1.20 | 1.38 | V |

Note: (1) Input signals shall be low or Hi- resistance state when VDD is off.

(2) It is recommended to refer the specifications of VESA Display Port Standard V1.3 in detail.

(3) Follow as VESA display port standard V1.3 at 2.7Gbps link rates.

**Figure 9 Display Port Main Link Signal**

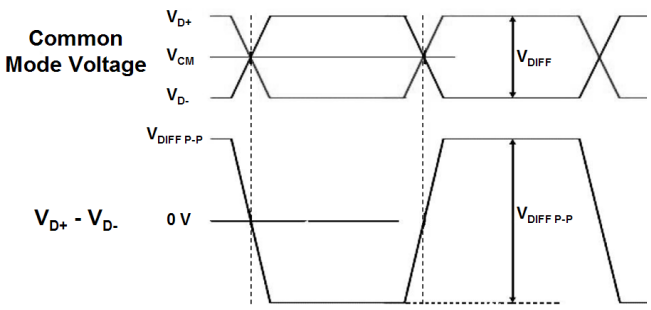



**Figure 10 Display Port AUX_CH Signal**

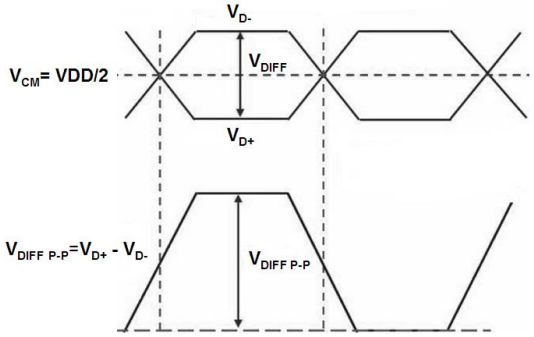



**Table 6 Display Port AUX_CH**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CM}$ | Differentia Common Mode Voltage | 0 | VDD/2 | 2 | V |
| $V_{Diff\ P-P}$ | Differential Peak to Peak Voltage | 0.39 | - | 1.38 | V |

Note: Follow as VESA display port standard V1.3.

**Table 7 Display Port VHPD**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{HPD}$ | HPD Voltage | 2.25 | - | 3.60 | V |

Note: Follow as VESA display port standard V1.3.

### 4.3 Interface Timings

**Table 8 Interface Timings**

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Clock Frequency | Fclk | TBD | (230.4) | TBD | MHz |
| H Total Time | HT | TBD | (2,240) | TBD | Clocks |
| H Active Time | HA | | 2,160 | | Clocks |
| V Total Time | VT | TBD | (1,472) | TBD | Lines |
| V Active Time | VA | | 1,440 | | Lines |
| Frame Rate | FV | (55) | (60) | (65) | Hz |

### 4.4 Input Power Specification0073

Input power specifications are as follows.

**Table 9 Input Power Specifications**

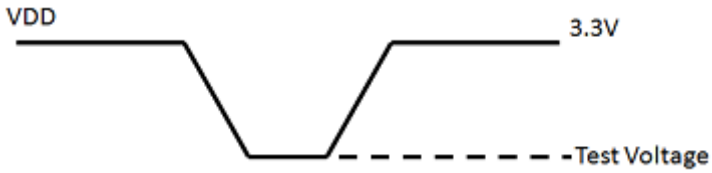
| Parameter | | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| *System Power Supply* | | | | | | | |
| LCD Drive Voltage (Logic) | | $V_{DD}$ | (3.0) | (3.3) | (3.6) | V | (1),(2),(3) |
| VDD Current | Mosaic Pattern | $I_{DD}$ | - | - | (0.27) | A | (1),(4) |
| VDD Power Consumption | Mosaic Pattern | $P_{DD}$ | - | - | (0.9) | W | |
| Rush Current | | $I_{Rush}$ | - | - | (1.5) | A | (1),(5) |
| Allowable Logic/LCD Drive Ripple Voltage | | $V_{VDD-RP}$ | - | - | (200) | mV | (1) |
| *LED Power Supply* | | | | | | | |
| LED Input Voltage | | $V_{LED}$ | (5) | (12) | (21) | V | (1),(2) |
| LED Power Consumption | | $P_{LED}$ | - | (2.6) | (2.88) | W | (1),(6) |
| LED Forward Voltage | | $V_F$ | - | - | (2.9) | V | (1),(2) |
| LED Forward Current | | $I_F$ | - | (18.5) | - | mA | |
| PWM Signal Voltage | High | $V_{PWM}$ | (2.2) | - | (3.6) | V | |
| | Low | | - | - | (0.6) | | |
| LED Enable Voltage | High | $V_{LED\_EN}$ | (2.2) | - | (3.6) | V | |
| | Low | | - | - | (0.6) | | |
| Input PWM Frequency | | $F_{PWM}$ | (0.1) | - | (30) | KHz | (1),(2),(7) |
| Duty Ratio | | PWM | (1) | - | (100) | % | (1),(8) |
| LED Life Time | | LT | (15,000) | - | - | Hours | (1),(9) |

Note(1) All of the specifications are guaranteed under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH.

Note(2) All of the absolute maximum ratings specified in the table, if exceeded, may cause faulty operation or unrecoverable damage. It is recommended to follow the typical value.

Note(3) VDD Power Dip Condition for Lenovo

**Figure 11 VDD Power Dip**



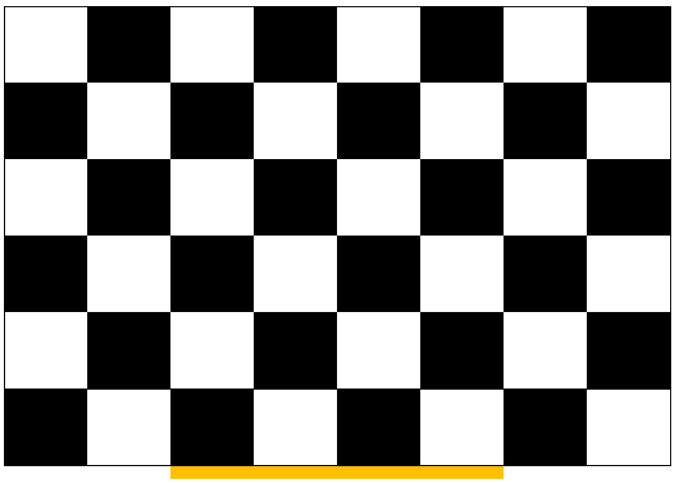

Test criteria:

1) 2.4V≤Test Voltage≤3.3V :Normal operation

2) 2.0V≤Test Voltage＜2.4V: No abnormal display after back to 3.3V input.

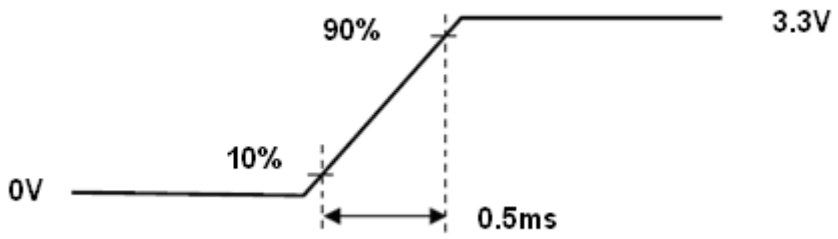
Note(4) The specified VDD current and power consumption are measured under the VDD = 3.3 V, FV = 60 Hz condition and Mosaic pattern.

**Figure 12 Mosaic pattern**



Note(5) The figures below is the measuring condition of VDD. Rush current can be measured when $T_{RUSH}$ is 0.5 ms.

**Figure 13 VDD Rising Time**




Note(6) The power consumption of LED Driver are under the VLED = 12.0V, Dimming of Max luminance.

Note(7) Although acceptable range as defined, the dimming ratio is not effective at all conditions. The PWM frequency should be fixed and stable for more consistent luminance control at any specific level desired.

Note(8) The operation of LED Driver below minimum dimming ratio may cause flickering or reliability issue.

Note(9) The life time is determined as the sum of the lighting time till the luminance of LCD at the typical LED current reducing to 50% of the minimum value under normal operating condition.

### 4.5 Power ON/OFF Sequence

Interface signals are also shown in the chart. Signals from any system shall be Hi-resistance state or low level when VDD voltage is off.

**Figure 14 Power Sequence**

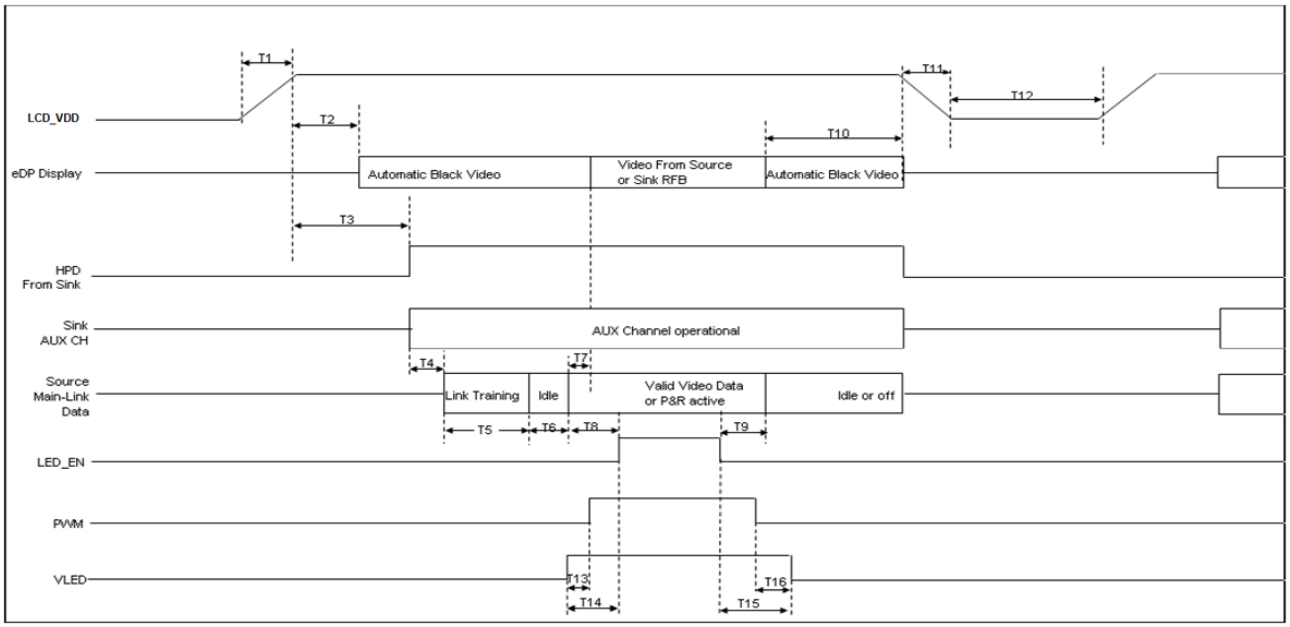



**Table 10 Power Sequencing Requirements**

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VDD Rise Time (10% to 90%) | T1 | (0.5) | - | (10) | ms |
| Delay from VDD to automatic Black Video generation | T2 | (0) | - | (200) | ms |
| Delay from VDD to HPD high | T3 | (0) | - | (200) | ms |
| Delay from HPD high to link training initialization | T4 | - | - | - | ms |
| Link training duration | T5 | - | - | - | ms |
| Link idle | T6 | - | - | - | ms |
| Delay from valid video data from Source to video on display | T7 | (0) | - | (50) | ms |
| Delay from valid video data from Source to backlight enable | T8 | (200) | - | - | ms |
| Delay from backlight disable to end of valid video date | T9 | - | - | - | ms |
| Delay from end of valid video data from Source to VDD off | T10 | (0) | - | (500) | ms |
| VDD fall time (90% to 10%) | T11 | (0) | - | (10) | ms |
| VDD off time | T12 | (500) | - | - | ms |
| Delay from VLED to PWM | T13 | (0) | - | - | ms |
| Delay from VLED to backlight enable | T14 | (0) | - | - | ms |
| Delay from backlight disable to VLED off | T15 | (0) | - | - | ms |
| Delay from PWM off to VLED off | T16 | (0) | - | - | ms |

# 5.0 Mechanical Characteristics

## 5.1 Outline Drawing

**Figure 15 Reference Outline Drawing (Front Side)**

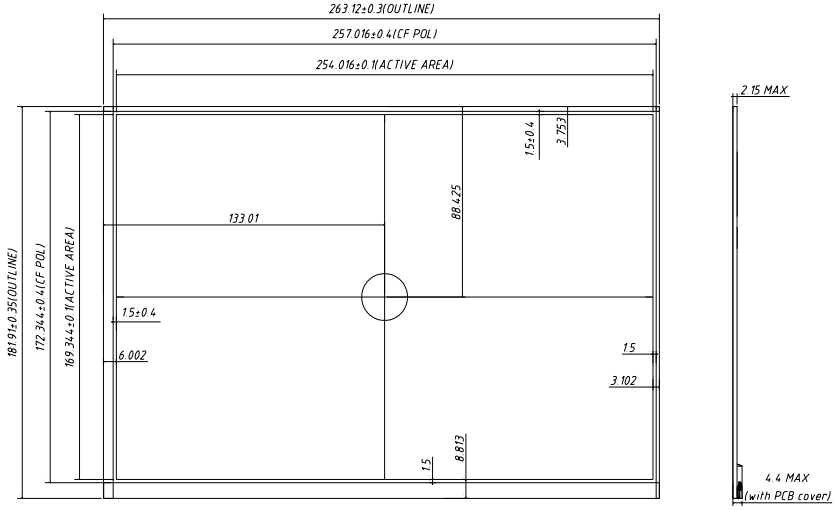
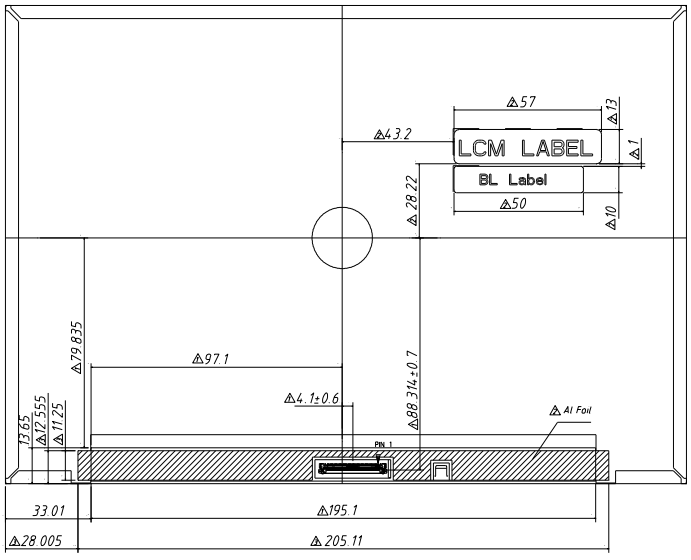
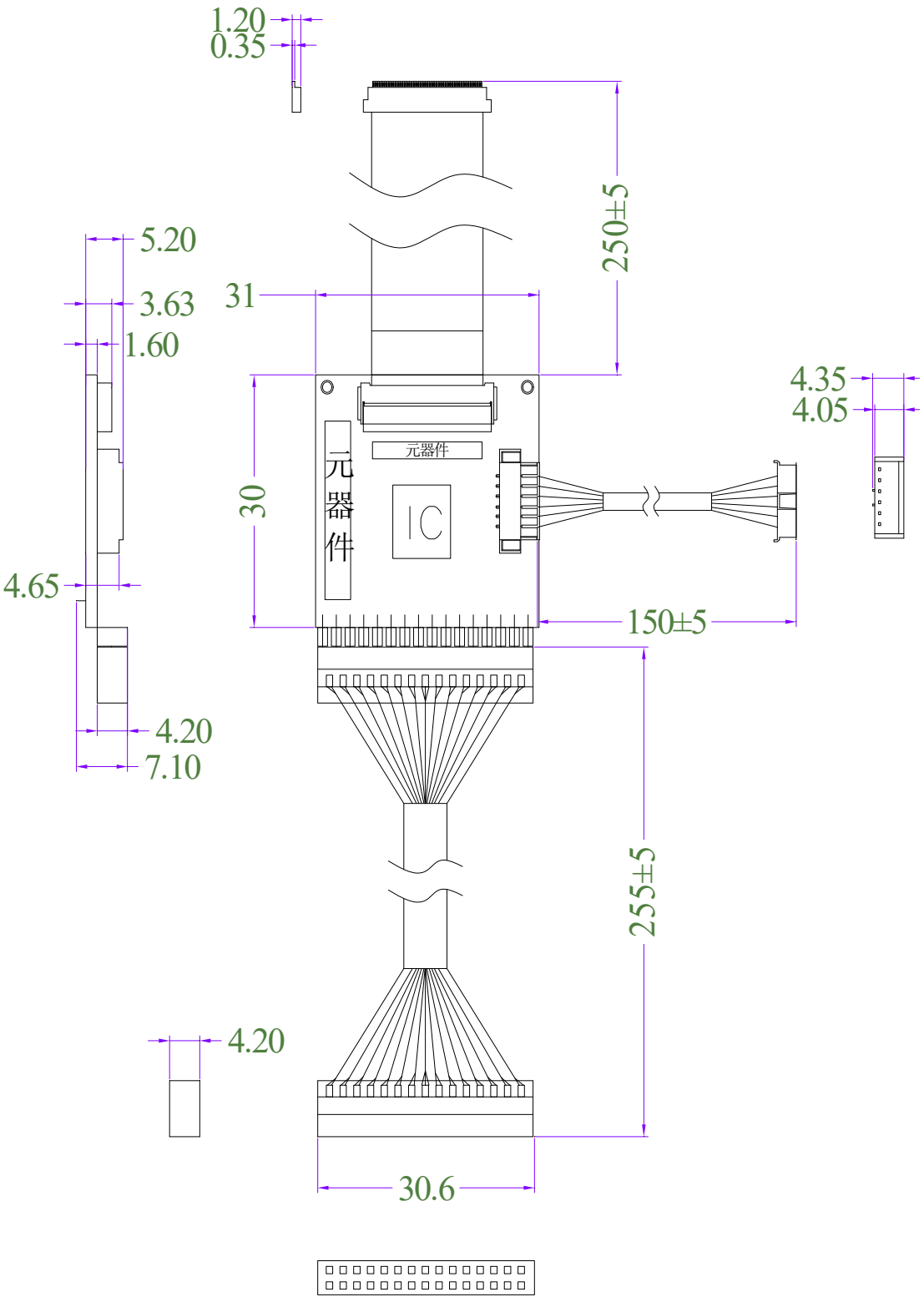



**Figure 16 Reference Outline Drawing (Back Side)**



# LVDS adapter board, for reference



**Dimension Specifications**

**Table 11 Module Dimension Specifications**

| Item | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Width | | (262.82) | (263.12) | (263.42) | mm |
| Height | | (181.56) | (181.91) | (182.26) | mm |
| Thickness | Without PCBA | - | - | (2.15) | mm |
| | With PCBA | - | - | (4.40) | mm |
| Weight | | - | - | (175) | g |

## 6.0 Reliability Conditions

**Table 12 Reliability Condition**

| Item | Package | Test Conditions | | Note |
|---|---|---|---|---|
| High Temperature/High Humidity Operating Test | Module | $T_{gs}$=50℃, 80%RH, 1000 hours | | (1),(2),(3), (4) |
| Low Temperature Operating Test | Module | $T_{gs}$=0℃, 500 hours | | |
| High Temperature/High Humidity Storage Test | Module | $T_a$=60℃, 90%RH, 300 hours | | (1),(2),(3) |
| Low Temperature Storage Test | Module | $T_a$=-20℃, 240 hours | | |
| Storage Temp/Hum Test | Module | -20~60℃,20%~95%,2cycle,48hours/cycle | | |
| Shock Non-operating Test | Module | 50G 18 msec Trapezoidal ±x, ±y, ±z each aixs/1times<br>210G 3msec half-sine ±x,±y,±z each aixs/1times | | (1),(3),(5) |
| Vibration Non-operating Test | Module | 1.5G,10Hz~200Hz, x、y、z each aixs. /30min | | |
| ESD Test(Operating) | Module | Contact | ±8KV, 150pF(330Ohm) | (1),(2),(6) |
| | | Air | ±15KV, 150pF(330Ohm) | |

Note(1) A sample can only have one test. Outward appearance, image quality and optical data can only be checked at normal conditions according to the XL document before reliable test. Only check the function of the module after reliability test.

Note(2) The setting of electrical parameters should follow the typical value before reliability test.

Note(3) During the test, it is unaccepted to have condensate water remains. Besides, protect the module from static electricity.

Note(4) The sample must be released for 24 hours under normal conditions before judging. Furthermore, all the judgment must be made under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH. Ta= Ambient Temperature, Tgs= Glass Surface Temperature.

Note(5) The module should be fixed firmly in order to avoid twisting and bending.

Note(6) It could be regarded as pass, when the module recovers from function fault caused by ESD after resetting.

## 7.0 Package Specification

**TBD**