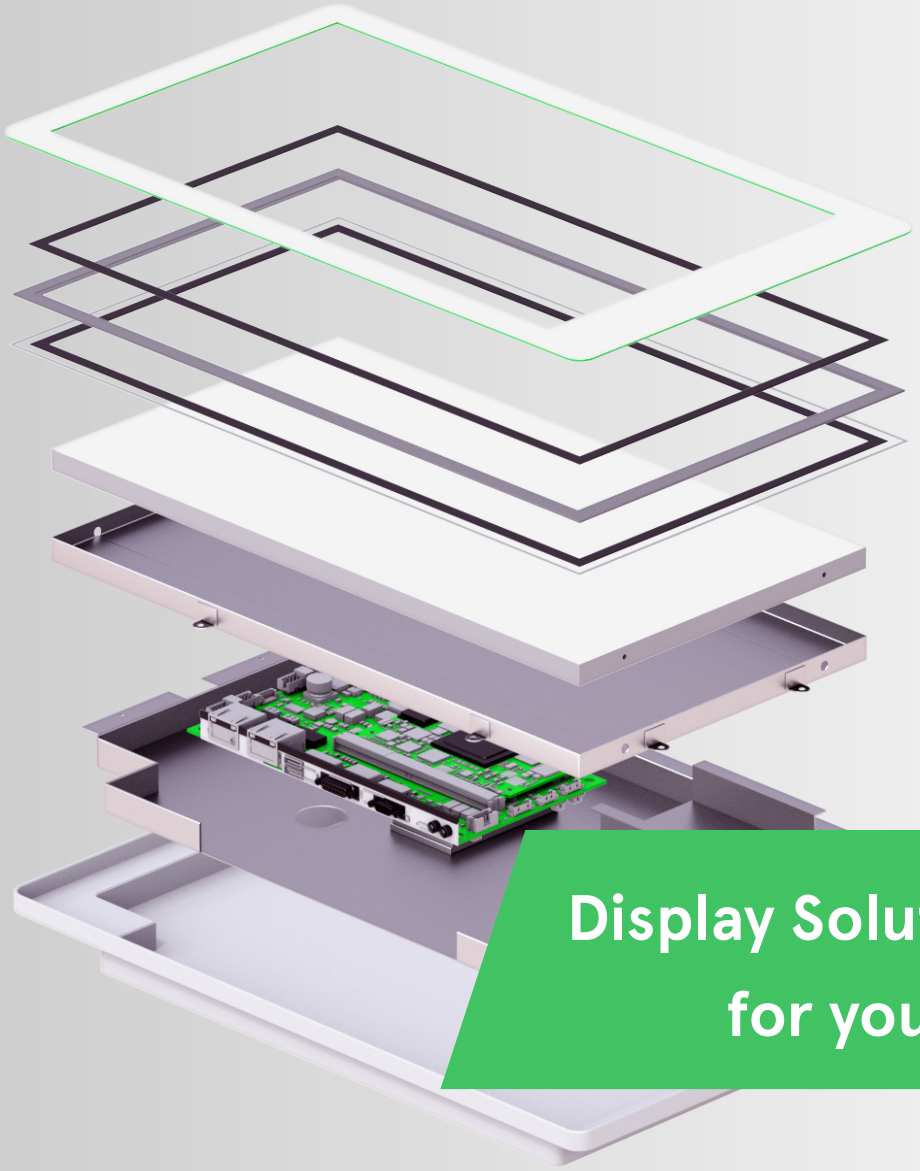
AVNET EMBEDDED



Display Solutions tailored for your Application

DATASHEET

TX31D208VM0BAB

TENTATIVE

KOE

JDI Group

Kaohsiung Opto-Electronics Inc.

FOR MESSRS : _____ DATE : Mar. 15th,2021

TECHNICAL DATA

TX31D208VM0BAB

Contents

ACCEPTED BY: _____

PROPOSED BY: Oblack Tsai

2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 12.1” WXGA format amorphous silicon TFT. The pixel format is vertical stripe and sub pixels are arranged as R(red), G(green), B(blue) sequentially. This display is RoHS compliant, and COG (chip on glass) technology and LED backlight are applied on this display.

Part Name	TX31D208VM0BAB
Module Dimensions	283.0(W) mm × 185.1 (H) mm × 9.7 (D) mm (max)
LCD Active Area	261.12(W)mm x 163.2(H)mm
Pixel Pitch	0.204 (W) mm × 0.204 (H) mm
Resolution	1280× 3 (RGB) (W) × 800 (H) dots
Color Pixel Arrangement	RGB Vertical Stripe
LCD Type	Normally Black
Display Type	Active Matrix
Number of Colors	262k(6 bit/color), 16.7M(8 bit/color)
Backlight	Light Emitting Diode (LED)
Weight	516g(typ)
Interface	LVDS (20 pins)
Power Supply Voltage	3.3V for LCD；30V for Backlight
Viewing Direction	Super Wide Version (In Plane switching)

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	4.0	V	-
Input Voltage of Logic	V_I	-0.3	V_{DD}	V	Note 1
Operating Temperature	Top	-40	80	˚C	Note 2
Storage Temperature	Tst	-40	80	˚C	Note 2
LED Forward Current	I_F	-	200	mA	-

Note 1: The rating is defined for the signal voltages of the interface such as CLK and pixel data pairs.

Note 2: The maximum rating is defined as above based on the panel surface temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25 .
- Operating under high temperature will shorten LED lifetime.

5. ELECTRICAL CHARACTERISTICS

5.1 LCD CHARACTERISTICS

$T_a = 25\,^{\circ}C,\ V_{SS} = 0V$

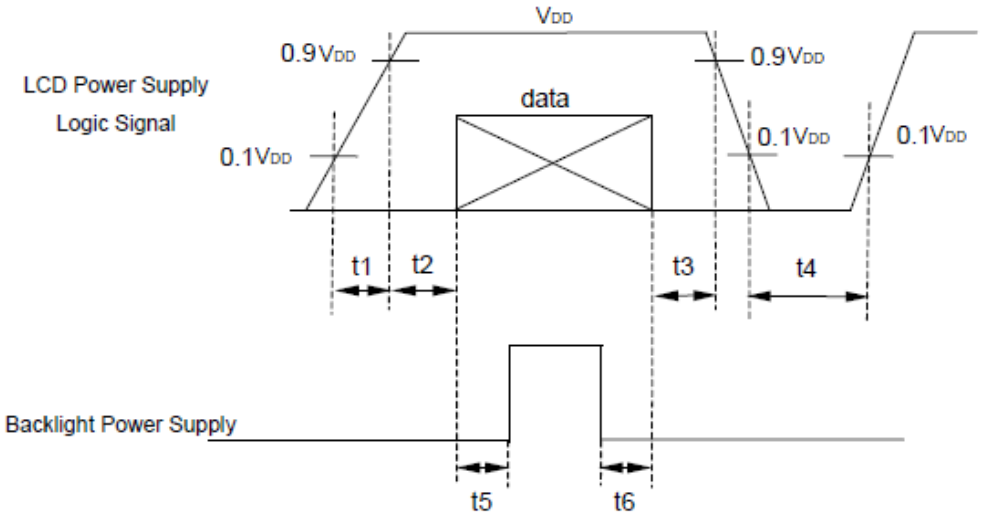
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-	3.0	3.3	3.6	V	Note 1
Differential Input Voltage for LVDS Receiver Threshold	V_I	"H" level	-	-	+200	mV	Note 2
		"L" level	-200	-	-		
Power Supply Current	I_{DD}	V_{DD}=3.3V	-	150	250	mA	Note 3
Frame Frequency	f_{Frame}	-	55	60	65	Hz	-
CLK Frequency	f_{CLK}	-	66	67	71	MHz	

Note 1: Power and signals sequence:

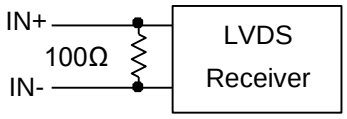
0.1ms ≤ t1 ≤ 10ms 500ms ≤ t4

0 < t2 ≤ 50ms 200ms ≤ t5

0 < t3 ≤ 50ms 0 ≤ t6



Note 2: VCM 1.2V is common mode voltage of LVDS transmitter and receiver. The input terminal of LVDS receiver is terminated with 100Ω.



Note 3: An all white check pattern is used when measuring I_{DD}. f_{Frame} is set to 60Hz. Moreover, 2A fuse is applied in the module for I_{DD}. For display activation and protection purpose, power supply is recommended larger than 5A to start the display and break fuse once any short circuit occurred.

5.2 BACKLIGHT CHARACTERISTICS

$T_a = 25\ ^\circ C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	V_{LED}	I_{LED}=95mA	-	30	34.6	V	Note 1
LED Forward Current (per serial)	I_{LED}	-	-	95	110	mA	
LED Lifetime	-	I_{LED}=95mA	-	100K	-	hrs	Note 2

Note 1: Fig. 5.1 shows the LED backlight circuit.

Note 2: The LED lifetime is estimated and defined as the time when brightness become 50% of the initial value.

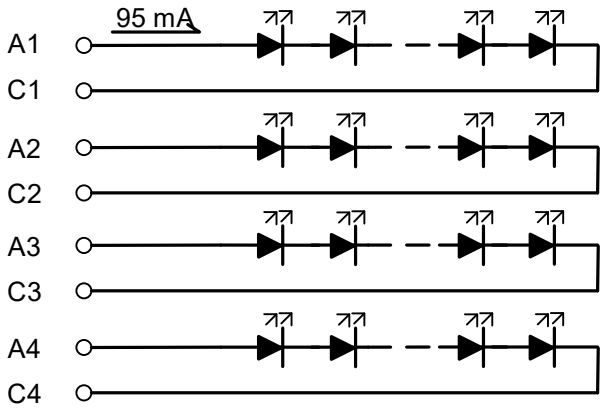


Fig 5.1

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The ambient temperature is 25°C.
- In the dark room less than 100 lx, the equipment has been set for the measurements as shown in Fig 6.1.

$T_a = 25\ ^{\circ}C$, $f_{Frame} = 60$ Hz, $V_{DD} = 3.3$V

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$	1200	1500	-	cd/m^2	Note 1
Brightness Uniformity		-		70	-	-	%	Note 2
Contrast Ratio		CR		650	1000	-	-	Note 3
Response Time		Tr + Tf	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	25	30	ms	Note 4
NTSC Ratio		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	70	-	%	-
Viewing Angle		θ x	$\phi = 0^{\circ}, CR \geq 10$	70	88	-	Degree	Note 5
		θ x′	$\phi = 180^{\circ}, CR \geq 10$	70	88	-		
		θ y	$\phi = 90^{\circ}, CR \geq 10$	70	88	-		
		θ y′	$\phi = 270^{\circ}, CR \geq 10$	70	88	-		
Color Chromaticity	Red	X	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	(0.649)	-	-	Note 6
		Y		-	(0.344)	-		
	Green	X		-	(0.309)	-		
		Y		-	(0.620)	-		
	Blue	X		-	(0.146)	-		
		Y		-	(0.092)	-		
	White	X		-	(0.313)	-		
		Y		-	(0.329)	-		

Note 1: The brightness is measured from the center point of the panel, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \text{ X100\%}$$

which is based on the brightness values of the 9 points measured by CS2000 as shown in Fig. 6.2.

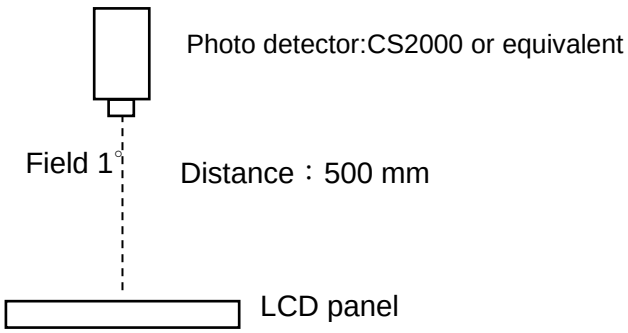


Fig. 6.1

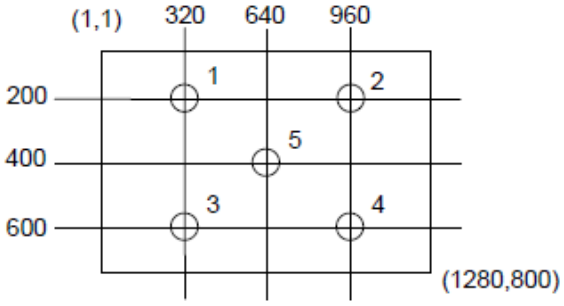


Fig. 6.2

Note 3: The Contrast ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 4: The definition of response time is shown in Fig. 6.3. The rising time is the period from 10% brightness to 90% brightness when the data is from black to white. Oppositely, falling time is the period from 90% brightness rising to 10% brightness.

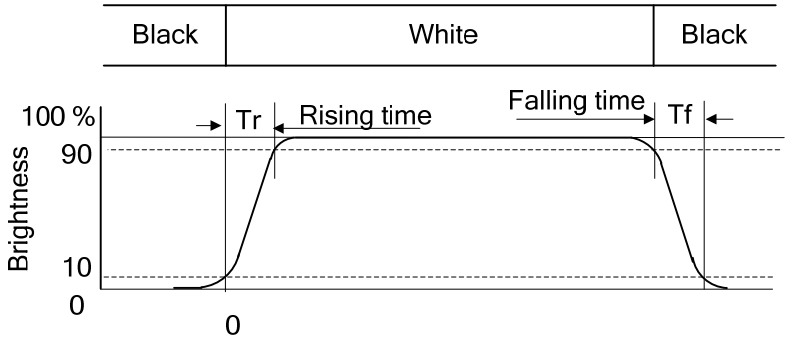


Fig. 6.3

Note 5: The definition of viewing angle is shown in Fig. 6.4. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^\circ$ means 6 o'clock, and $\phi = 0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

The display is super wide viewing angle version, so that the best optical performance can be obtained from every viewing direction.

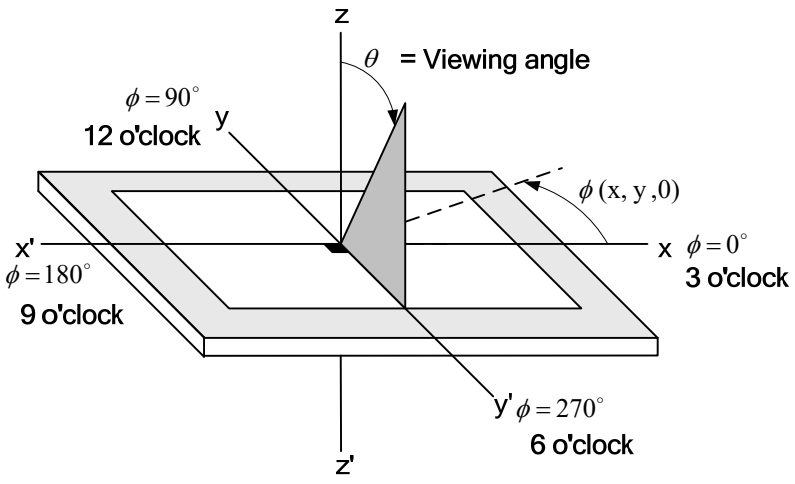
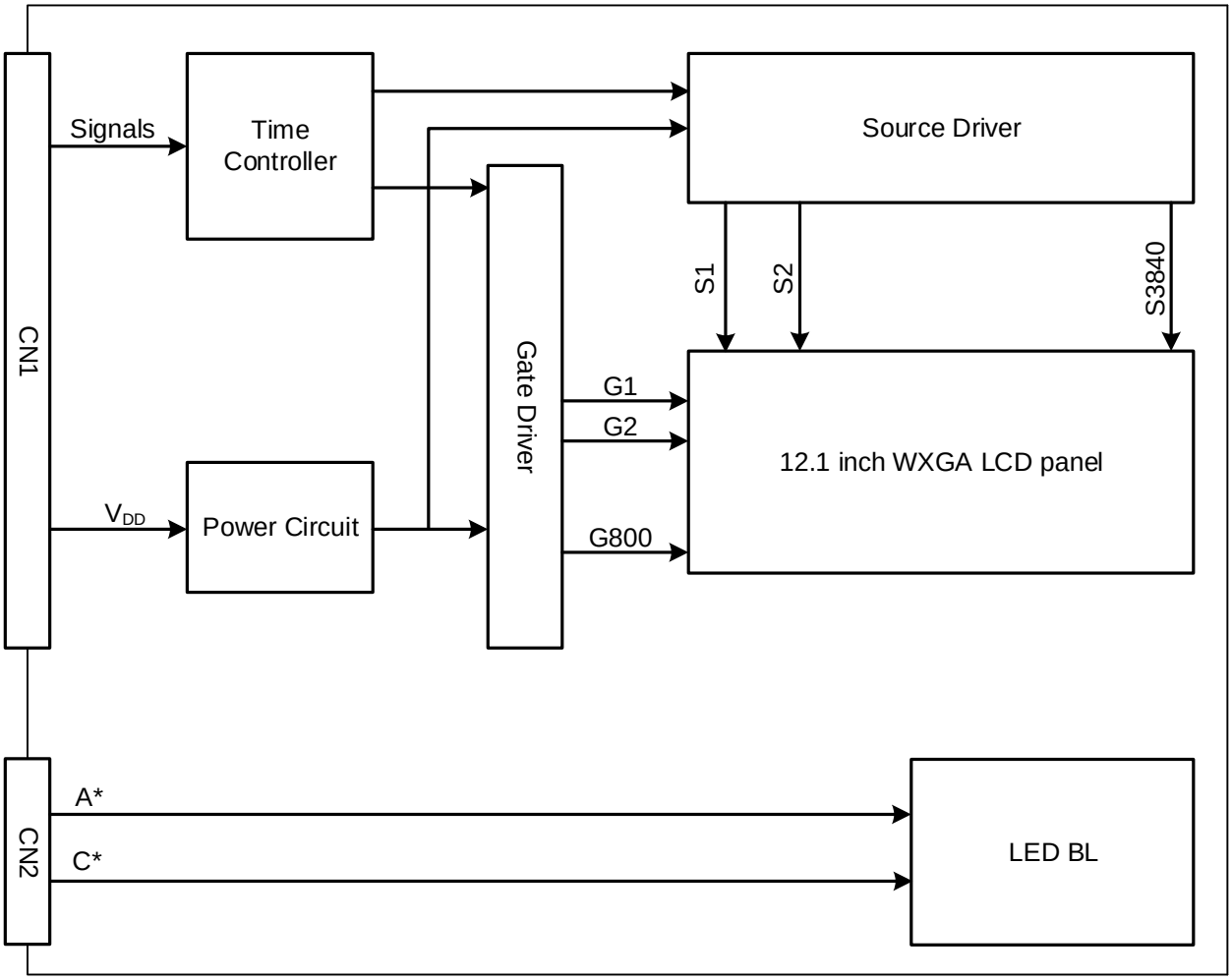


Fig. 6.4

Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

7. BLOCK DIAGRAM



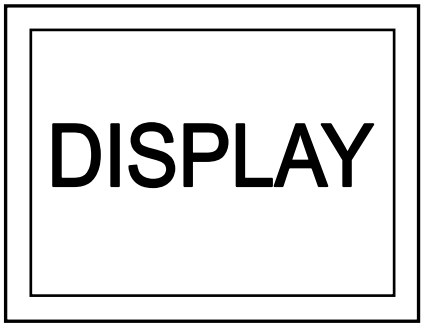
8. LCD INTERFACE

8.1 INTERFACE PIN CONNECTIONS

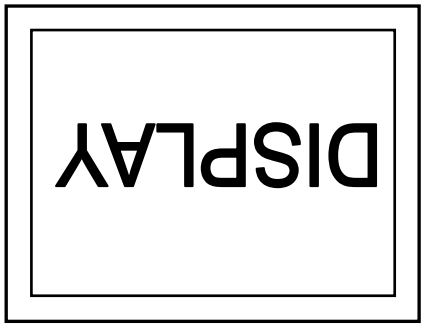
1) The display interface connector (CN1) is 20186-020E-11F made by I-PEX and pin assignment is as below:

Pin No.	Symbol	Function (ISP 6 bit compatibility mode)		Function (ISP 8 bit compatibility mode)
		6bit input	8 bit input	
1	V_{DD}	+3.3V Power supply		←
2	V_{DD}	+3.3V Power supply		←
3	GND	GND		←
4	GND	GND		←
5	Link 0-	R0, R1, R2, R3, R4, R5, G0	R2, R3, R4, R5, R6, R7, G2	R0, R1, R2, R3, R4, R5, G0
6	Link 0+	R0, R1, R2, R3, R4, R5, G0	R2, R3, R4, R5, R6, R7, G2	R0, R1, R2, R3, R4, R5, G0
7	GND	GND		←
8	Link 1-	G1, G2, G3, G4, G5, B0, B1	G3, G4, G5, G6, G7, B2, B3	G1, G2, G3, G4, G5, B0, B1
9	Link 1+	G1, G2, G3, G4, G5, B0, B1	G3, G4, G5, G6, G7, B2, B3	G1, G2, G3, G4, G5, B0, B1
10	GND	GND		←
11	Link 2-	B2, B3, B4, B5, DENA	B4, B5, B6, B7, DENA	B2, B3, B4, B5, DENA
12	Link 2+	B2, B3, B4, B5, DENA	B4, B5, B6, B7, DENA	B2, B3, B4, B5, DENA
13	GND	GND		←
14	CLKIN-	Clock-		←
15	CLKIN+	Clock+		←
16	GND	GND		←
17	Link 3-	See: Note 2	R0, R1, G0, G1, B0, B1	R6, R7, G6, G7, B6, B7
18	Link 3+	See: Note 2	R0, R1, G0, G1, B0, B1	R6, R7, G6, G7, B6, B7
19	MODE	Low=ISP 6 bit compatibility mode		High=ISP 8 bit compatibility mode
20	SC	Scan direction control(Low=Normal, High=Reverse		←

Note 1:Scan direction selector (SC)：



SC：Low

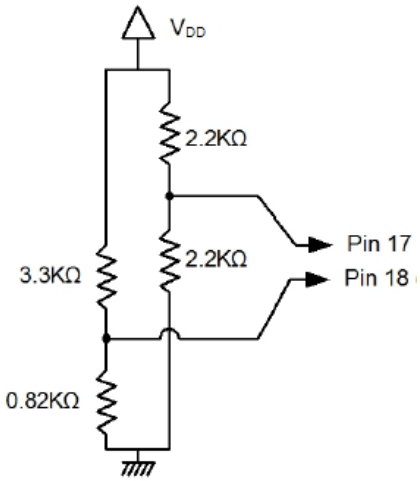


SC：High

Note 2: The Pin 19 (MODE) and Pin 20 (SC) are set high by the internal resistor of the driver IC. Suggest to set high or pull GND instead floating.

Note 3: The Pin 17 and Pin 18 should be set the constant level of the LVDS format in the JEIDA 6 bits Mode.

Reference only



2) The backlight interface connector (CN2) is 3800K-F08N-03 made by Entery, and pin assignment as below.

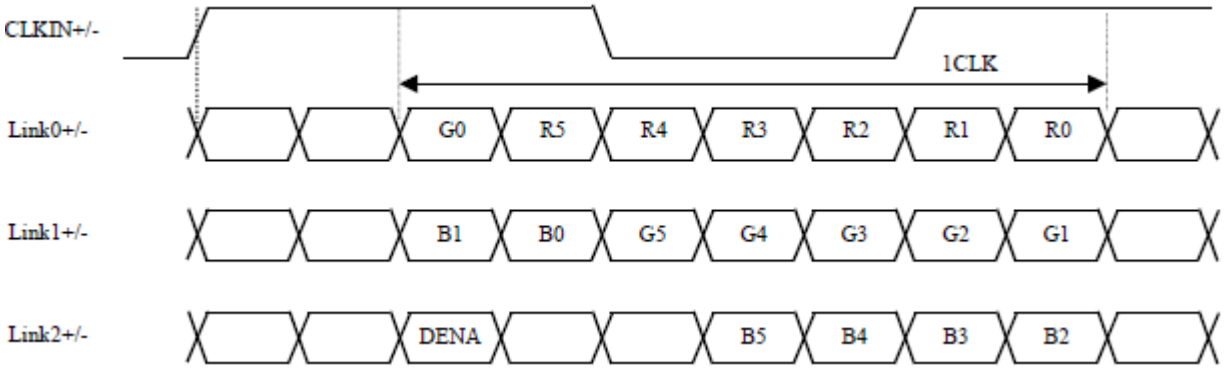
Corresponding connector：FI-S8S(JAE)

Pin No.	Symbol	Function
1	C1	LED Cathode1
2	A1	LED Anode1
3	A2	LED Anode2
4	C2	LED Cathode2
5	C3	LED Cathode3
6	A3	LED Anode3
7	A4	LED Anode4
8	C4	LED Cathode4

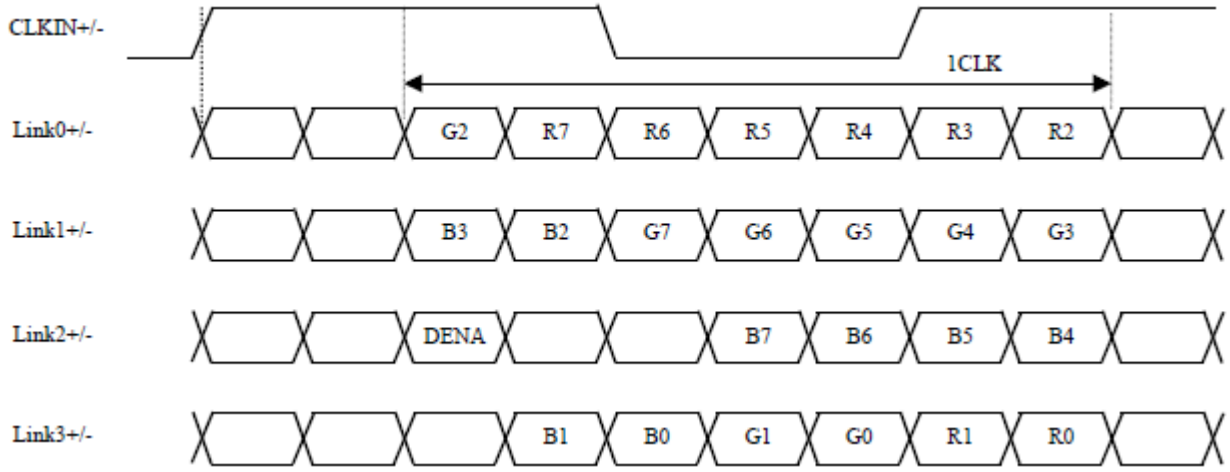
Note1: GND_L is connected GND (of CN1) and the LCD frame internally.

8.2 DATA MAPPING

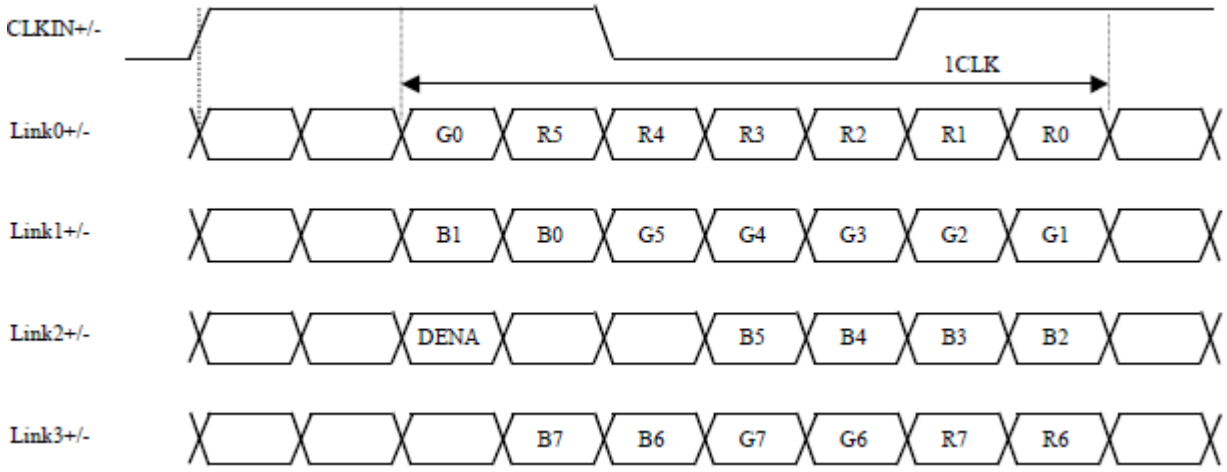
a. ISP 6 bit compatibility mode(6 bit input)



b. ISP 6 bit compatibility mode(8 bit input)



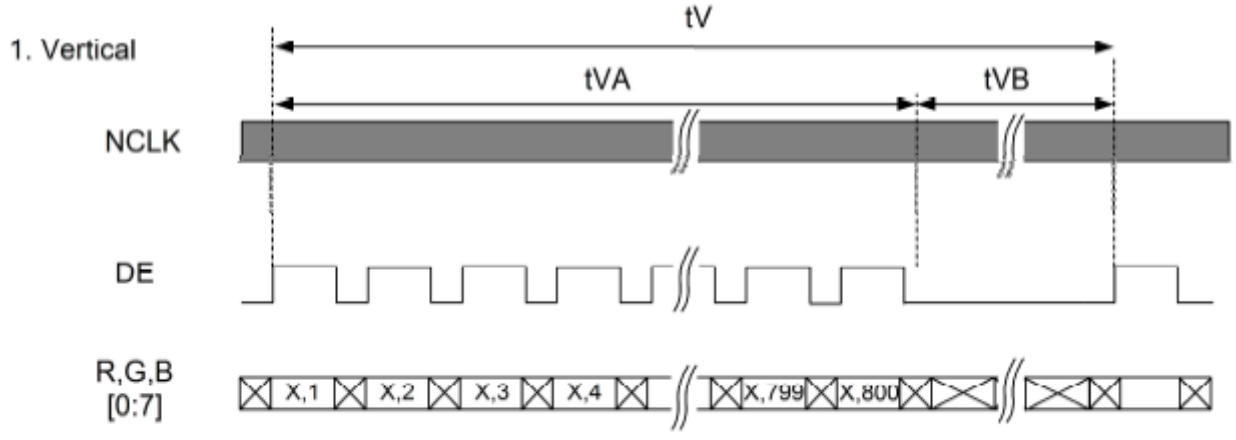
c. ISP 8 bit compatibility mode

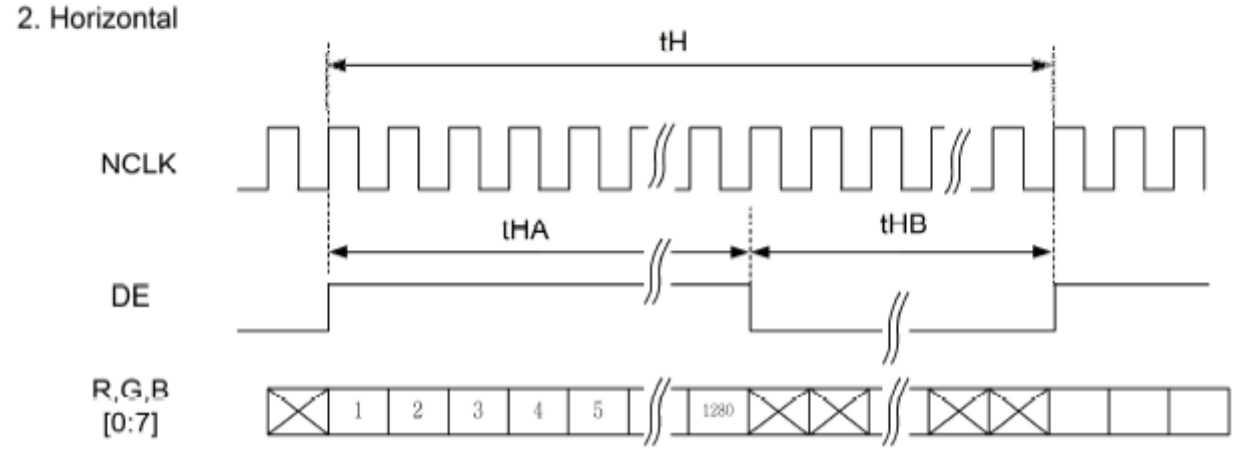


8.3 TIMING TABLE

Interface Timing (DE mode only)

Item			Symbol	Min.	Typ.	Max.	Unit
DCLK	Frequency		fCLK	66	67	71	MHz
	Period		tCLK	14.1	14.9	15.2	ns
DENK	Horizontal	Active Time	tHA	1280	1280	1280	t_{CLK}
		Blanking Time	tHB	70	80	90	t_{CLK}
		Frequency	fH	44.6	49.2	56.5	kHz
		Period	tH	17.7	20.3	22.4	μs
	Vertica	Active Time	tVA	800	800	800	t_H
		Blanking Time	tVB	10	20	70	t_H
		Frequency	fv	55	60	65	Hz
		Period	tv	15.4	16.7	18.1	ms

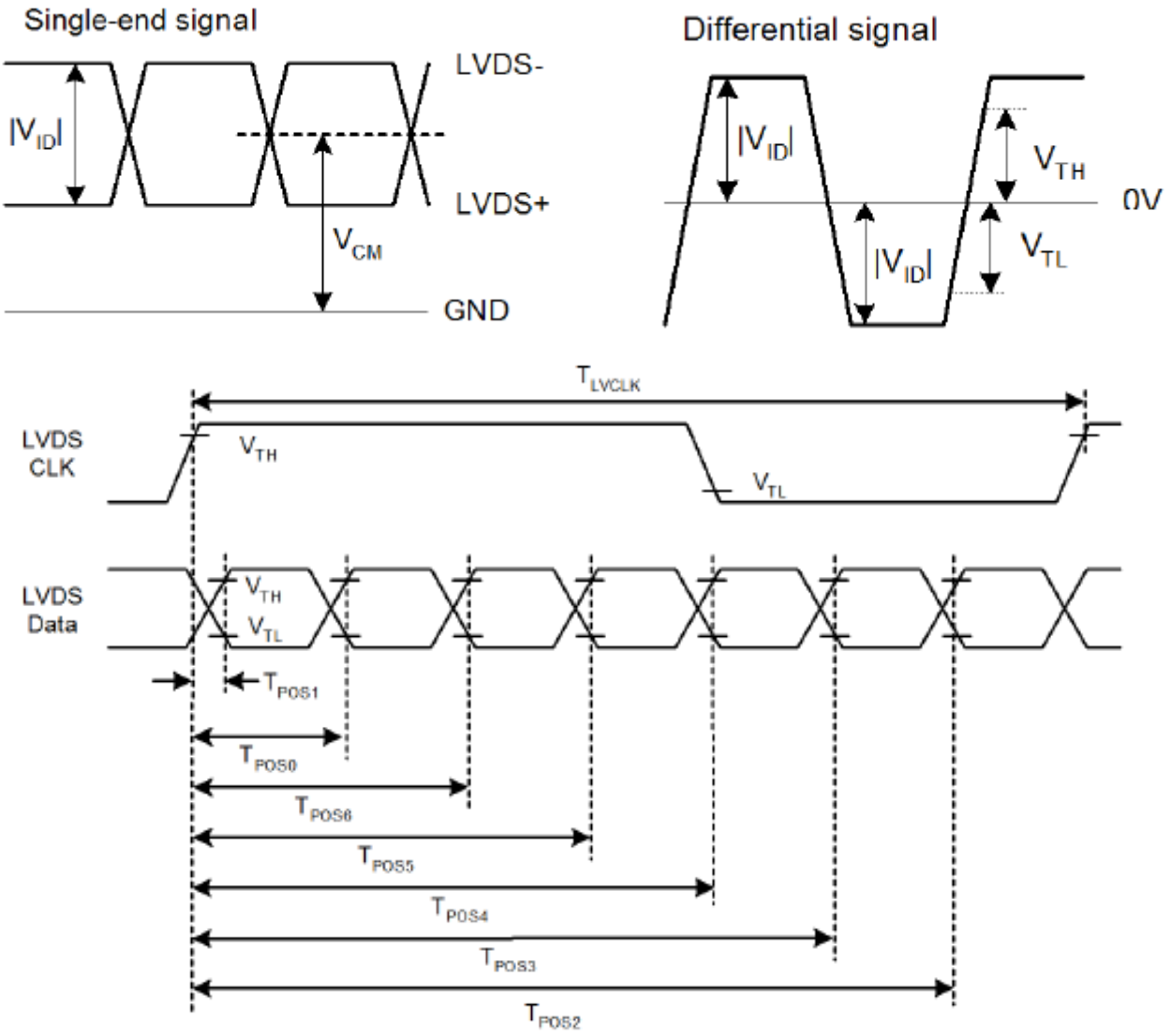




Note 1: All timing parameters should be constant in each frame.

Note 2: Blanking time tolerance (Base on IC specification) :3 ≧ | tVBn − tVBn-1 | ≧ 0

8.4 LVDS RECEIVER TIMING



Item	Symbol	Min.	Typ.	Max.	Unit	
Differential Input High threshold	V_{TH}	-	-	200	mV	
Differential Input Low Threshold	V_{TL}	-200	-	-	mV	
Differential Input Common Mode Voltage	V_{CM}	1.0	1.2	1.7-|V_{ID}|/2	V	
Input Leakage Current	I_{IN}	-10	-	10	uA	RX+/-, RXC+/-
Differential Input Voltage	|V_{ID}|	200	-	600	mV	
1 date bit time	UI	-	1/7	-	T_{LVCLK}	
Position 1	T_{POS1}	-0.25	0	0.25	UI	
Position 0	T_{POS0}	0.75	1	1.25		
Position 6	T_{POS6}	1.75	2	2.25		
Position 5	T_{POS5}	2.75	3	3.25		
Position 4	T_{POS4}	3.75	4	4.25		
Position 3	T_{POS3}	4.75	5	5.25		
Position 2	T_{POS2}	5.75	6	6.25		

8.5 DATA INPUT for DISPLAY COLOR

a. 6 bit input

Input color		Red Data						Green Data						Blue Data					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
		MSB					LSB	MSB					LSB	MSB					LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note 1: Definition of gray scale :

Color(n) ---n indicates gray scale level.

Higher n means brighter level.

Note 2: Data

1 : High, 0 : Low

b. 8 bit input

Input color		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note 1: Definition of gray scale :

Color(n) ---n indicates gray scale level.

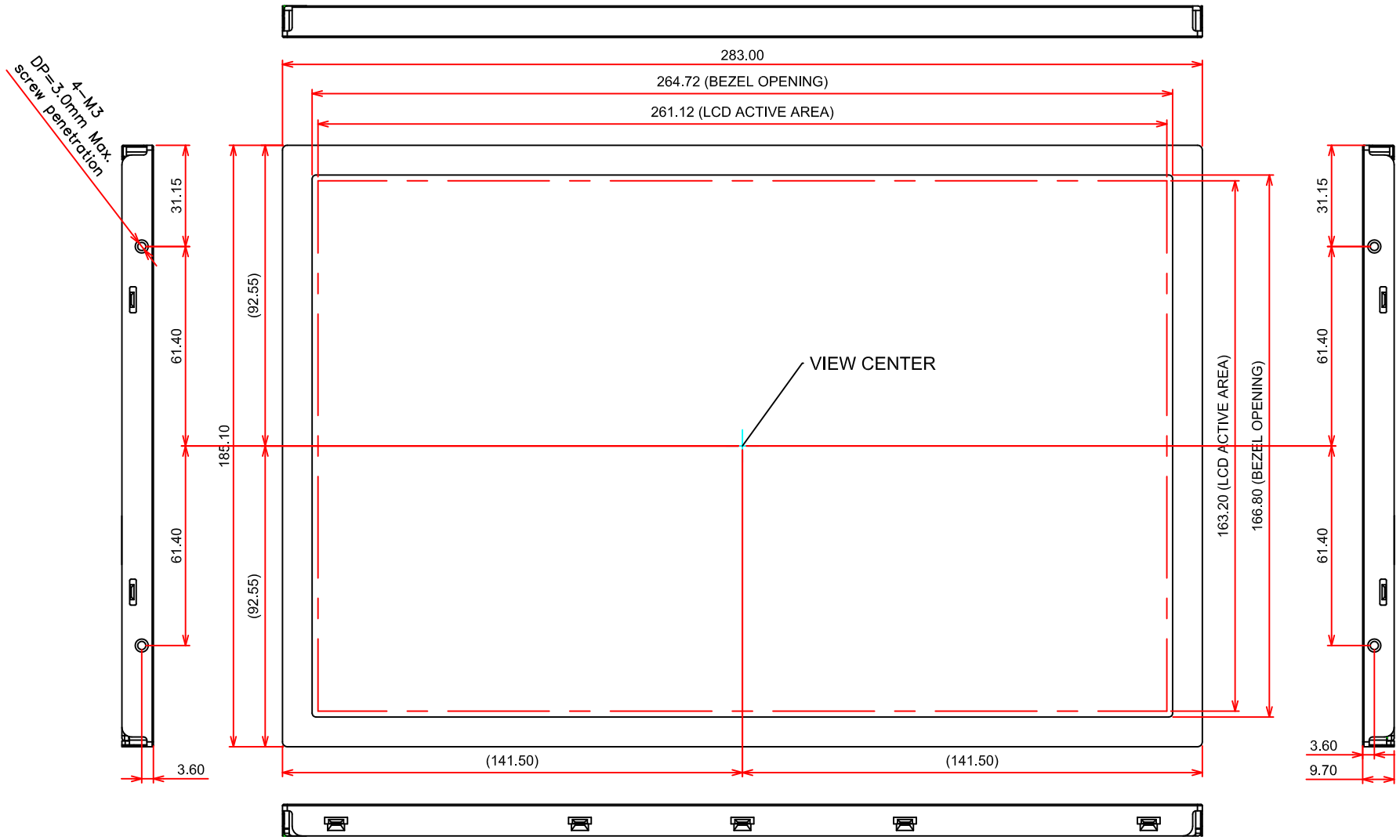
Higher n means brighter level.

Note 2: Data

1 : High, 0 : Low

9. OUTLINE DIMENSIONS

9.1 FRONT VIEW



General Tolerance:±0.5mm
Scale : NTS
Unit : mm

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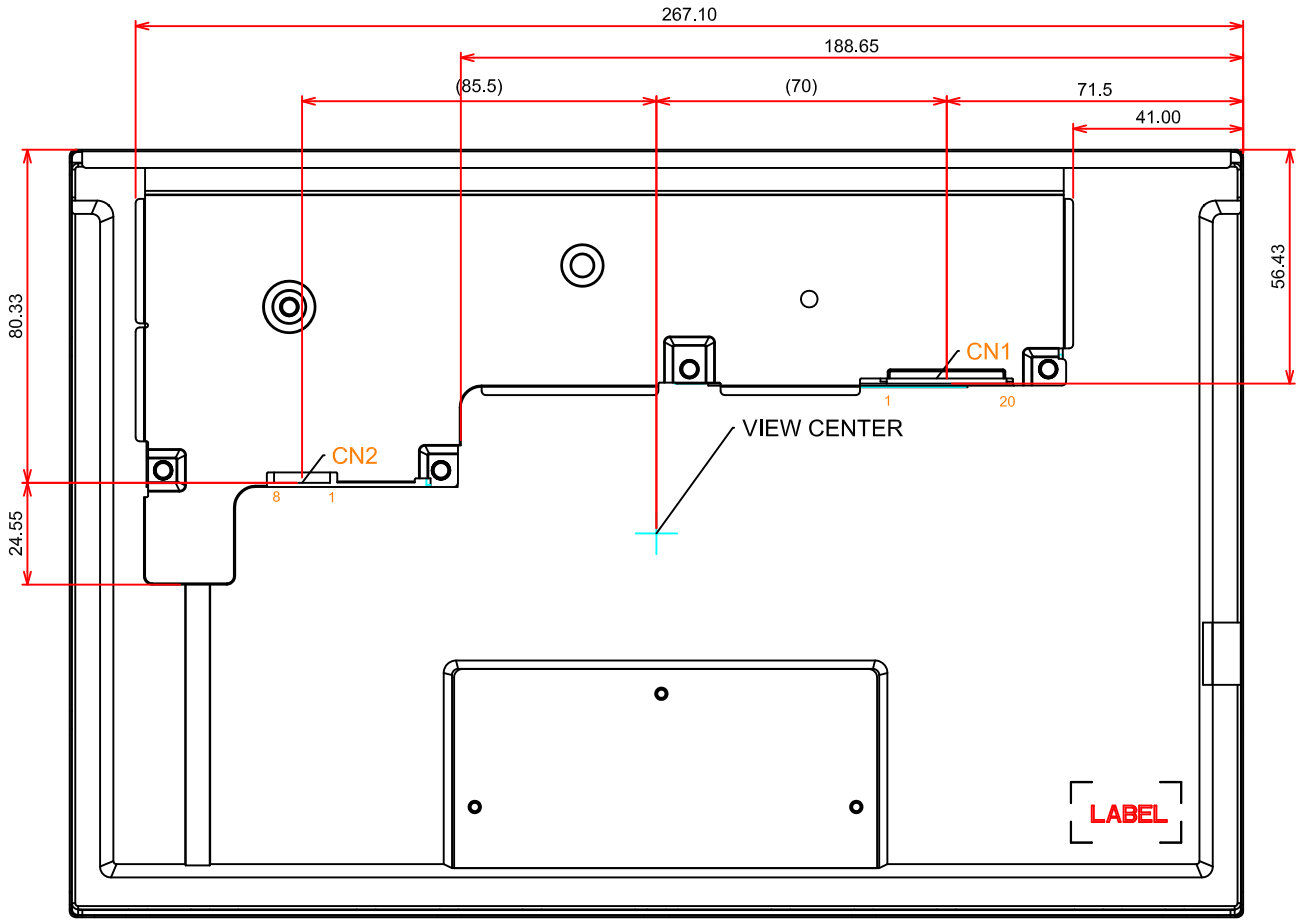
9.2 REAR VIEW



Note 1) CN1 : 20186-020E-11F (I-PEX)
CN2 : 3800K-F08N-03 (ENTERY)

General Tolerance:±0.5mm
Scale : NTS
Unit : mm

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10. DESIGNATION of LOT MARK

1) The lot mark is showing in Fig.10.1. First 4 digits are used to represent production lot, T represented made in Taiwan, and the last 6 digits are the serial number.

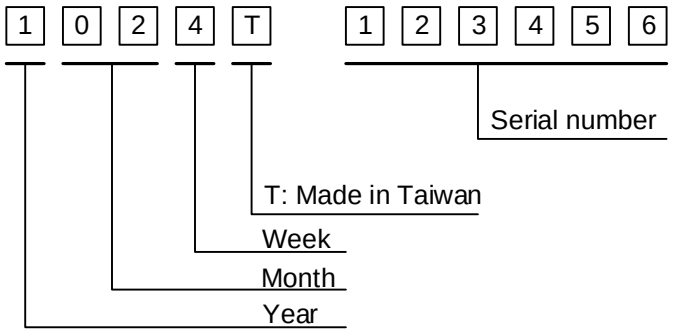

Fig. 10.1

2) The tables as below are showing what the first 4 digits of lot mark are shorted for.

Year	Lot Mark
2021	1
2022	2
2023	3
2024	4
2025	5

Month	Lot Mark	Month	Lot Mark
Jan.	01	Jul.	07
Feb.	02	Aug.	08
Mar.	03	Sep.	09
Apr.	04	Oct.	10
May	05	Nov.	11
Jun.	06	Dec.	12

Week	Lot Mark
1~7 days	1
8~14 days	2
15~21 days	3
22~28 days	4
29~31 days	5

3) Except letters I and O, revision number will be shown on lot mark and following letters A to Z.

4) The location of the lot mark is on the back of the display shown in Fig. 10.2.

Label example:

Fig. 10.2