CONFIDENTIAL(B)

SPECIFICATION

OF

LIQUID CRYSTAL DISPLAY MODULE

UNITED RADIANT TECHNOLOGY CORP. 光聯科技 Sep-23-2022 品管部 QC DEPT.

CUSTOMER : URT-STD

Model No. : UMOH-9587MD-T

Model version : 2

Document Revision : 2

CUSTOMER APPROVED SIGNATURE			

This specification need to be signed by purchaser or customer as a specification of products production and delivery from URT. Without signature of this specification , any purchase order for this model no. will be treated and considered that this specification is automatically acknowledged and accepted by purchaser or customer.

U.R.T. UNITED RADIANT TECHNOLOGY CORPORATION

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APPROVED	CHECKED	PREPARED	Date

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Revision record

Document Revision	Model No. Version No.	Description	Revision by
0	UMOH-9587MD-T Version No.0	7” TFT LCD, 800*1280 dots.	Aiching Cheng Y.C. Lin 13-May-2022
1	UMOH-9587MD-T Version No.1	Add the backlight lifetime specification.	Aiching Cheng Y.C. Lin 24-May-2022
2	UMOH-9587MD-T Version No.2	Mark the connector brand name.	Aiching Cheng Y.C. Lin 23-Sep-2022

CONTENTS:

1. BASIC SPECIFICATION

1.1 Mechanical specifications

Items	Nominal Dimension	Unit
Active screen size	7.0” diagonal	-
Dot Matrix	800 x R.G.B. x 1280	Pixel
Module Size (W x V x T)	99.85 x 161.7 x 2.6	mm.
Active Area (W x V)	94.2 x 150.72	mm.
Dot Pitch (W x V)	0.11775 x 0.11775	mm.
Color depth	16.7M	color
Interface	MIPI interface	-
LCM Driver IC	ILI9881	-
Driving IC Package	COG	-
Module Weight	84±10%	g

1.2 Display specification

Display	Descriptions	Note
LCD Type	IPS	-
LCD Mode	Normally Black	-
Polarizer Mode	Transmission	-
Polarizer Surface	Anti-Glare	-
Pixel arrangement	RGB vertical stripe	-
Backlight Type	LED	-
Viewing Direction	Full	-

1.3 Outline dimension

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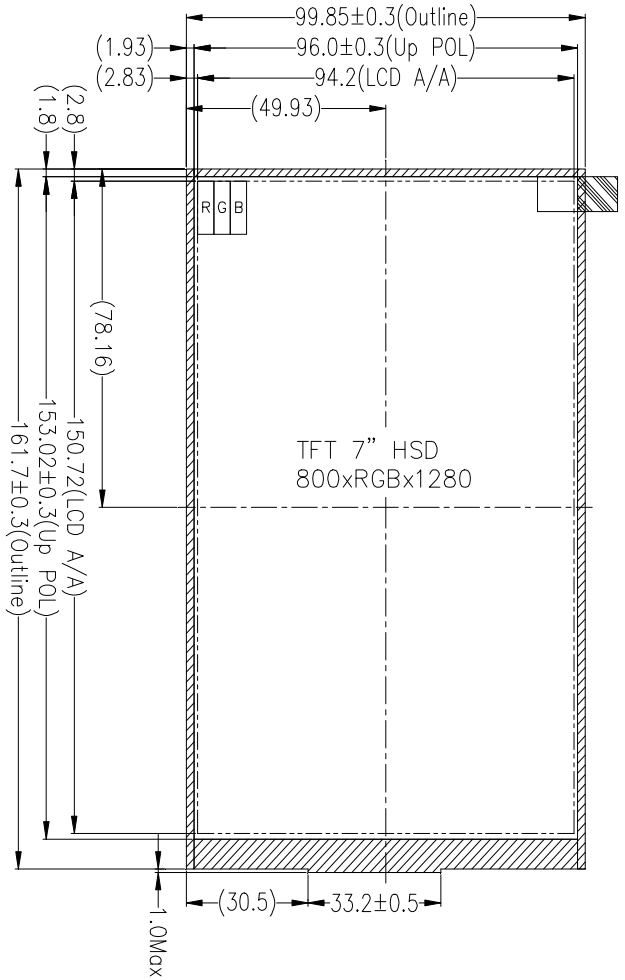
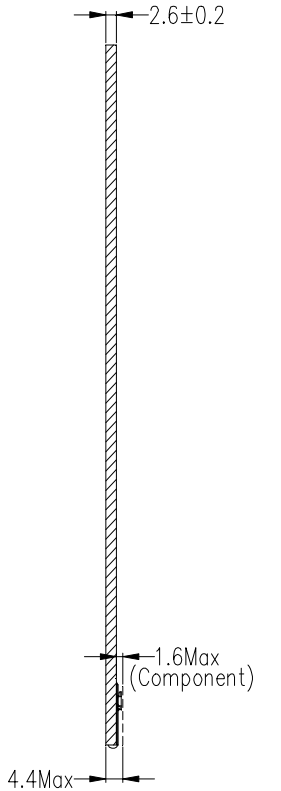
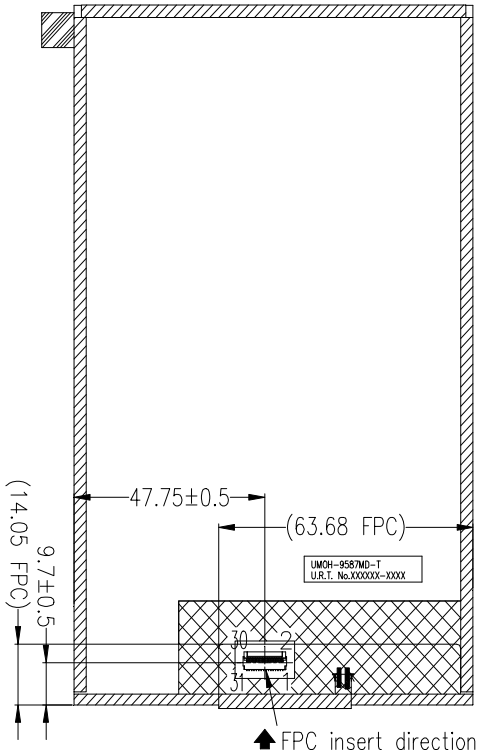


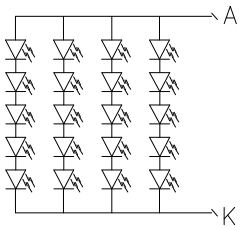




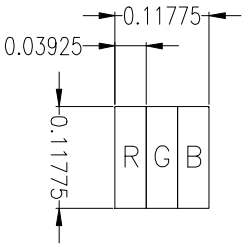
Connector
PIN ASSIGNMENT

Pin No.	Signal
1	VLED(A)
2	VLED(A)
3	VLED(A)
4	NC
5	FB1(K)
6	FB2(K)
7	FB3(K)
8	FB4(K)
9	GND
10	GND
11	MIPI-2P
12	MIPI-2N
13	GND
14	MIPI-1P
15	MIPI-1N
16	GND
17	MIPI-CLKP
18	MIPI-CLKN
19	GND
20	MIPI-0P
21	MIPI-0N
22	GND
23	MIPI-3P
24	MIPI-3N
25	GND
26	NC
27	RESET
28	NC
29	VDD1V8
30	VDD3V3
31	VDD3V3

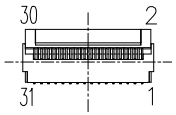
NOTE:
1. LCD: 7.0" TFT, Transmissive Type,
   Normally Black, Anti-Glare
2. Top: -20~+70°C, Tst: -30~+80°C
3. TFT Viewing Direction: Full Viewing
4. Backlight LED Color:
   White 5x4=20 pcs,
   Constant Current If=80mA, Vf=15.0V(typ)
5. Tolerance for not assigned: ±0.3 mm
6. This product conform with the standard of ROHS



LED Backlight
Circuit Diagram

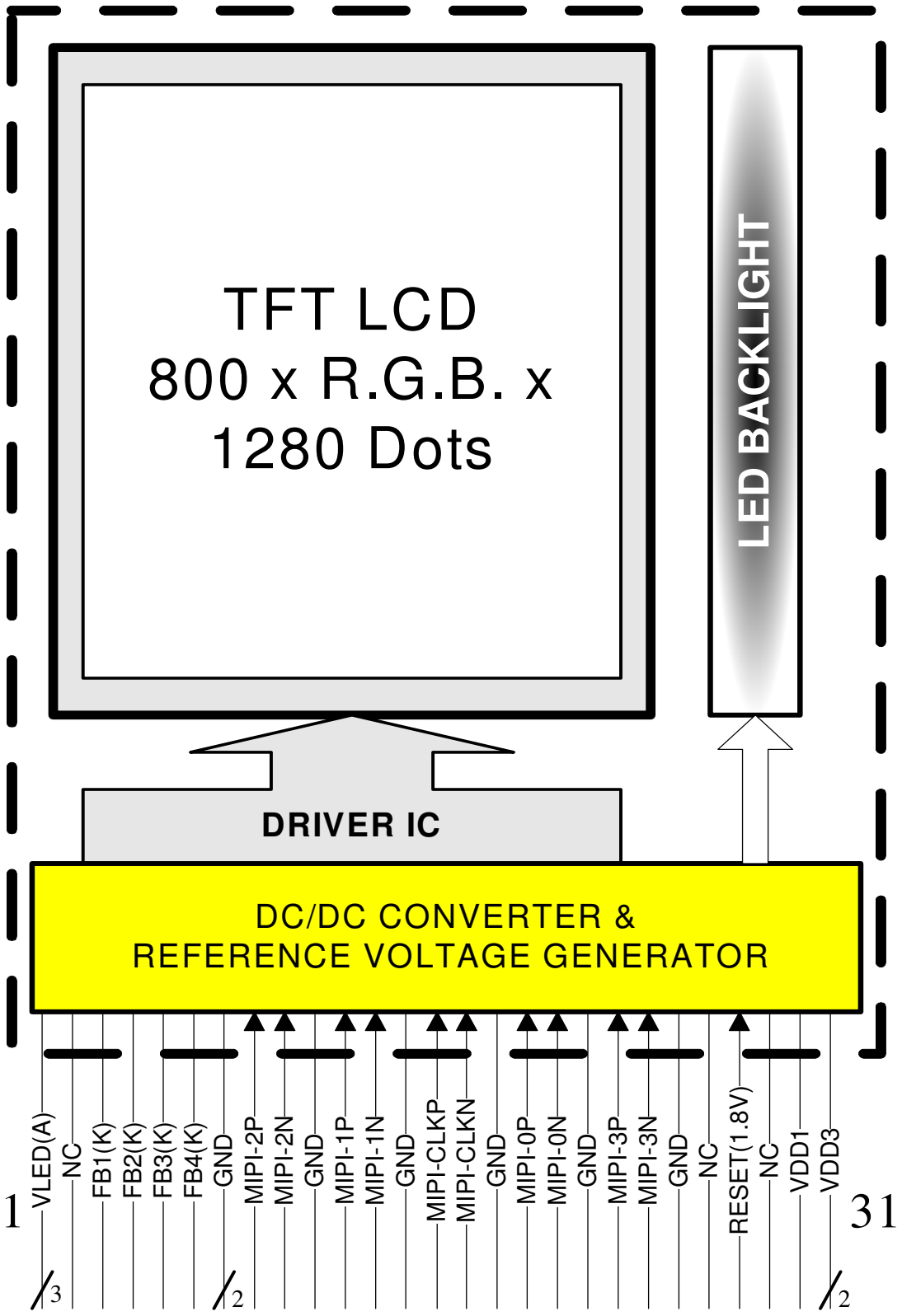


Pixel Detail



HIROSE Connector:
FH35C-31S-0.3SHW

1.4 Block diagram:



1.5 Interface pin Connection:

Pin No.	Pin Symbol	I/O	Description
1~3	VLED(A)	P	Power for LED backlight (Anode)
4	NC	-	No connection
5	FB1(K)	P	Power for LED backlight (Cathode)
6	FB2(K)	P	Power for LED backlight (Cathode)
7	FB3(K)	P	Power for LED backlight (Cathode)
8	FB4(K)	P	Power for LED backlight (Cathode)
9~10	GND	P	Ground
11	MIPI-2P	I	MIPI data positive signal
12	MIPI-2N	I	MIPI data negative signal
13	GND	P	Ground
14	MIPI-1P	I	MIPI data positive signal
15	MIPI-1N	I	MIPI data negative signal
16	GND	P	Ground
17	MIPI-CLKP	I	MIPI CLK positive signal
18	MIPI-CLKN	I	MIPI CLK negative signal
19	GND	P	Ground
20	MIPI-0P	I	MIPI data positive signal
21	MIPI-0N	I	MIPI data negative signal
22	GND	P	Ground
23	MIPI-3P	I	MIPI data positive signal
24	MIPI-3N	I	MIPI data negative signal
25	GND	P	Ground
26	NC	-	No connection
27	RESET(1.8V)	I	Chip reset pin
28	NC	-	No connection
29	VDD1	P	A power supply for the logic power and I/O circuit. VDD1=1.65 to 3.6V.
30~31	VDD3	P	A power supply for the analog power. VDD3=3.0V to 3.6V.

2. ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit
Power Supply Voltage	VDD1	1.65	3.6	V
	VDD3	-0.3	6.0	
Input Voltage	VIH	0.7*VDD1	VDD1	V
	VIL	0	0.3*VDD1	
Operate temperature range	TOP	-20	70	℃
Storage temperature range	TST	-30	80	℃

2.2 DC Characteristics

Typical Operation Conditions

(Note 1) T_a= 25℃

Items	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	VDD1	1.65	1.8	3.6	V
	VDD3	3.0	3.3	3.6	V

Current Consumption

(Note 1) T_a= 25℃

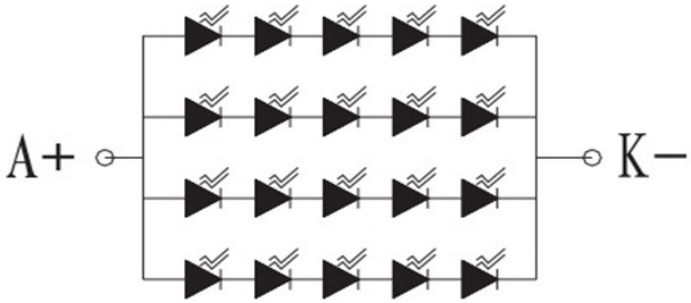
Items	Symbol	Min.	Typ.	Max.	Unit
Current for Driver	IVDD1	-	25	-	mA
	IVDD3	-	45	-	mA

2.3 Back-light only Specification:

PARAMETER	Symbol	MIN	TYP	MAX	Unit	Note
LED Light Bar Power Supply Voltage	VL	-	16.5	-	V	Total LED
LED Light Bar Power Supply Current	IL	-	80	-	mA	IF=80mA
Peak forward current	IFP		100		mA	Total LED
Half-Life Time	Lf	-	50000	-	hrs	1

Note 1：The "Half-Life Time" is defined as the LED chip brightness decreases to 50% than original brightness, based on Ta 25±2℃,60±10% RH condition.

Internal Circuit Diagram

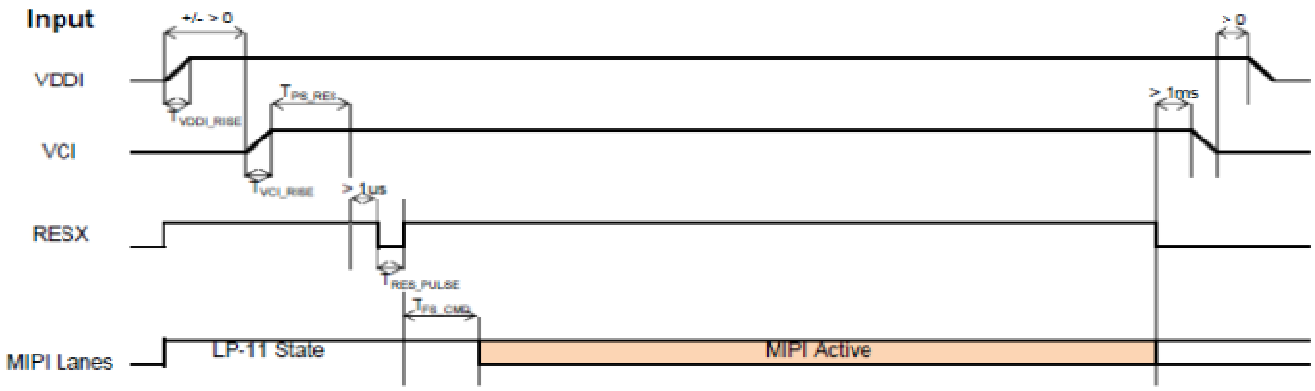


CURRENT IF=80mA

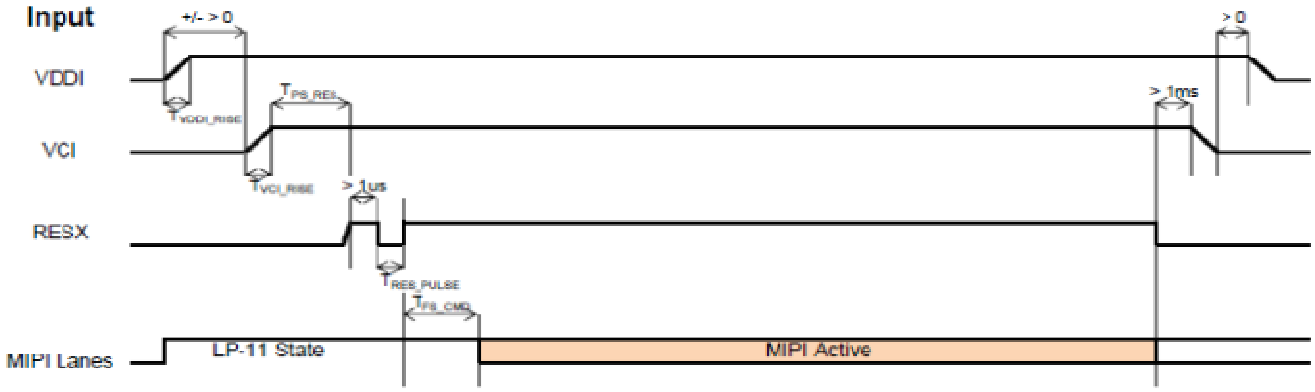
5*4=20LED

2.4 POWER ON/OFF SEQUENCE

Case A:



Case B:



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

2.5 INITIAL CODE

FFH	98H	20H	05H	50H	10H
	81H	21H	02H	51H	32H
	03H	22H	00H	52H	54H
		23H	00H	53H	76H
01H	00H	24H	00H	54H	98H
02H	00H	25H	00H	55H	BAH
03H	72H	26H	00H	56H	10H
04H	00H	27H	00H	57H	32H
05H	00H	28H	33H	58H	54H
06H	09H	29H	22H	59H	76H
07H	00H	2AH	00H	5AH	98H
08H	00H	2BH	00H	5BH	BAH
09H	00H	2CH	00H	5CH	DCH
0AH	00H	2DH	00H	5DH	FEH
0BH	00H	2EH	00H	5EH	00H
0CH	00H	2FH	00H	5FH	01H
0DH	00H	30H	00H	60H	00H
0EH	00H	31H	00H	61H	15H
0FH	00H	32H	00H	62H	14H
10H	00H	33H	00H	63H	0EH
11H	00H	34H	04H	64H	0FH
12H	00H	35H	00H	65H	0CH
13H	00H	36H	00H	66H	0DH
14H	00H	37H	00H	67H	06H
15H	00H	38H	3CH	68H	02H
16H	00H	39H	00H	69H	02H
17H	00H	3AH	00H	6AH	02H
18H	00H	3BH	00H	6BH	02H
19H	00H	3CH	00H	6CH	02H
1AH	00H	3DH	00H	6DH	02H
1BH	00H	3EH	00H	6EH	07H
1CH	00H	3FH	00H	6FH	02H
1DH	00H	40H	00H	70H	02H
1EH	40H	41H	00H	71H	02H
1FH	80H	42H	00H	72H	02H
		43H	00H	73H	02H
		44H	00H	74H	02H
				75H	01H

76H 00H	35H 1FH	B2H 5BH
77H 14H	33H 14H	B3H 23H
78H 15H	7AH 0FH	C0H 00H
79H 0EH	38H 01H	C1H 11H
7AH 0FH	39H 00H	C2H 1EH
7BH 0CH		C3H 0FH
7CH 0DH	FFH 98H	C4H 12H
7DH 06H	81H	C5H 26H
7EH 02H	01H	C6H 1CH
7FH 02H		C7H 1EH
80H 02H	22H 0AH	C8H 87H
81H 02H	31H 00H	C9H 19H
82H 02H	53H 45H	CAH 26H
83H 02H	55H 4EH	CBH 7FH
84H 07H	50H C7H	CCH 20H
85H 02H	51H C2H	CDH 22H
86H 02H	60H 25H	CEH 58H
87H 02H	63H 00H	CFH 2AH
88H 02H		D0H 2EH
89H 02H	A0H 00H	D1H 50H
8AH 02H	A1H 16H	D2H 5DH
	A2H 26H	D3H 23H
FFH 98H	A3H 16H	
81H	A4H 19H	FFH 98H
04H	A5H 2BH	81H
	A6H 1EH	00H
6EH 2AH	A7H 20H	
6FH 35H	A8H 93H	11H
3AH 24H	A9H 20H	DELYA(120ms)
8DH 14H	AAH 2CH	29H
87H BAH	ABH 87H	
26H 76H	ACH 1FH	
B2H D1H	ADH 1FH	
B5H 27H	AEH 53H	
31H 75H	AFH 27H	
30H 03H	B0H 2AH	
3BH 98H	B1H 52H	

2.6 DC ELECTRICAL CHARACTERISTIC

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VCI	-	2.5	2.8	6.6	V	
Analog operating voltage	VCIREF		2.5	2.8	6.6	V	
Digital operating voltage	VDDI	-	1.65	2.8	3.6	V	
Digital operating voltage	VCC1		1.65	2.8	6.6	V	
Digital operating voltage	VCC2		1.65	2.8	6.6	V	
DSI operating voltage	VDDAM	-	1.65	1.8	3.6	V	
OTP Supply voltage	MTP_PWR	-	8.4	8.5	8.6	V	
Analog operating voltage	VSP	-	4.5		6.6	V	
Analog operating voltage	VSN	-	-6.6		-4.5	V	
Logic High level input voltage	VIH	-	0.7*VDDI		VDDI	V	Note1
Logic Low level input voltage	VIL	-	-0.3		0.3*VDDI	V	Note1
Logic High level output voltage TE , LEDPWM	VOH	IOH = -1.0mA	0.8*VDDI		VDDI	V	Note1
Logic Low level output voltage TE , LEDPWM	VOL	IOL = +1.0mA	0		0.2*VDDI	V	Note1
Gate Driver High Voltage	VGH	-	8.0	-	18	V	
Gate Driver Low Voltage	VGL	-	-18.0	-	-7.0	V	
Driver Supply Voltage	-	|VGH-VGL|	15	-	32	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-4.0	-	0	V	Note3

Notes:

1. Ta = -30 to 70 °C (to 85 °C no damage) , VCI = 2.5V to 6.6V, VDDI = 1.65V to 3.6V
2. Supply digital VDDI voltage equal or less than analog VCI voltage.
3. Source channel loading = 9KΩ,70pF/channel

2.7 AC characteristics

DSI Timing CharacteristicsHigh Speed Mode

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VDD=2.5V to 3.6V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	2xUI$_{INST}$	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UI$_{INSTA}$ UI$_{INSTB}$	UI instantaneous halfs (UI = UI$_{INSTA}$ = UI$_{INSTB}$)	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15xUI	-	-	ps	
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3xUI	ps	

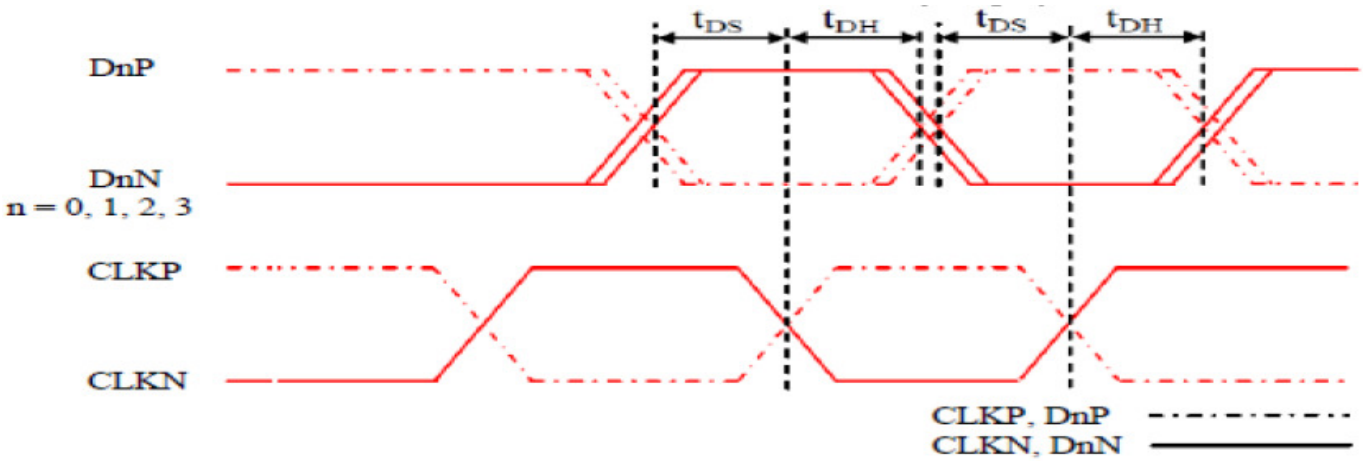


Figure 106: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

DSI clock channel timing

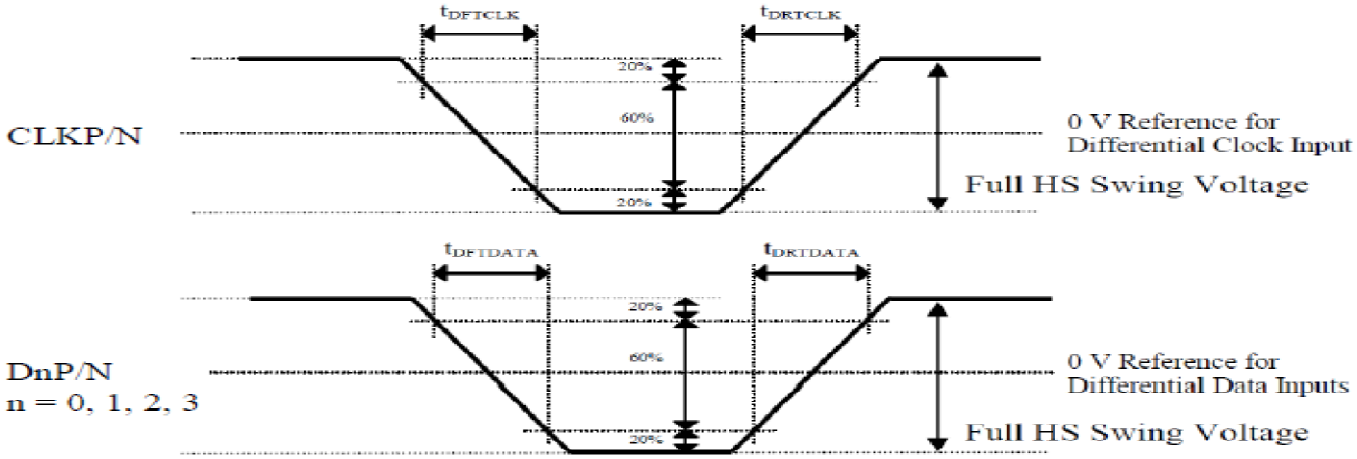


Figure 107: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

Rising and fall time on clock and data channel

2.8 Timings for DSI Video mode

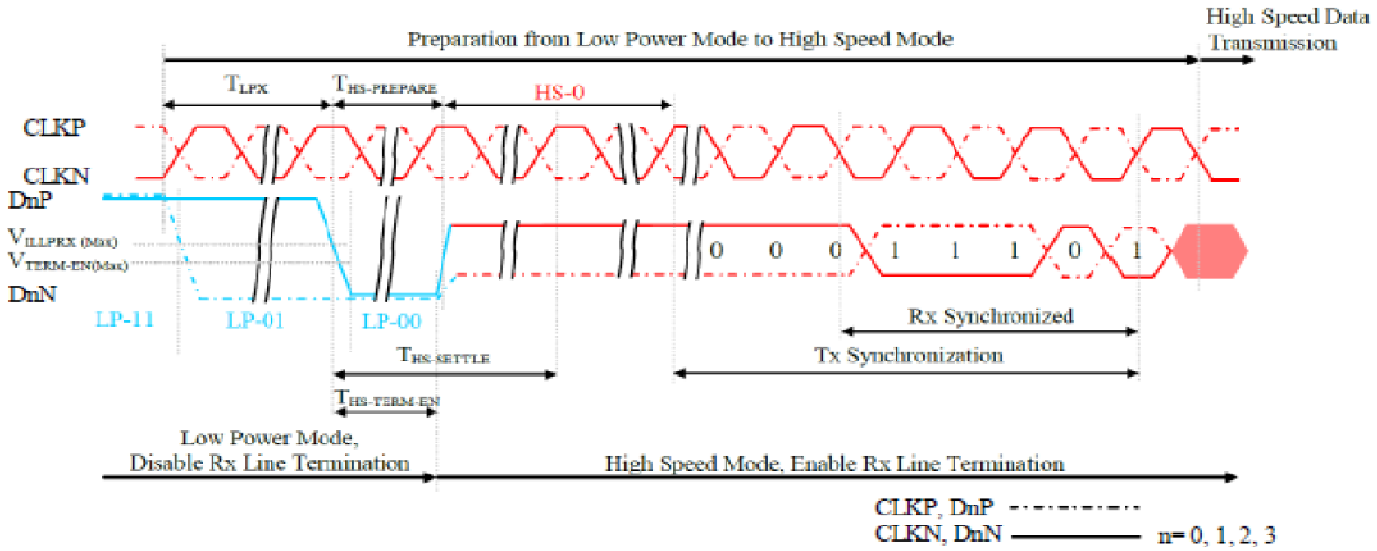


Figure 110: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

Clock lanes-High Speed Mode to/from Low Power Mode Timing

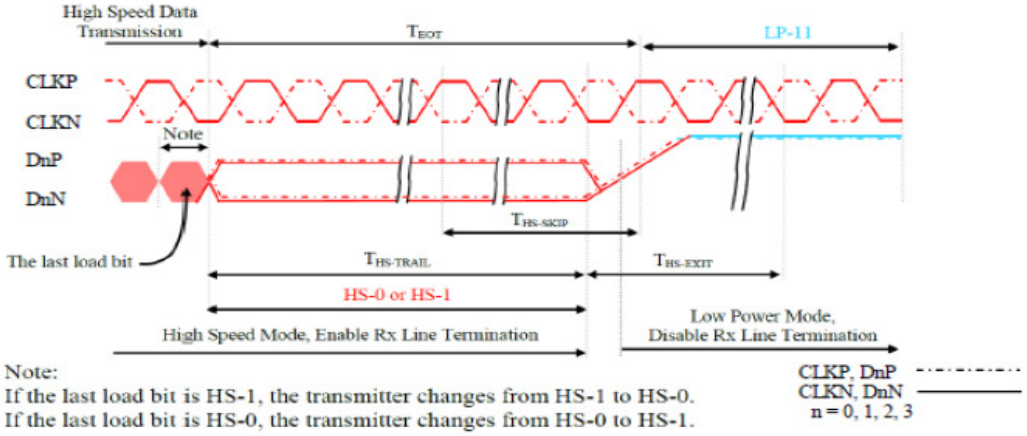
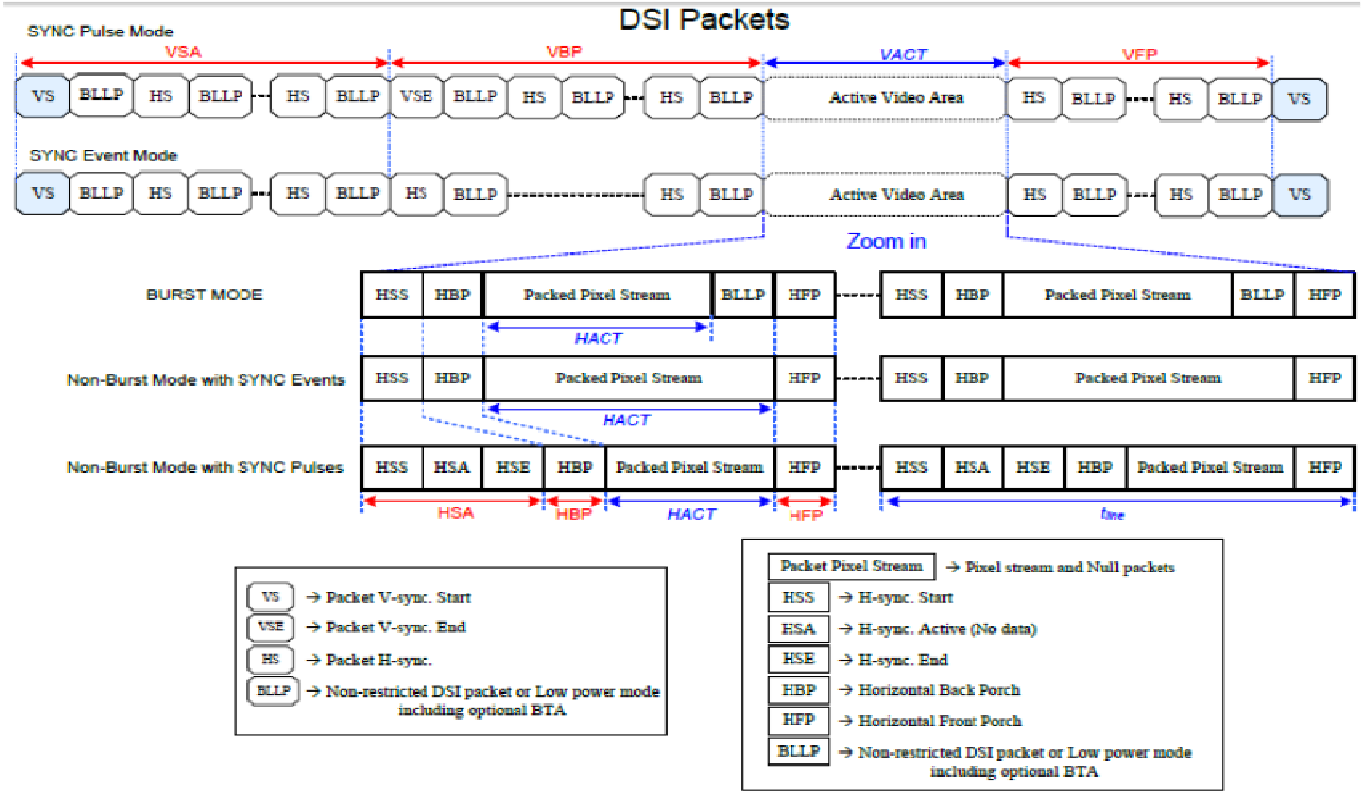


Figure 111: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C-04) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

2.9 Parallel RGB input timing table



1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example : BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

Note:

1. Lanenum: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.1DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.
5. Please reference to “Table 39: Limited Clock Channel Speed”.
6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

3. OPTICAL CHARACTERISTICS

3.1 Characteristics

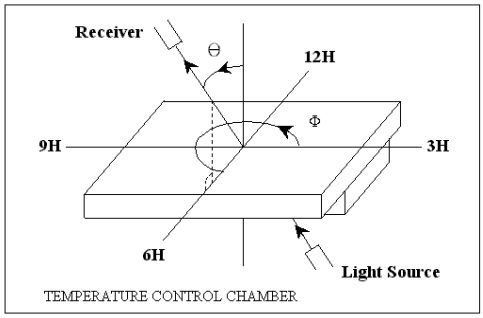
Electrical and Optical Characteristics

No.	Item			symbol / temp.		Min.	Typ.	Max.	Unit	Note
1	Response Time			Tr+Tf	θ=Φ=0°	-	30	35	ms	2
2	Viewing Angle	Hor.	Cr≧10	θ_{2+}	Φ= 0°	-	85	-	degree	3
				θ_{2-}	Φ= 180°	-	85	-		
		Ver.		θ_{1+}	Φ= 270°	-	85	-		
				θ_{1-}	Φ= 90°	-	85	-		
3	Contrast Ratio			Cr	25 ℃	-	700	-	-	4
4	Red x-code			Rx	25 ℃	0.577	0.627	0.677	-	5
	Red y-code			Ry		0.295	0.345	0.395		
	Green x-code			Gx		0.303	0.353	0.403		
	Green y-code			Gy		0.553	0.603	0.653		
	Blue x-code			Bx		0.093	0.143	0.193		
	Blue y-code			By		0.033	0.083	0.133		
	White x-code			Wx		0.240	0.290	0.340		
	White y-code			Wy		0.274	0.324	0.374		
	Brightness			Y		420	500	-	cd/m^2	
5	Brightness Uniformity				25 ℃	70	80	-	%	6

3.2 Definition of optical characteristics

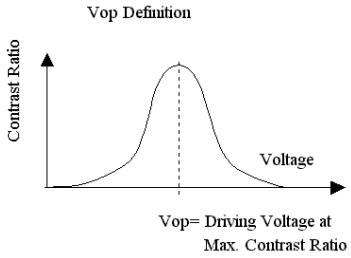
Measurement condition :

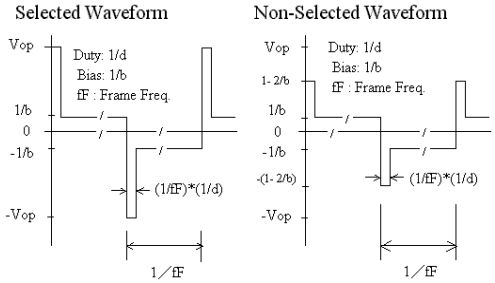
Transmissive and Transflective type



PHOTAL LCD-5000

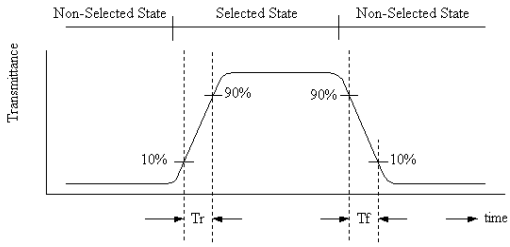
[Note 1] Definition of LCD Driving Vop and Waveform :



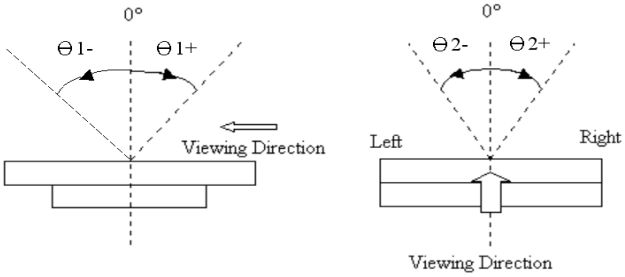


[Note 2] Definition of Response Time

for Negative type :

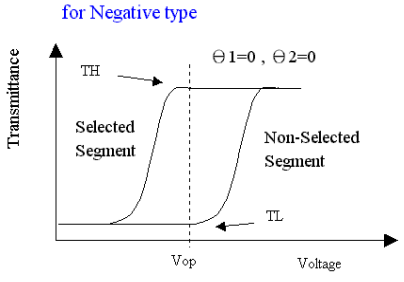


[Note 3] Definition of Viewing Angle :



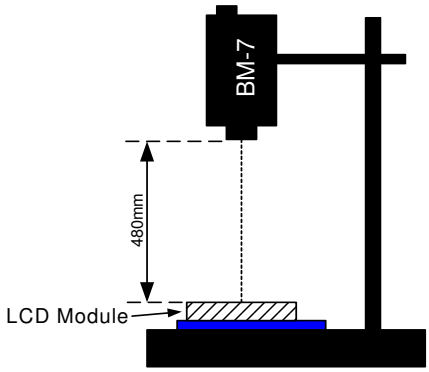
[Note 4] Definition of Contrast Ratio :

for Negative type

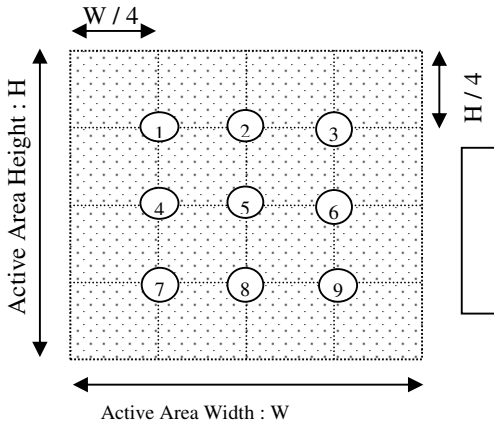


$$\text{Contrast Ratio} = \frac{TH}{TL}$$

[Note 5] Definition of measurement of Color Chromaticity and Brightness

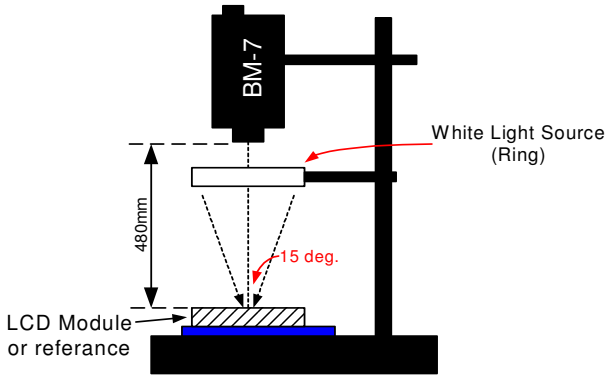


[Note 6] Definition of Brightness Uniformity

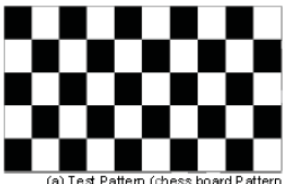
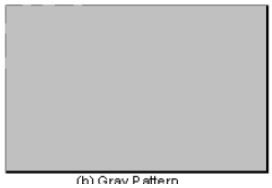


$$\text{Brightness Uniformity} = \frac{\text{Minimum Brightness of Point 1~9}}{\text{Maximum Brightness of Point 1~9}}$$

[Note 7] Definition of Measurement of Reflectance



4. RELIABILITY :

Item No	Items	Condition	Remark	
1	High temperature operating	70 ℃ , 96 hours	1	
2	Low temperature operating	-20 ℃ , 96 hours	1	
3	High temperature storage	80 ℃ , 96 hours	1	
4	Low temperature storage	-30 ℃ , 96 hours	1	
5	High temperature & humidity storage	60℃, 90%RH, 96hours	2	
6	Thermal Shock storage	-30℃, 30min.<=> 80℃, 30min. 10 Cycles	1	
7	Vibration test	10 => 55 =>10 => 55 => 10 Hz , within 1 minute Amplitude : 1.5mm. 15 minutes for each Direction (X,Y,Z)		
8	ESD test	150pF , 330Ω Contact:±4KV,Air:±8KV	1	Class C
		200pF, 0Ω, ±200V contact test	2	
9	Image Sticking Test	25 ± 2℃ Operation with test pattern sustained for 1hrs, then change to 50% gray pattern immediately.after5mins,themura must be disappeared completely.  (a) Test Pattern (chess board Pattern)  (b) Gray Pattern		

Note 1：The product move into the room temperature for at least 2 hours with no condensation.

Note 2：The product move into the room temperature for at least 24 hours with no condensation.

Note 3 : Please change the display picture (autorun) during operating mode. Avoid displaying static images to avoid image sticking , and the image sticking is accelerated by temperature.

* One single product test for only one item.

* Judgment after test : keep in room temperature for more than 2 hours.

- Current consumption < 2 times of initial value
- Function : work normally

5. PRODUCT HANDLING AND APPLICATION

☐ PRECAUTION FOR HANDLING LCM

- The LCD module contains a C-MOS LSI. People who operate the LCM should wear ESD protection eguipement to prevent ESD hurt on products.
- Do not input any signal before power is turned on.
- Do not take LCM from its packaging bag until it is assembled.
- Peel off the LCM protective film slowly since static electricity may be generated.
- Pay attention to the humidity of the work shop, 50~60%RH is satisfactory.
- Use a non-leak iron for soldering LCM.
- Do not touch the display surface or connection terminals area with bare hands.Smudges on the display surface reduce the insulation between terminals.
- Cautions for soldering to LCM:

  Condition for soldering I/O terminals:
  Temperature at iron tip :350℃±15℃.
  Soldering time : 3~4sec./ terminals.
  Type of solder : Eutectic solder(rosin flux filled).

☐ PRECAUTION IN USE OF LCD

- Do not contact or scratch the front surface and the contact pads of a LCD panel with hard materials such as metal or glass or with one's nail.
- To clean the surface , wipe it gently with soft cloth dampened by alcohol.
- Do not attempt to wiped off the contact pads.
- Keep LCD panels away from direct sunlight , also avoid them in high-temperature & high humidity environment for a long period.
- Do not drive LCD panels by DC voltage.
- Do not expose LCD panels to organic solvent.
- Liquid in LCD is hazardous substance. In case a contact with liquid crystal material is occured, be sure to immediately wash such material away by soap and water.
- The polarizer is easily damaged and should be handle with special care. Don't press or rub it with hard objects.

☐ PRECAUTION FOR STORING AND USE OF LCM

- To avoid degradation of the device , do not store the module under the conditions of direct sunlight , high temperature or high humidity . Keep the module in bags designed to prevent static electricity charging under low temperature / normal humidity conditions(avoid high temperature / high humidity and low temperature below 0℃)
- Never use the LCD , LCM under 45 Hz , the liquid crystal will decomposition and cause permently damage on display !!

☐ USING ON MEDICAL CARE , SAFETY OR HAZARDOUS APPLICATION OR SYSTEM

- For the application in medical care, safety and hazardous prodcuts or systems, an authorization from URT is required. URT will not responsible for any damage or loss which caused by the products without any authorization given by URT.
- This product is not allowed to be designed and used for military application and/or purpose.
- The delivery of this product to the countries and/or regions where the embargoes are imposed by U.N. is prohibited.
- The application and delivery of this product must comply with Startegic High-Tech Commodities (SHTC) export control and the sales to the embargoed and/or sanctioned countries or regions are strictly prohibited.

6. DATE CODE OF PRODUCTS

- Date code will be shown on each product :

- **YY MM DD - XXXX**

  Year Month Day - Production lots

- Example: 121108 - 0003 ==> Year 2012, November,8th , Batch no.0003

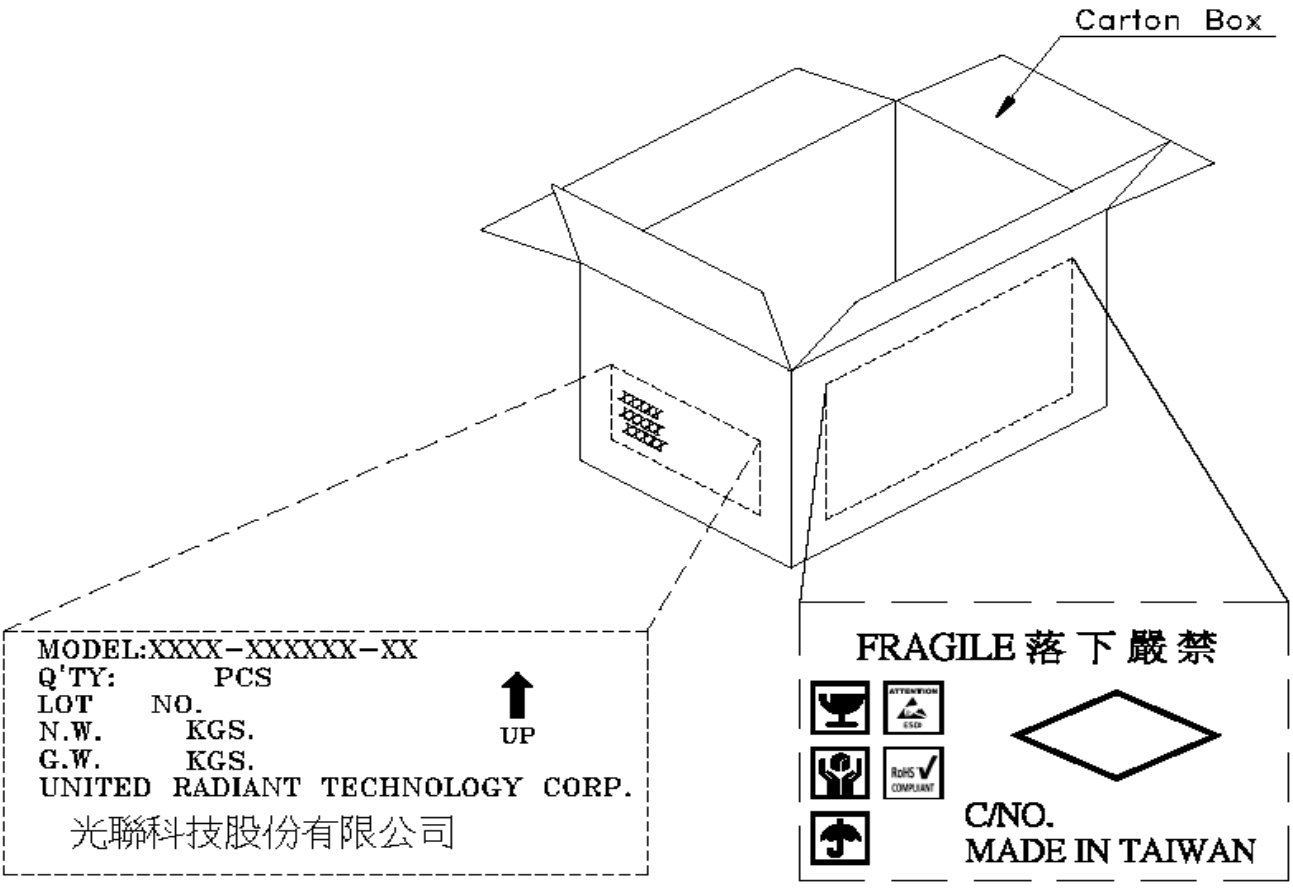
Note ： The lot no. attached on the packing box will be used for tracking once the part is too small to print the date code.

7. LOT NO.

Instruction of lot number:

LOT NO. : 0 0 0 8 3 5 2 5 (EX)

- Date: 01–1 st, 02–2 ed, ... 31–31 th
- Week: 1 ——— 6
- Week of Month: 1 ——— 5
- Month: 01–January, 02–February, ... 12–December
- Year: 00–2000, 01–2001



8. INSPECTION STANDARD

8.1 QUALITY :

THE QUALITY OF GOODS SUPPLIED TO PURCHASER SHALL COME UP TO THE FOLLOWING STANDARD.

8.1.1 THE METHOD OF PRESERVING GOODS

AFTER DELIVERY OF GOODS FROM U.R.T. TO PURCHASER. PURCHASER SHALL CONTROL THE LCM AT -10 ℃ ～ 40 ℃ ,AND IT MIGHT BE DESIRABLE TO KEEP AT THE NORMAL ROOM TEMPERATURE AND HUMIDITY UNTIL INCOMING INSPECTION OR THROWING INTO PROCESS LINE.

8.1.2 INCOMING INSPECTION

(A) THE METHOD OF INSPECTION

IF PURCHASER MAKE AN INCOMING INSPECTION , A SAMPLING PLAN SHALL BE APPLIED ON THE CONDITION THAT QUALITY OF ONE DELIVERY SHALL BE REGARDED AS ONE LOT.

(B) THE STANDARD OF QUALITY

ISO-2859-1 (SAME AS MIL-STD-105E) , LEVEL Ⅱ SINGLE PLAN.

CLASS	AQL(%)
MAJOR	0.65 %
MINOR	1.5 %

EVERY ITEM SHALL BE INSPECTED ACCORDING TO THE CLASS.

(C) MEASURE

IF AS THE RESULT OF ABOVE RECEIVING INSPECTION , A LOT OUT IS DISCOVERED. PURCHASER SHALL BE INFORM SELLER OF IT WITHIN SEVEN DAYS. BUT FIRST SHIPMENT WITHIN FOURTEEN DAYS.

8.1.3 WARRANTY POLICY

U.R.T. WILL PROVIDE ONE-YEAR WARRANTY FOR THE PRODUCTS ONLY IF UNDER SPECIFICATION OPERATING CONDITIONS. U.R.T. WILL REPLACE NEW PRODUCTS FOR THESE DEFECT PRODUCTS WHICH UNDER WARRANTY PERIOD AND BELONG TO THE RESPONSIBILITY OF U.R.T.

8.2 INSPECTION CONDITION IS AS FOLLOWS：

(1) Viewing distance is approximately 35~40 cm

(2) Viewing angle is normal to the LCD panel as Fig-1(30°)

(3) Ambient temperature is approximately 25±5℃

(4) Ambient humidity is 60±5%RH

(5) Ambient illuminance is from 300~500 Lux

(6) Input signal timing should be typical value

(7) Mura & Light leakage inspection an ND-Filter 5%

8.3 Special condtion：

(1) Viewing distance is close for inspection of adjacent dots and distance between defect dots.

(2) Viewing condition of " Shot block non-uniformity from oblique angle"is as Fig-2.

(3) Exceptional case：Veiw angle±40°while inspected image-sticking

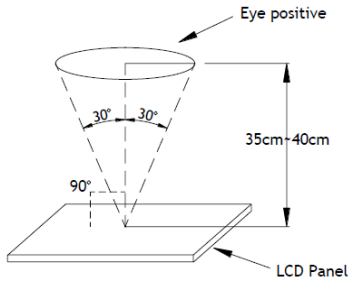


Fig-1

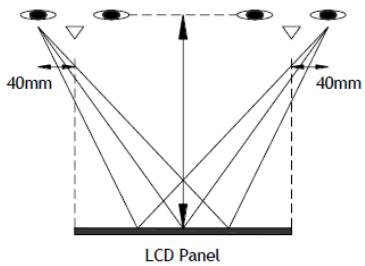
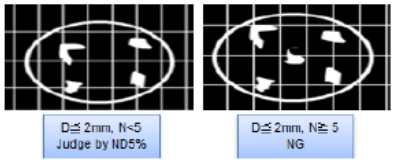


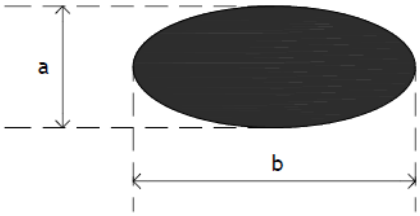
Fig-2

8.4 STANDARD OF VISUAL INSPECTION

Defecttype			Limit			Note
	Scratch		W≦0.05mm		Ignore	Note1
			0.05mm≦w≦0.1mm L≦10mm		N≦3	
			10mm<l, 0.1mm<w		N=0	
	Internal	Spot	Φ < 0.2mm		Ignore	Note1
			0.2mm≦φ≦0.4mm		N≦3	
			0.4≦φ		N=0	
		Fiber	0.1mm ≦W≦0.2mm l≦2.5mm		N≦4	Note1
			0.2mm<w, 2.5mm<l		N=0	
		Polarizer bubble	φ<0.3mm		Ignore	Note1
			0.25mm≦φ≦0.5mm		N≦2	
			0.5mm<φ		N=0	
		Dent	φ<0.25mm		Ignore	Note1
			0.25mm≦φ≦0.5mm		N≦4	
			0.5mm<φ		N=0	
Electrical Defect	Bright dot		C area	O area	Total	Note2 Note3
			N≦0	N≦2	N≦2	
	Dark dot		N≦2	N≦4	N≦4	
	Total dot		N≦2	N≦4	N≦4	
	2 Adjacent Bright Sub Pixel Defect		N≦0	N≦0	N≦0	Note4
	2 Adjacent Dark Sub Pixel Defect		N≦1	N≦1	N≦1	
	Three or more adjacent dot		Not allowed			
	Line defect		Not allowed			-
	Low brightness dot		D>2mm	ND5%		
			D≦2mm	N<5	ND5%	
				N≧5	NG	
			 D≦2mm, N<5 Judge by ND5% D≦2mm, N≧5 NG			

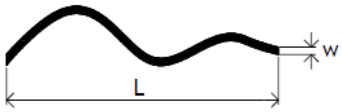
(1) one pixel consists of 3 sub-pixels, including r, g, and b dot. (sub-pixel = dot)
(2) panel is acceptable if distance between 2 dot defects are greater or equal to 5mm.

Note1 : W : Width[mm], L : Length[mm], N : Number, φ: Average Diameter



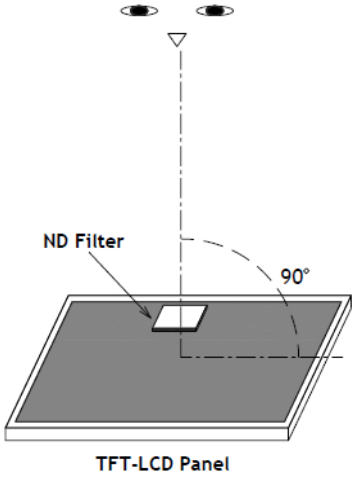
ø=(a+b)/2

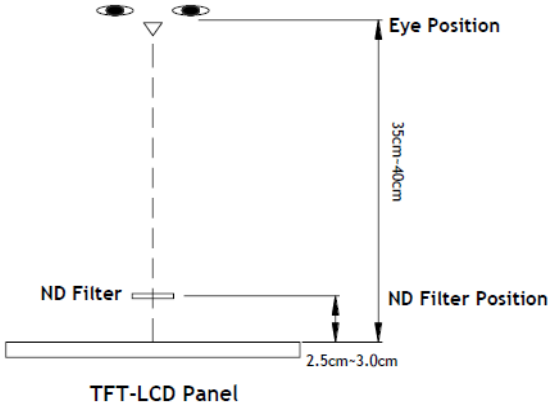
1.(White ,Black) Spot
2.Polarizer Bubble



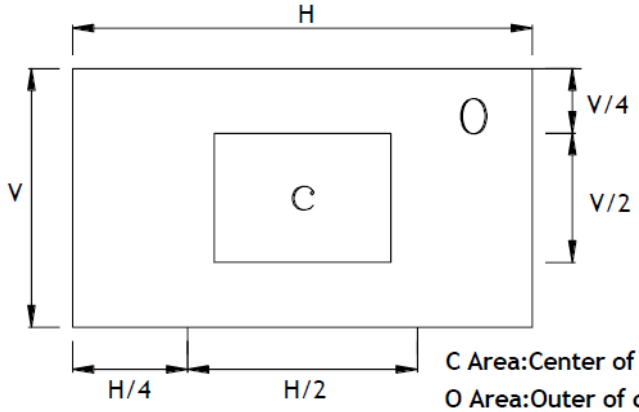
Scratch & Fiber

Note2 : Bright dot is defined as the defective area of the dot is larger than 50% of one sub-Pixel area.





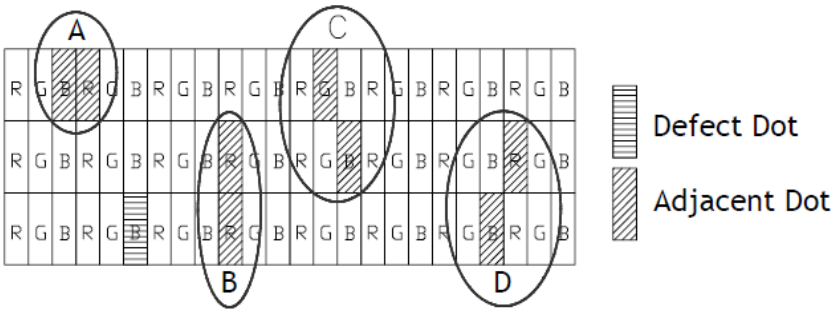
Note3 :



C Area:Center of display area
O Area:Outer of display area

Note4 : Judge defect dot and adjacent dot as following. Allow below (as A, B, C and D status)

adjacent defect dots, including bright and dart adjacent dot. And they will be counted 2defect dots in total quantity.



Note5 : Other condition

(1) The defects that are not defined above and considered to be problem shall be reviewed anddiscussed by both parties.

(2) Defects on the Black Matrix, out of Display area, are not considered as a defect or counted.