晶采光電科技股份有限公司
AMPIRE CO., LTD.

Specifications for LCD module

Customer	
Customer part no.	
Ampire part no.	**AM-7201280KTZQW-01H**
Approved by	
Date	

☐ **Preliminary Specification**
■ **Formal Specification**

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Approved by	Checked by	Organized by
Patrick	Jessica	Lawlite

This Specification is subject to change without notice.

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2022/09/12	-	New Release	Jessica
2022/09/16	4,20	Update storage temperature to -30~75℃	Jessica
20222/11/15	9,10	Update interface	Lawlite
	24,25	Update drawing	
	4,5	Update Electrical Characteristics	
	11	AC Characteristics	
2022/12/05	24,25	Update drawing	Lawlite
	4,20	Update Operating temperature to -20~75℃	

1. General Descriptions

1.1 Introduction

This is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) single chip and sub sheet that use amorphous silicon TFT as a switching device. This TFT LCD panel has a 4.99 inch diagonally measured active display area with HD resolution (720 horizontal by 1280 vertical pixels array).

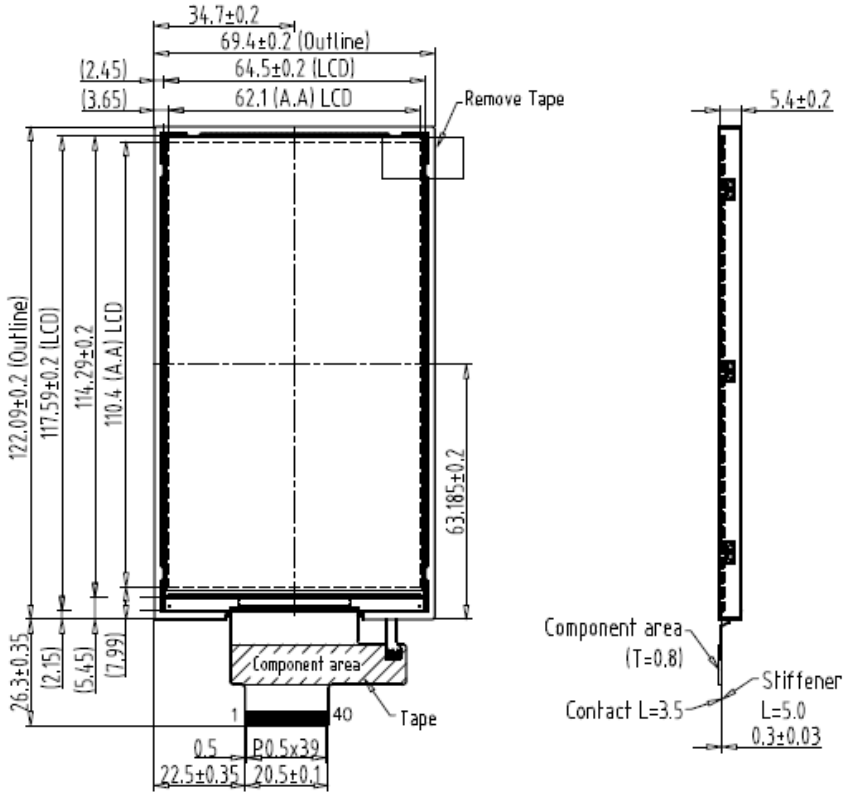
1.2 Features

(1) 4.99 Inch TFT-LCD Panel

(2) MIPI Interface

1.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	5.0	Inch
Number of pixel	720 x 1280	-
Pixel Pitch (H x V)	0.08625 x 0.08625	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Display Mode	Normally Black, IPS	-
White Luminance	**450**(Typ.)	cd /m2
Electrical Interface (Logic)	MIPI	-



2. Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Conditions
System power supply Voltage	IOVCC	-0.3	3.8	V	(1),(2)
Power supply VSP	VSP	-0.3	7.0	V	(1),(2)
Power supply VSN	VSN	-7.0	0.3	V	(1),(2)
Operating Temperature	TOP	**-20**	**75**	℃	(3),(4),(5),(6)
Storage Temperature	TST	**-30**	**80**	℃	

Note(1) All the parameters specified in the table are absolute maximum rating values that may cause faulty operation or unrecoverable damage, if exceeded. It is recommended to follow the typical value.

Note(2) All the contents of electro-optical specifications and display fineness are guaranteed under Normal Conditions. Normal conditions are defined as: Temperature: 25℃, Humidity: 55± 10%RH.

Note(3) Unpredictable results may occur when it was used in extreme conditions. Ta= Ambient Temperature, Tgs= Glass Surface Temperature. All the display fineness should be inspected under normal conditions.

Note(4) Wet bulb temperature should be lower than 58℃, and no condensation of water. Besides, protect the module from static electricity.

3. Electrical Characteristics

3.1 TFT LCD Module

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply voltage	IOVCC	1.65	2.8	3.6	V	
Supply Voltage	VSP	4.5	--	6.6	V	
Supply Voltage	VSN	-4.5	--	-6.6	V	

Note(1) fV =60Hz , Ta=25℃ , Display pattern : All White.

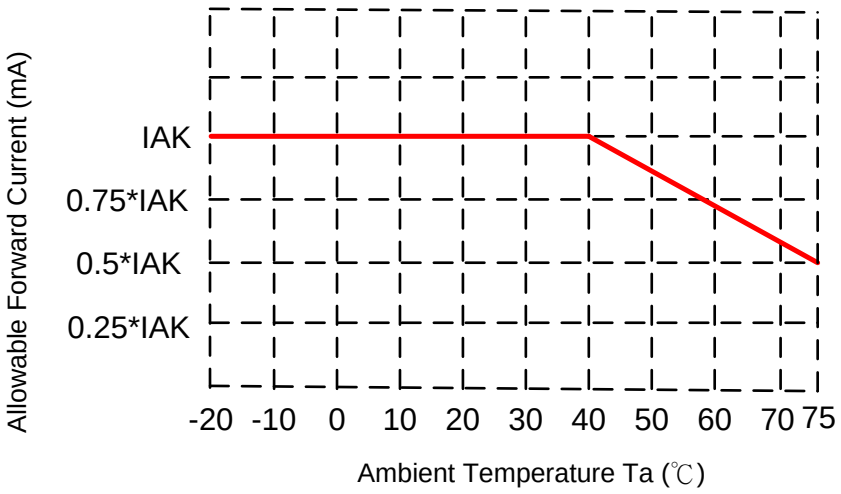
Note(2) *:Will be reference only

3.2 Backlight Unit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
LED Voltage	VAK	16.8	18.0	19.2	V	
LED current	IAK	--	40	--	mA	(2)
Life time	Hrs.	50K	--	--	Hours	(1)(2)

Note(1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3℃, typical IAK value indicated in the above table until the brightness becomes less than 50%.

Note(2) When LCM is operated over 40℃ ambient temperature, the **IAK** should be follow :



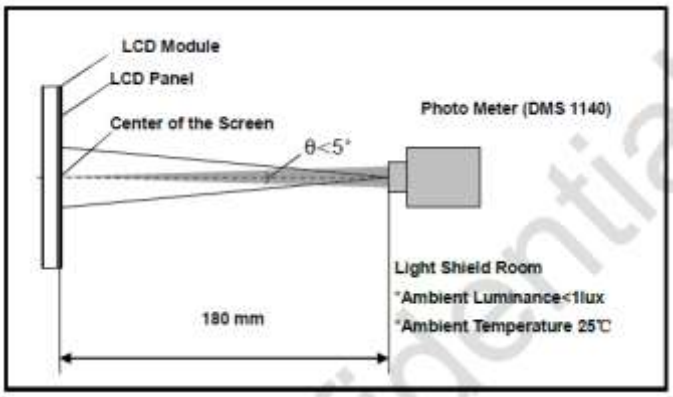
4. Optical Characteristics

The optical characteristics are measured under stable conditions as following notes

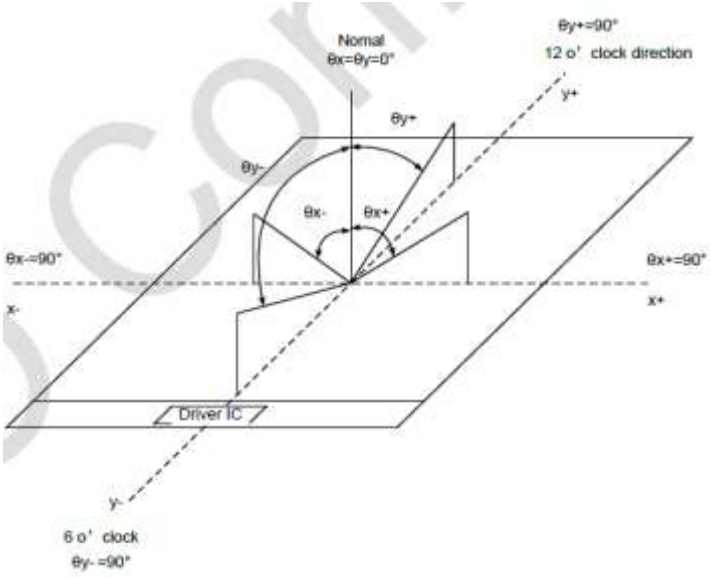
Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle （CR>10）	Horizontal	θ x+	80	85	-	degree	(1),(2)
		θ x-	80	85	-		
	Vertical	θ y+	80	85	-		
		θ y-	80	85	-		
Contrast Ratio	Center		900	1200	-	-	(1),(3) θ x=θ y=0°
Response Time	Rising + Falling		-	35	40	ms	(1),(4),(6),(7),(8) θ x=θ y=0°
NTSC	CIE1931		65	70	-	%	Under C-light (1),(5) θ x=θy=0°
Color Chromaticity (CIE1931)	Red	x	Typ. -0.05	TBD	Typ. +0.05	-	
	Red	y		TBD		-	
	Green	x		TBD		-	
	Green	y		TBD		-	
	Blue	x		TBD		-	
	Blue	y		TBD		-	
	White	x		TBD		-	
	White	y		TBD		-	
White Luminance	Center		**360**	**450**	-	cd/m^2	(1),(2) θx=θy=0°
Luminance Uniformity	9Points		-	TBD	-	%	(1),(2),(6) θx=θy=0°

Note(1) Measurement Setup:

The LCD module should be stabilized at given temperature (25°C) for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 30 minutes in a windless room.



Note(2) Definition of Viewing Angle



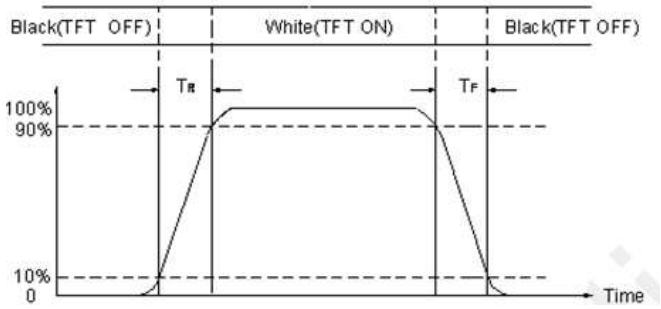
Note(3) Definition Of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression

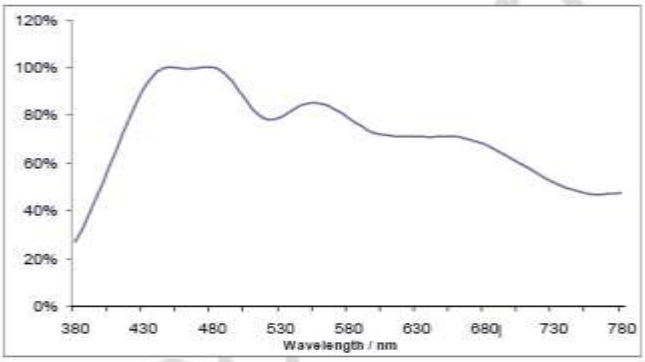
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255, L0: Luminance of gray level 0

Note(4) Definition Of Response Time (TR, TF)



Note(5) Definition of Brightness Luminance



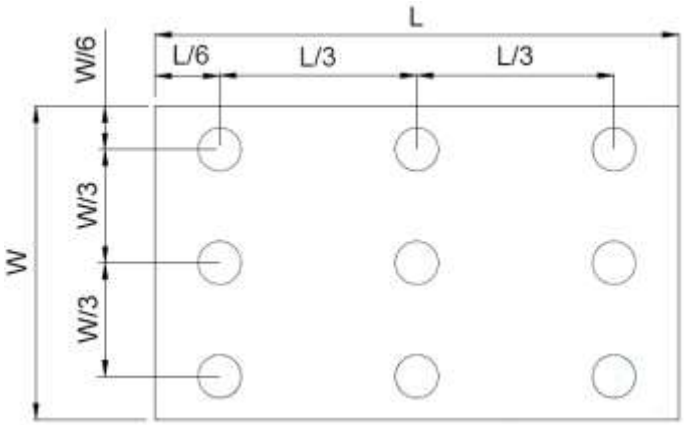
Note(6) Definition of Brightness Luminance

Active area is divided into 9 measuring areas (Refer to bellow figure).

Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity (Yu)} = \frac{\text{Bmin}}{\text{Bmax}}$$

L ----- Active area length W ----- Active area width



Bmax: The measured maximum luminance of all measurement position.

Bmin: The measured minimum luminance of all measurement position.

5. Interface

No.	Symbol	Functions
1	IOVCC(1.8V)	Power input 1.8V for logic power
2	IOVCC(1.8V)	Power input 1.8V for logic power
3	IOVCC(1.8V)	Power input 1.8V for logic power
4	NC	No Connection
5	NC	No Connection
6	NC	No Connection
7	NC	No Connection
8	NC	No Connection
9	GND	Ground
10	DATA2_P (D2_P)	MIPI SDI differential data pair
11	DATA2_N (D2_N)	MIPI SDI differential data pair
12	GND	Ground
13	DATA1_P (D1_P)	MIPI SDI differential data pair
14	DATA1_N (D1_N)	MIPI SDI differential data pair
15	GND	Ground
16	STB_P (CLK_P)	MIPI SDI differential CLK pair
17	STB_N (CLK_N)	MIPI SDI differential CLK pair
18	GND	Ground
19	DATA0_P (D0_P)	MIPI DSI differential data pair
20	DATA0_N (D0_N)	MIPI DSI differential data pair
21	GND	Ground
22	DATA3_P (D3_P)	MIPI SDI differential data pair
23	DATA3_N (D3_N)	MIPI SDI differential data pair
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	GND	Ground
28	TE	Tearing effect output
29	RESET	Reset signal, low active
30	NC	No Connection
31	LEDK	Power for LED backlight cathode

32	LEDK	Power for LED backlight cathode
33	LEDA	Power for LED backlight anode
34	LEDA	Power for LED backlight anode
35	GND	Ground
36	VSN	Power Supply; connect an external power
37	VSN	Power Supply; connect an external power
38	VSP	Power Supply; connect an external power
39	VSP	Power Supply; connect an external power
40	GND	Ground

6. AC Characteristics

6.1 High Speed Mode – Clock Channel Timing

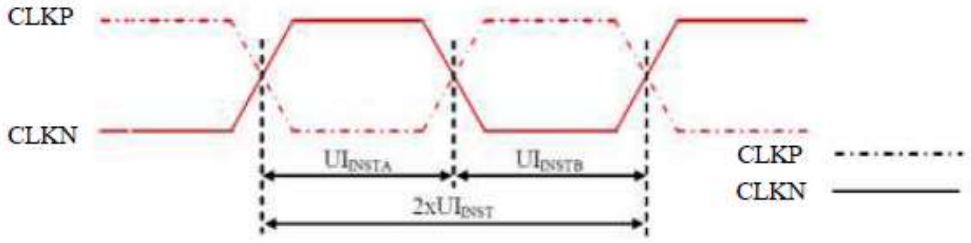


Figure 105: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps

6.2 High Speed Mode – Data Clock Channel Timing

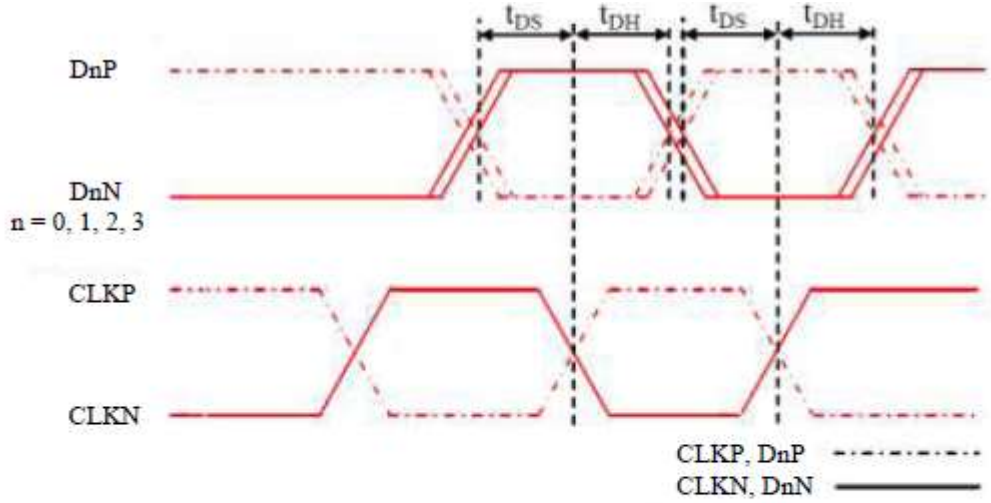


Figure 106: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

6.3 High Speed Mode – Rising and Falling Timings

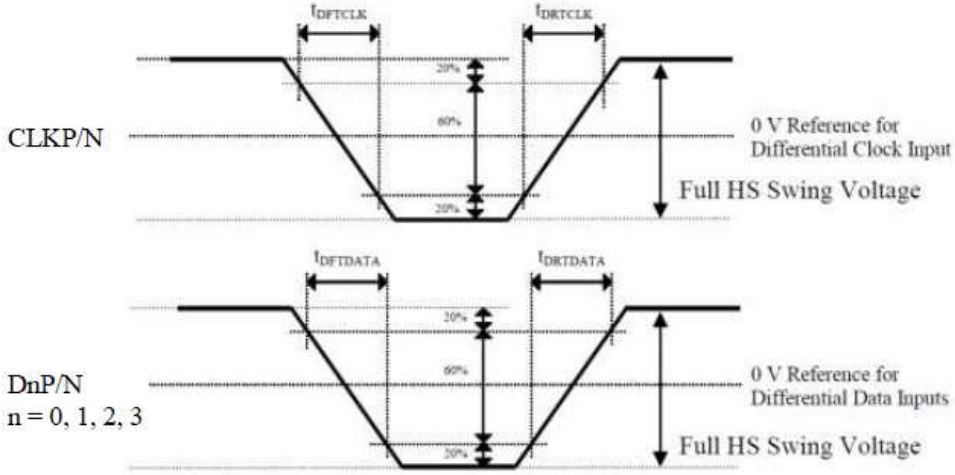


Figure 107: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

6.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module

(ILI9881C-04) are illustrated for reference purposes below

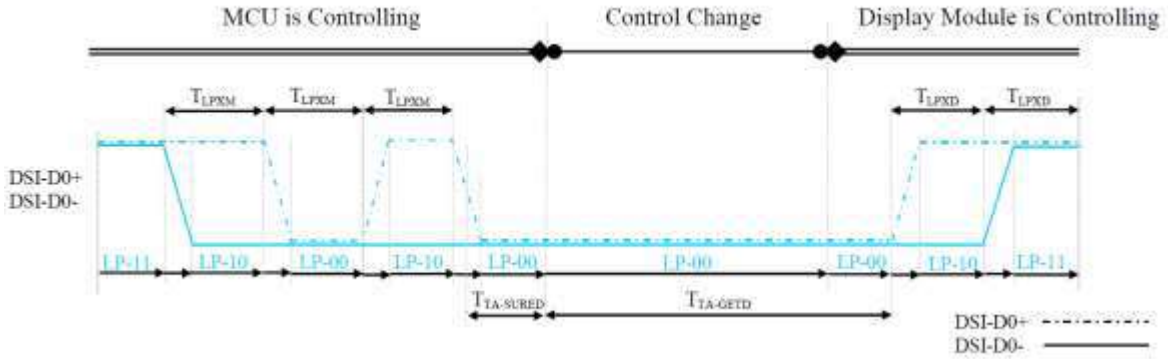


Figure 108: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C-04) to the MCU are illustrated for reference purposes below.

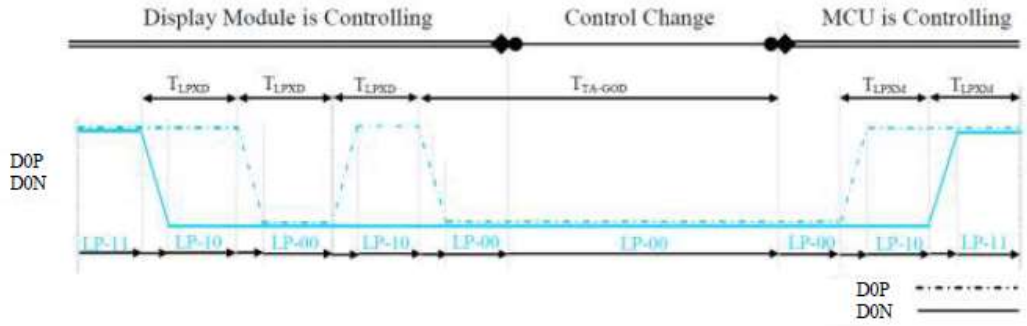


Figure 109: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C-04)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C-04) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C-04) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C-04)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

6.5 Data Lanes from Low Power Mode to High Speed Mode

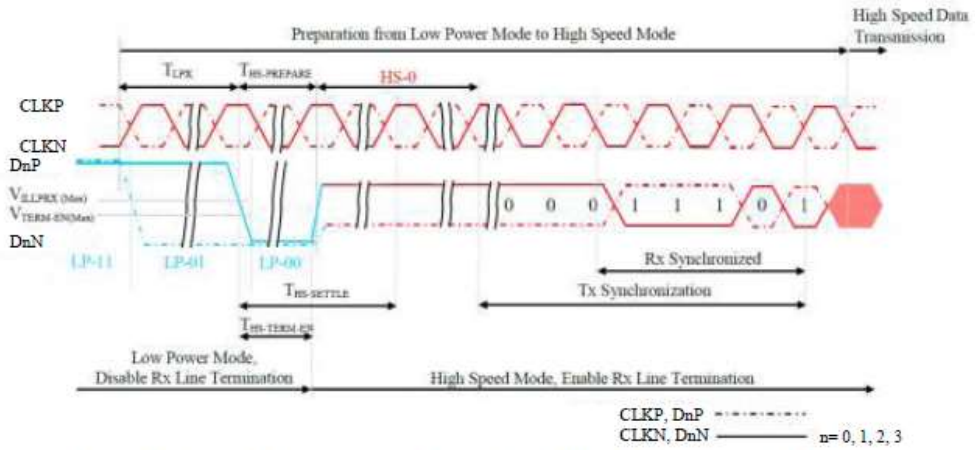


Figure 110: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

6.6 Data Lanes from High Speed Mode to Low Power Mode

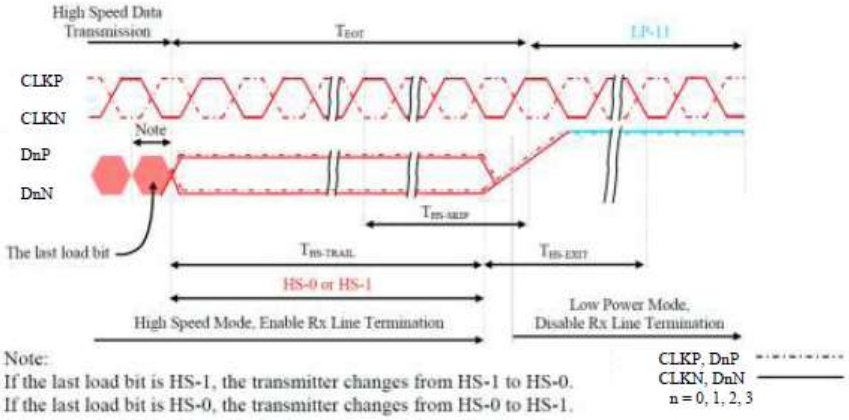


Figure 111: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C-04) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

6.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

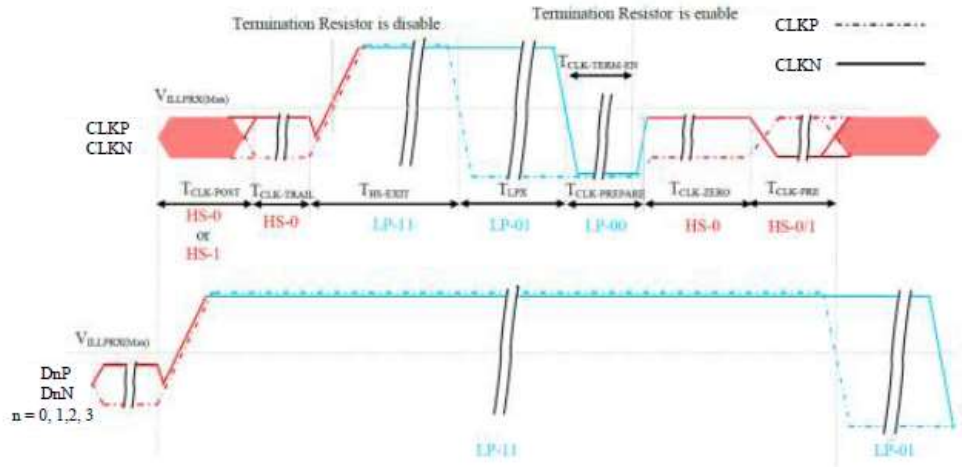
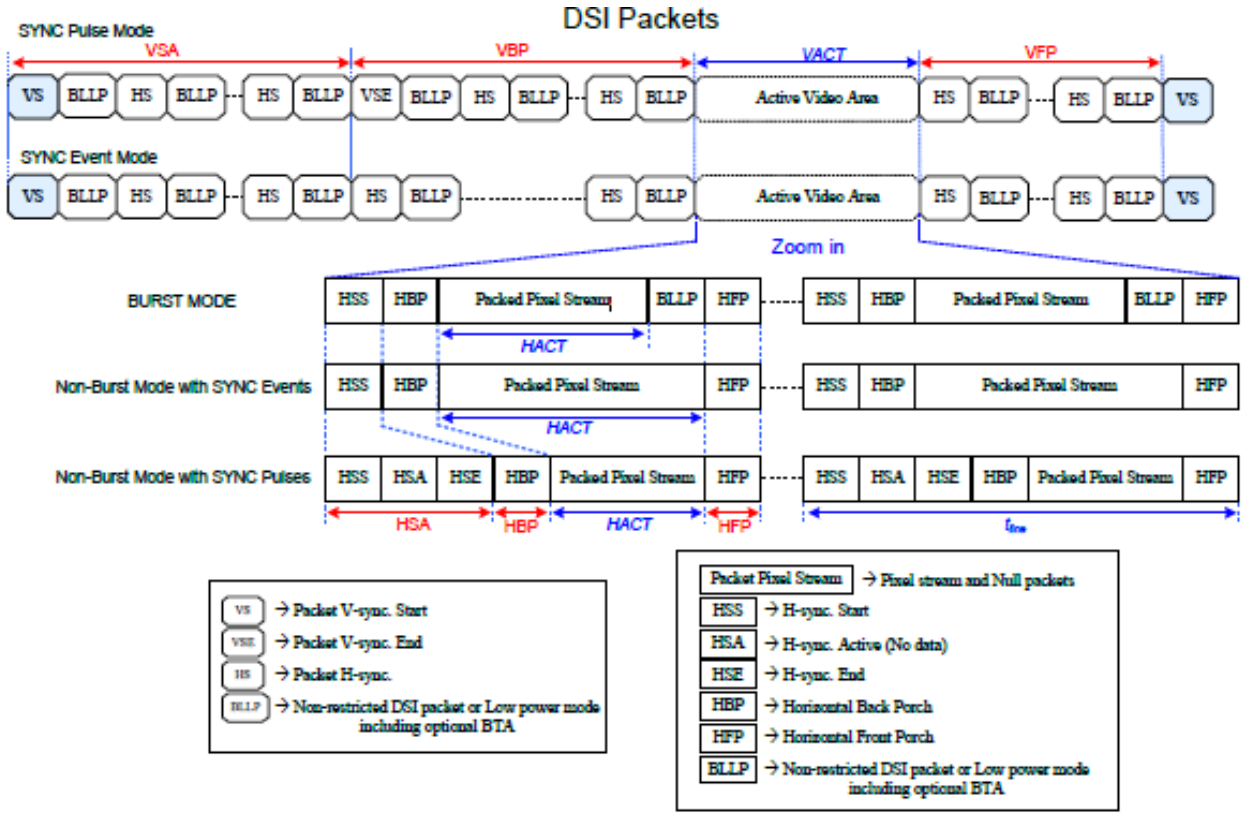


Figure 112: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

6.8 Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example : BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

Note:

1. Lanenum: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.1DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.
5. Please reference to “Table 39: Limited Clock Channel Speed”.
6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values
of VSA, VBP and VFP will be changed by different panel GIP setting.

7. Reliability Conditions

Test Item	Test Conditions	Note
High Temperature Operation	75±3°C , Dry t=240 hrs	
Low Temperature Operation	-20±3°C , Dry t=240 hrs	
High Temperature Storage	80±3°C , Dry t=240 hrs	1,2
Low Temperature Storage	-30±3°C , Dry t=240 hrs	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note(1) Condensation of water is not permitted on the module.

Note(2) The module should be inspected after 1 hour storage in normal conditions (15-35°C, 45-65%RH).

Note(3) The module shouldn't be tested more than one condition, and all the test conditions are independent.

Note(4) All the reliability tests should be done without protective film on the module.

Definitions of life end point:

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

8. Use Precautions

8.1 Handling precautions

(1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
(2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
(3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
(4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

8.2 Installing precautions

(1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
(2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
(3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
(4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

8.3 Storage precautions

(1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
(2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
(3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

8.4 Operating precautions

(1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
(2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
(3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
(4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
(5) Make certain that each signal noise level is within the standard (L level: 0.2 IOVCC or less and H level: 0.8 IOVCC or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
(6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
(7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

(8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

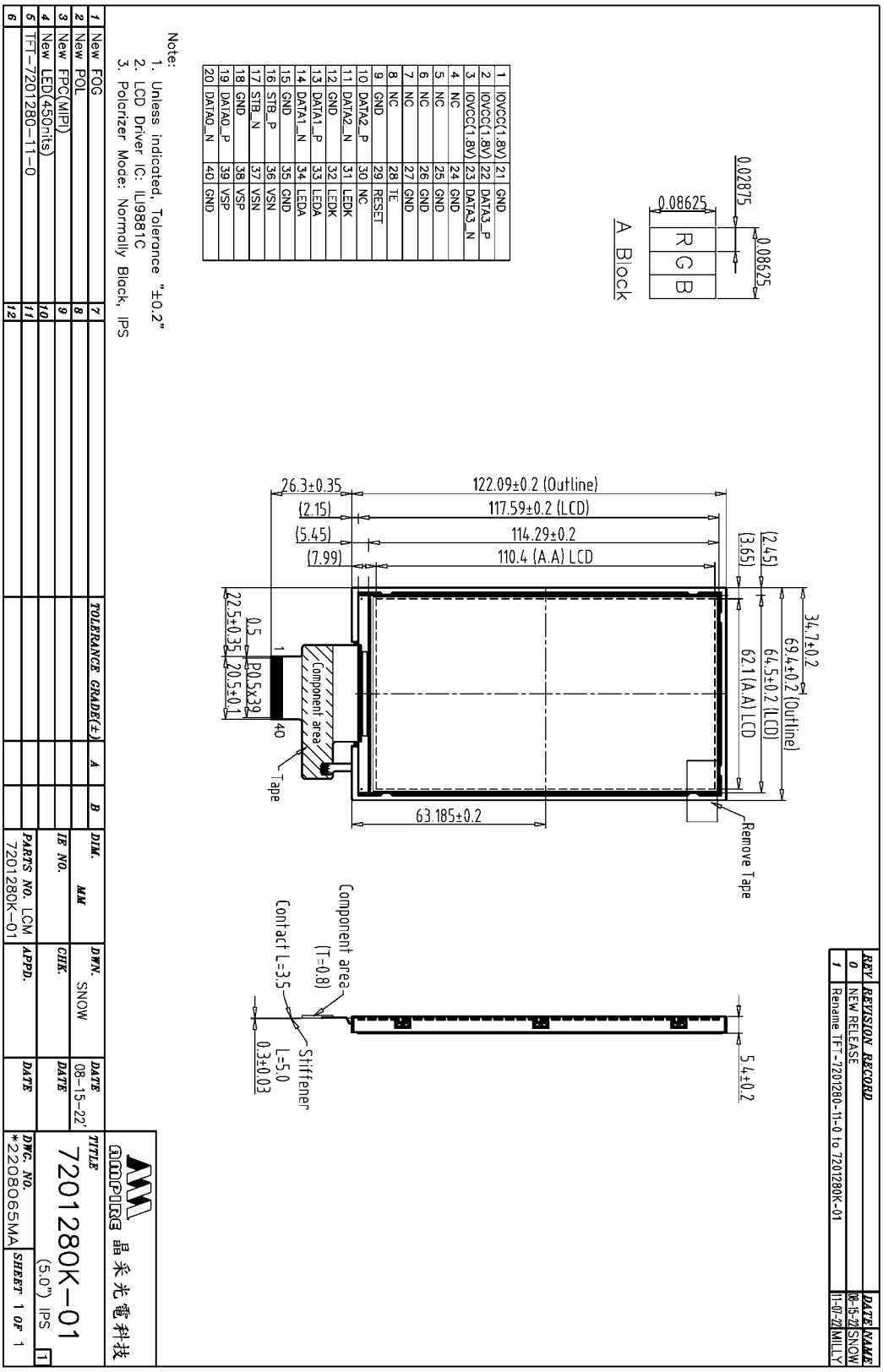
8.5 Mechanism

(1) Please mount LCD module by using mounting holes arranged in four corners tightly.

8.6 Other

(1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
(2) Do not keep the LCD at the same display pattern continually. The residual image will happen and it will damage the LCD. Please use screen saver
(3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

9. Outline Dimension



1	IOVCC(1.8V)	21	GND
2	IOVCC(1.8V)	22	DATA3_P
3	IOVCC(1.8V)	23	DATA3_N
4	NC	24	GND
5	NC	25	GND
6	NC	26	GND
7	NC	27	GND
8	NC	28	TE
9	GND	29	RESET
10	DATA2_P	30	NC
11	DATA2_N	31	LEDK
12	GND	32	LEDK
13	DATA1_P	33	LEDA
14	DATA1_N	34	LEDA
15	GND	35	GND
16	STB_P	36	VSN
17	STB_N	37	VSN
18	GND	38	VSP
19	DATA0_P	39	VSP
20	DATA0_N	40	GND

REV	REVISION RECORD	DATE	NAME
0	NEW RELEASE	18-12-29	SNOW
1	Rename TFT-7201280-11-0 to 7201280K-01	11-07-22	MILLY

1	New FOG	7							
2	New POL	8							
3	New FPC(MIPI)	9							
4	New LED(450nits)	10							
5	TFT-7201280-11-0	11							
6		12							

TOLERANCE GRADE(±)	A	B
DIM. MM		
IE NO.		
PARTS NO. LCM 7201280K-01		

DWN.	SNOW	08-15-22'
CHK.		DATE
APPD.		DATE

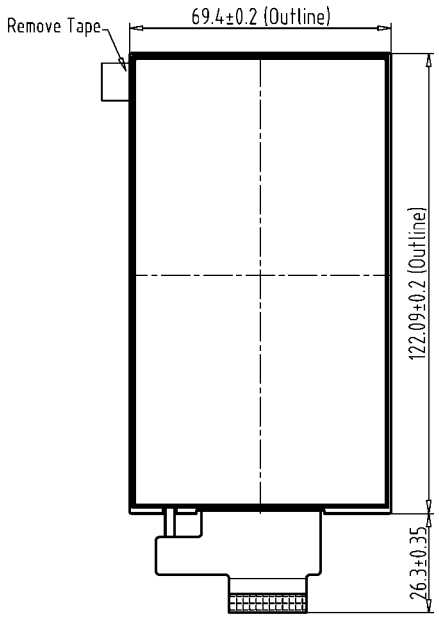
AMPIRE 晶采光電科技

TITLE: 7201280K-01 (5.0") IPS 1

DWG. NO. *2208065MA

SHEET 1 OF 1

REV	REVISION RECORD	DATE	NAME
0	NEW RELEASE	08-15-22	SNOW
1	Rename TFT-7201280-11-0 to 7201280K-01	11-07-22	MILLY



Back View

1	IOVCC(1.8V)	21	GND
2	IOVCC(1.8V)	22	DATA3_P
3	IOVCC(1.8V)	23	DATA3_N
4	NC	24	GND
5	NC	25	GND
6	NC	26	GND
7	NC	27	GND
8	NC	28	TE
9	GND	29	RESET
10	DATA2_P	30	NC
11	DATA2_N	31	LEDK
12	GND	32	LEDK
13	DATA1_P	33	LEDA
14	DATA1_N	34	LEDA
15	GND	35	GND
16	STB_P	36	VSN
17	STB_N	37	VSN
18	GND	38	VSP
19	DATA0_P	39	VSP
20	DATA0_N	40	GND

Note:
1. Unless indicated, Tolerance "±0.2"
2. LCD Driver IC: ILI9881C
3. Polarizer Mode: Normally Black, IPS

1	New FOG	7		TOLERANCE GRADE(±)	A	B	DIM. MM	DWN. SNOW	DATE 08-15-22'	TITLE 7201280K-01 (5.0") IPS 1
2	New POL	8					IE NO.	CHK.	DATE	
3	New FPC(MIPI)	9								
4	New LED(450nits)	10								
5	TFT-7201280-11-0	11					PARTS NO. LCM-1 7201280K-01	APPD.	DATE	DWG. NO. *2208066MA SHEET 1 OF 1
6		12								

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AMPIRE CO., LTD.

Date: 2022/12/05

10. Package
TBD