



晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AM-19201080NTZQW-00
APPROVED BY	
DATE	

☐ Approved For Specifications

☐ Approved For Specifications & Sample

AMPIRE CO., LTD.

**4F., No.116, Sec. 1, Xintai 5th Rd., Xizhi Dist., New Taipei City 221,
Taiwan (R.O.C.)**

22181 新北市 汐止區 新台五路一段 116 號 4 樓(東方科學園區 A 棟)

TEL:886-2-26967269 , FAX:886-2-26967196 or 26967270

APPROVED BY	CHECKED BY	ORGANIZED BY

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2018/12/20	--	New Release	Raymond

1. Features

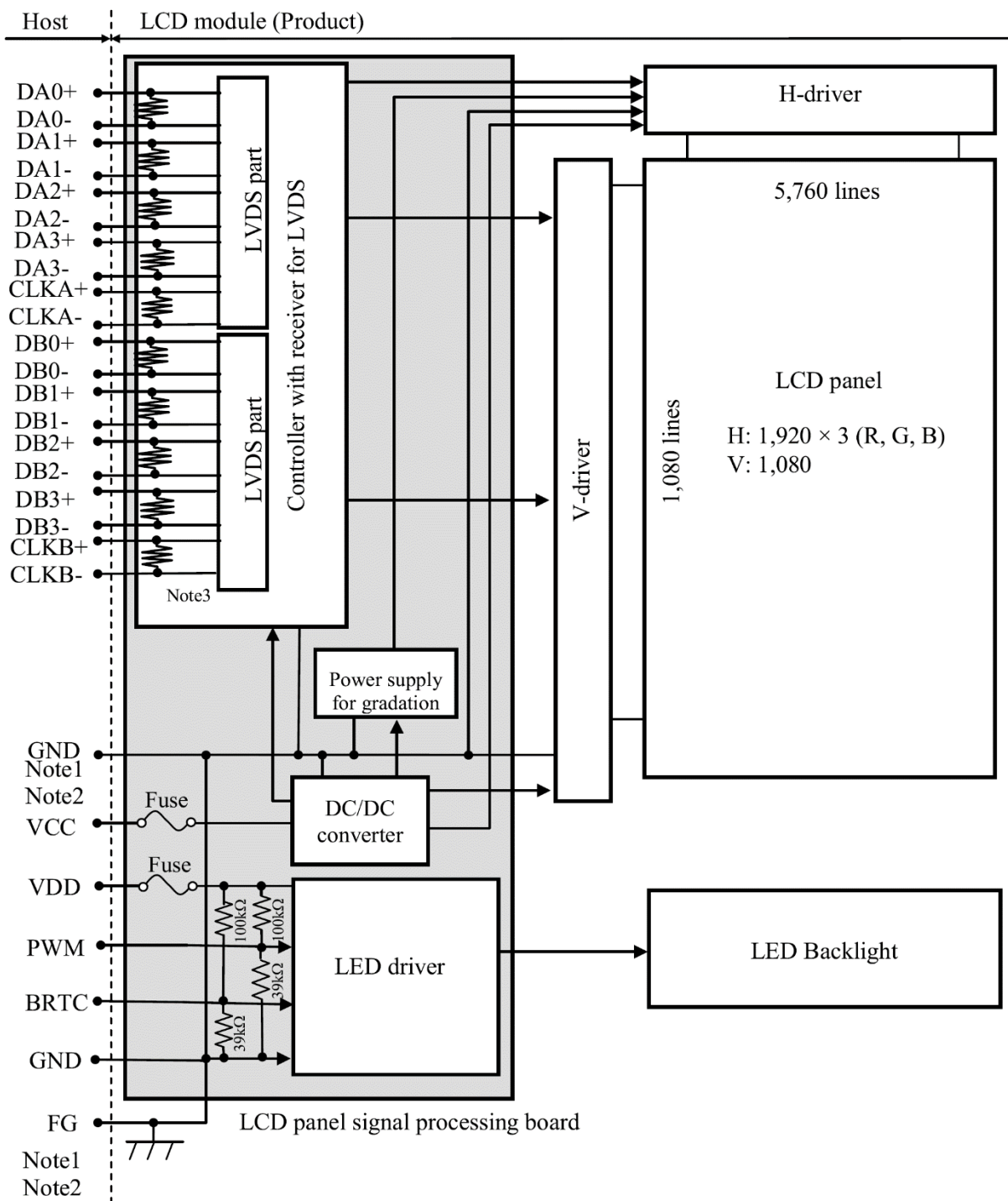
15.6 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module. This module is composed of a 15.6" TFT-LCD panel and LED backlight and LED driving board.

- (1) Construction: 15.6" a-Si TFT active matrix, White LED Backlight.
- (2) Resolution (pixel): 1920(R.G.B) X 1080
- (3) Number of the Colors : 16.7M colors (R , G , B 8 bit digital each)
- (4) LCD type :SFT with Normally Black

2. PHYSICAL SPECIFICATIONS

Item	Specifications	unit
LCD size	15.6 inch (Diagonal)	
Resolution	1920 x (RGB) x 1080	dot
Dot pitch	0.05975(H) x 0.17925(V)	mm
Active area	344.16(W) x 193.59(H)	mm
Module size	363.8(W) x 215.9(H) x 6.3(D)	mm
Surface treatment(Up Polarizer)	Antiglare	
Color arrangement	RGB-stripe	
Contrast Ratio	1000:1	
Brightness	400	cd/m ²

3. BLOCK DIAGRAM



Note 1: Relation between GND (Signal ground and LED driver ground) and FG (Frame ground) in the LCD module is as follows.

GND-FG	Connected
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Note 2: GND and FG must be connected to customer equipment's ground, and it is recommended that these grounds to be connected together in customer equipment.

Note 3: Each pair of the LVDS signal has a 100Ω terminating resistance.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	363.8 ± 0.5 (W) x 215.9 ± 0.5 (H) x 6.3 ± 0.5 (D)	mm
Display area	344.16 (H) x 193.59 (V)	mm
Weight	610 (typ.), 670 (max.)	g

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VCC	-0.3 to +4.0	V	Ta = 25°C
	LED driver	VDD	-0.3 to +15.0	V	
Input voltage for signals	Display signals Note1	VD	-0.3 to VCC+0.3	V	
	Function signal for LED driver	PWM	-0.3 to +5.5	V	
		BRTC	-0.3 to +5.5	V	
Storage temperature		Tst	-20 to +70	°C	-
Operating temperature	Front surface	TopF	-20 to +70	°C	Note2
	Rear surface	TopR	-20 to +70	°C	Note3
Relative humidity Note4		RH	≤ 95	%	Ta ≤ 40°C
			≤ 85	%	40°C < Ta ≤ 50°C
			≤ 55	%	50°C < Ta ≤ 60°C
			≤ 36	%	60°C < Ta ≤ 70°C
Absolute humidity Note4		AH	≤ 70 Note5	g/m³	Ta = 70°C

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CLKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CLKB+/-

Note2: Measured at LCD panel surface (including self-heat)

Note3: Measured at LCD module's rear shield surface (including self-heat)

Note4: No condensation

Note5: Water amount at Ta= 70°C and RH= 36%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VCC	3	3.3	3.6	V	-
Power supply current		ICC	-	530 Note1	1,000 Note2	mA	at VCC= 3.3V
Permissible ripple voltage		VRPC	-	-	100	mVp-p	for VCC Note3, Note4, Note5
Differential input threshold voltage	High	VTH	-	-	100	mV	at VCM= 1.2V Note6, Note7
	Low	VTL	-100	-	-	mV	
Input Differential Voltage		VID	100	400	600	mV	-
Differential Input Common Mode Voltage		VCM	0.7	1.2	1.6	V	-
Terminating resistance		RT	-	100	-	W	-

Note1: Checkered flag pattern [by IEC 61747-6]

Note2: Pattern for maximum current.

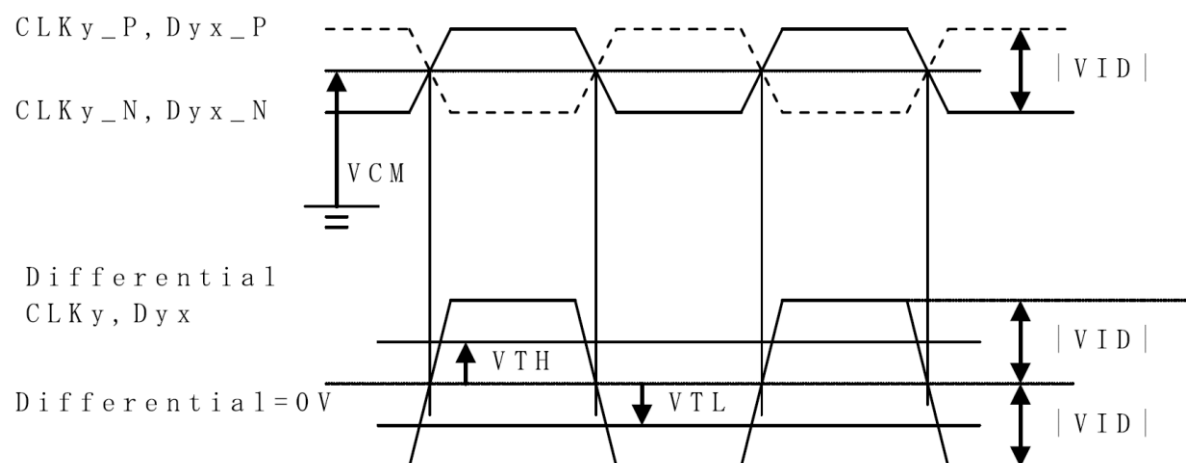
Note3: This product works even if the ripple voltage levels are over the permissible values, but there might be noise on the display image.

Note4: The permissible ripple voltage includes spike noise.

Note5: The load variation influence does not include.

Note6: Common mode voltage for LVDS receiver.

Note7: DC characteristics (LVDS receiver part)



$CLKy_P, CLKy_N$: $y = A, B$

Dyx_P, Dyx_N : $y = A, B$ $x = 0, 1, 2, 3$

$|VID| = |**_P - **_N|$

$V_{CM} = (**_P + **_N) / 2$

P: +, N: -

** : CLKy or Dyx

4.3.2 LED driver

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply voltage		VDD	10.8	12	13.2	V	Note1
Power supply current		IDD	-	1,000	1,400 Note2	mA	at VDD= 12.0V Note3
Permissible ripple voltage		VRPD	-	-	200	mVp-p	for VDD Note4, Note5, Note6
Input voltage for PWM signal	High	VDFH1	2	-	5	V	Note7
	Low	VDFL1	0	-	0.4	V	
Input voltage for BRTC signal	High	VDFH2	2	-	5	V	
	Low	VDFL2	0	-	0.8	V	
Input current for PWM signal	High	IDFH1	-	-	300	mA	
	Low	IDFL1	-300	-	-	mA	
Input current for BRTC signal	High	IDFH2	-	-	300	mA	
	Low	IDFL2	-300	-	-	mA	
PWM frequency		f _{PWM}	200	-	1k	Hz	Note8, Note9
PWM duty ratio		DR _{PWM}	1	-	100	%	Note10, Note11
PWM pulse width		t _{PWH}	20	-	-	ms	

Note1: When designing of the power supply, take the measures for the prevention of surge voltage.

Note2: This value excludes peak current such as overshoot current.

Note3: At the maximum luminance control

Note4: The power supply lines (VDD and GND) may have ripple voltage during luminance control of LED. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on.

Note5: This product works even if the ripple voltage levels are over the permissible values, but there might be noise on the display image.

Note6: The permissible ripple voltage includes spike noise.

Note7: See "3. BLOCK DIAGRAM".

Note8: A recommended f_{PWM} value is as follows.

$$f_{PWM} = \frac{2n - 1}{4} \times f_v$$

(n = integer, f_v = frame frequency of LCD module)

Note9: Depending on the frequency used, some noise may appear on the screen, please conduct a thorough evaluation.

Note10: While the BRTC signal is high, do not set the t_{PWH} (PWM pulse width) is less than minimum value. It may cause abnormal working of the backlight. In this case, turn the backlight off and then on again by BRTC signal.

Note11: Regardless of the PWM frequency, both PWM duty ratio and PWM pulse width must be always more than the minimum values.

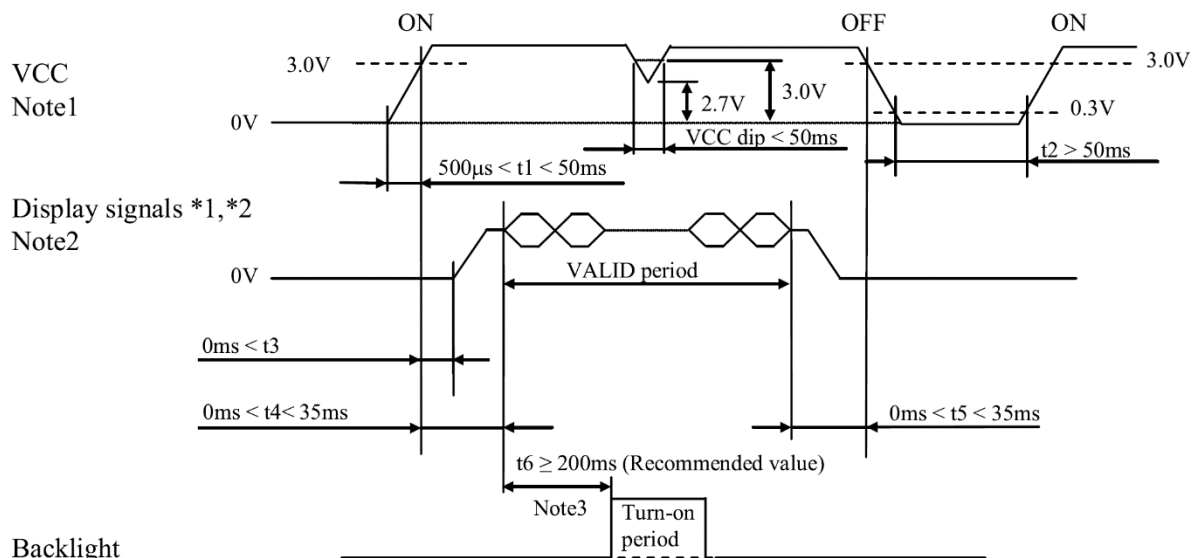
4.3.3 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VCC	FCC16152AB	KAMAYA ELECTRIC CO.,LTD	1.5A	3.0A 5 seconds	Note1
			36V		
VDD	FCC16202AB	KAMAYA ELECTRIC CO.,LTD	2.0A	4.0A 5 seconds	
			36V		

Note1: The power supply's rated current must be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board



*1 DA0+/-, DA1+/-, DA2+/-, DA3+/-, CLKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CLKB+/-

*2 These signals should be measured at the terminal of 100Ω resistance.

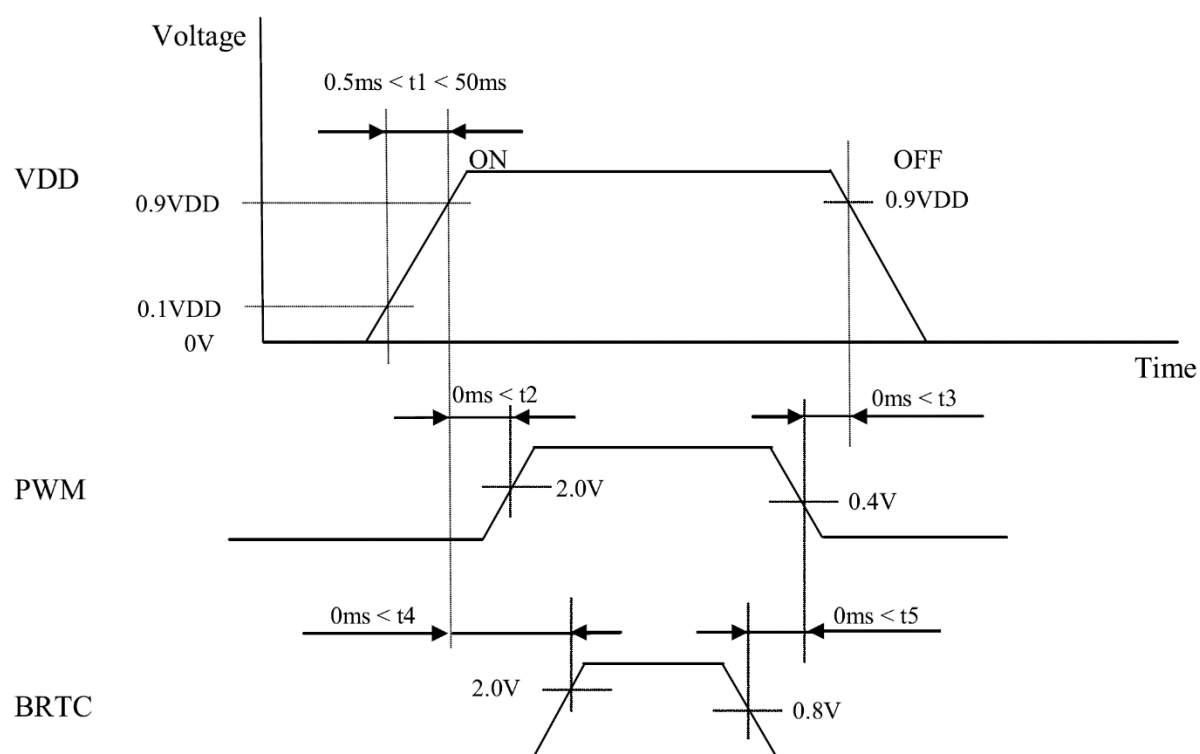
Note1: If there is a voltage variation (voltage drop) at the rising edge of VCC below 3.0V, there is a possibility that a product does not work due to a protection circuit.

Note2: Display signals (DA0+/-, DA1+/-, DA2+/-, DA3+/-, CLKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CLKB+/-) must be set to Low or High-impedance, except the VALID period (See above sequence diagram), in order to avoid the circuitry damage. If some of display signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. If a customer stops the display signals, VCC also must be shut down.

Note3: In order to avoid unstable data display, the backlight is recommended to turn on within the VALID period of display and function signals.

Recommended value: $t6 \geq 200ms$

4.4.2 LED driver



4.5 Interface

4.5.1 LCD panel signal processing board

CN1 socket (LCD module side) : MDF76KBW-30S-1H(55) (HIROSE ELECTRIC Co., Ltd.)

Adaptable plug : MDF76-30P-1C (HIROSE ELECTRIC Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	DA0-	Odd pixel data 0	Note1
2	DA0+		
3	DA1-	Odd pixel data 1	Note1
4	DA1+		
5	DA2-	Odd pixel data 2	Note1
6	DA2+		
7	GND	Ground	Note2
8	CLKA-	Odd pixel clock	Note1
9	CLKA+		
10	DA3-	Odd pixel data 3	Note1
11	DA3+		
12	DB0-	Even pixel data 0	Note1
13	DB0+		
14	GND	Ground	Note2
15	DB1-	Even pixel data 1	Note1
16	DB1+		
17	GND	Ground	Note2
18	DB2-	Even pixel data 2	Note1
19	DB2+		
20	CLKB-	Even pixel clock	Note1
21	CLKB+		
22	DB3-	Even pixel data 3	Note1
23	DB3+		
24	GND	Ground	Note2
25	GND	Ground	Note2
26	GND	Ground	Note2
27	GND	Ground	Note2
28	VCC	Power supply	Note2
29			
30			

Note1: Twist pair wires with 100Ω(Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note2: All GND and VCC terminals should be used without any non-connected lines.

4.5.2 LED driver

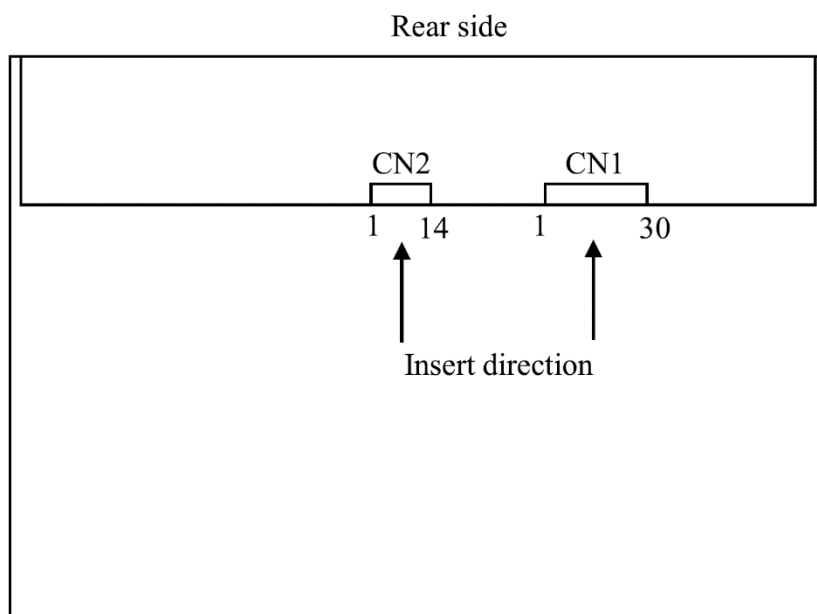
CN2 socket (LCD module side) : DF19L-14P-1H(54)(HIROSE ELECTRIC Co., Ltd.)

Adaptable plug : DF19-14S-1C (HIROSE ELECTRIC Co., Ltd.)

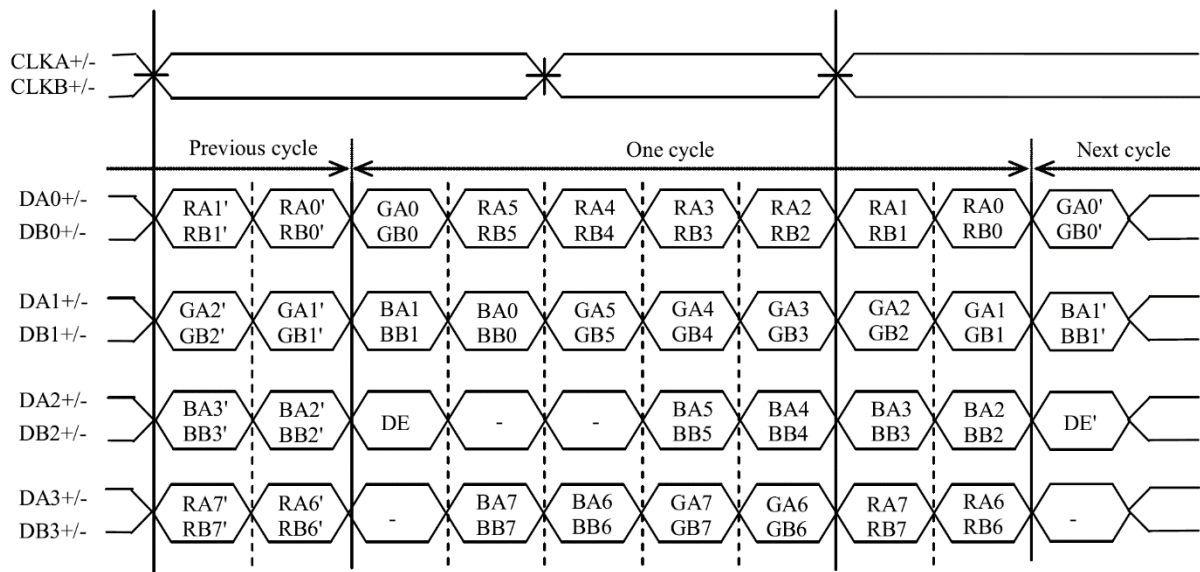
Pin No.	Symbol	Function	Description
1	VDD	Power supply	Note1
2	VDD		
3	VDD		
4	VDD		
5	VDD		
6	GND	LED driver ground	Note1
7	GND		
8	GND		
9	GND		
10	GND		
11	RSVD	Keep this pin open.	-
12	BRTC	Backlight ON/OFF control	High or Open: Backlight ON Low: Backlight OFF
13	PWM	Luminance control	PWM dimming
14	GND	LED driver ground	Note1

Note1: All VDD and GND terminals should be used without any non-connected lines.

4.5.3 Positions of socket



4.5.3 Input data mapping



Note1: LSB (Least Significant Bit) – R0, G0, B0 MSB (Most Significant Bit) – R7, G7, B7

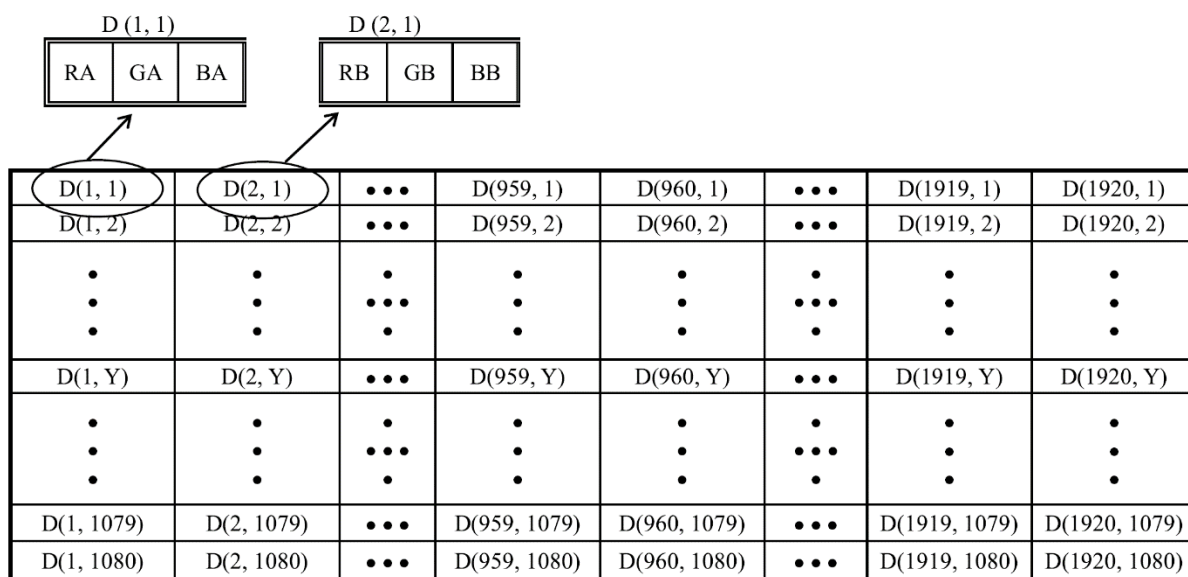
Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

4.6 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display equivalent of 16,777,216 colors with 256 gray scales. Also the relation between display colors and input data signals is as follows.

Display colors		Data signal (0: Low level, 1: High level)																							
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑				:	:						:	:							:	:				
	↓				:	:						:	:							:	:				
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green gray scale		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Blue gray scale	↑				:	:						:	:							:	:				
	↓				:	:						:	:							:	:				
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

4.7 DISPLAY POSITIONS

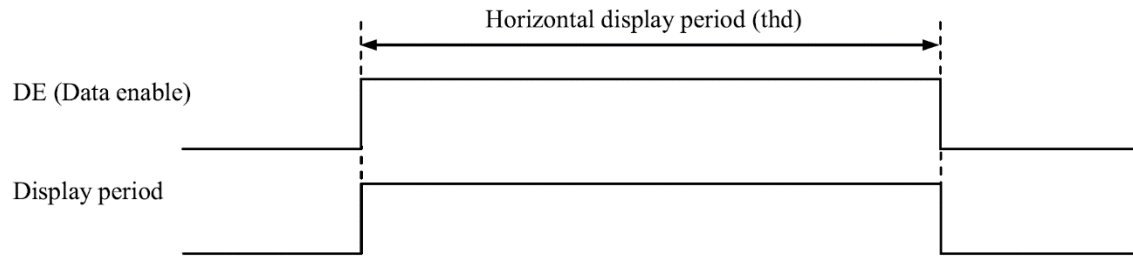


4.8 INPUT SIGNAL TIMINGS

4.8.1 Outline of input signal timings

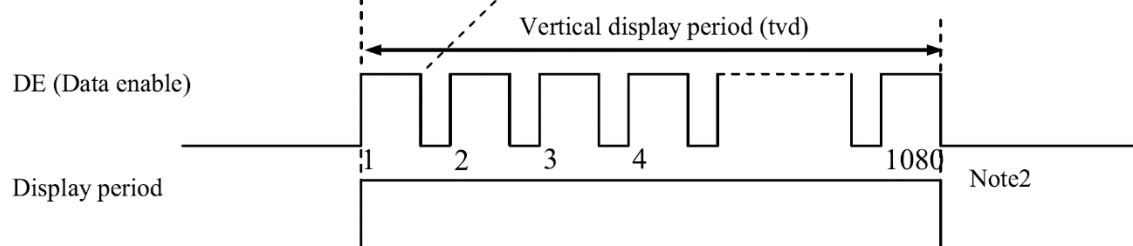
- Horizontal signal

Note1



- Vertical signal

Note1



Note1: This diagram indicates virtual signal for set up to timing.

Note2: See "4.8.3 Input signal timing chart" for the pulse number.

4.8.2 Timing characteristics

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency		1/tc	65	74.175	81.5	MHz	13.48ns (typ.)
	Duty ratio		-	-			-	-
	Rise time, Fall time		-				ns	
DATA	CLK-DATA	Setup time	-	-			ns	-
		Hold time	-				ns	
	Rise time, Fall time		-				ns	
DE	Horizontal	Cycle	th	13.19	14.83	16.53	us	67.43kHz (typ.)
				1,075	1,100	-	CLK	
		Display period	thd	960			CLK	-
	Vertical (One frame)	Cycle	tv	15.39	16.68	18.18	ms	59.94Hz (typ.)
				1,100	1,125	-	H	
		Display period	tvd	1,080			H	-
	CLK-DE	Setup time	-	-			ns	-
		Hold time	-				ns	
	Rise time, Fall time		-				ns	

Note1: Definition of parameters is as follows.

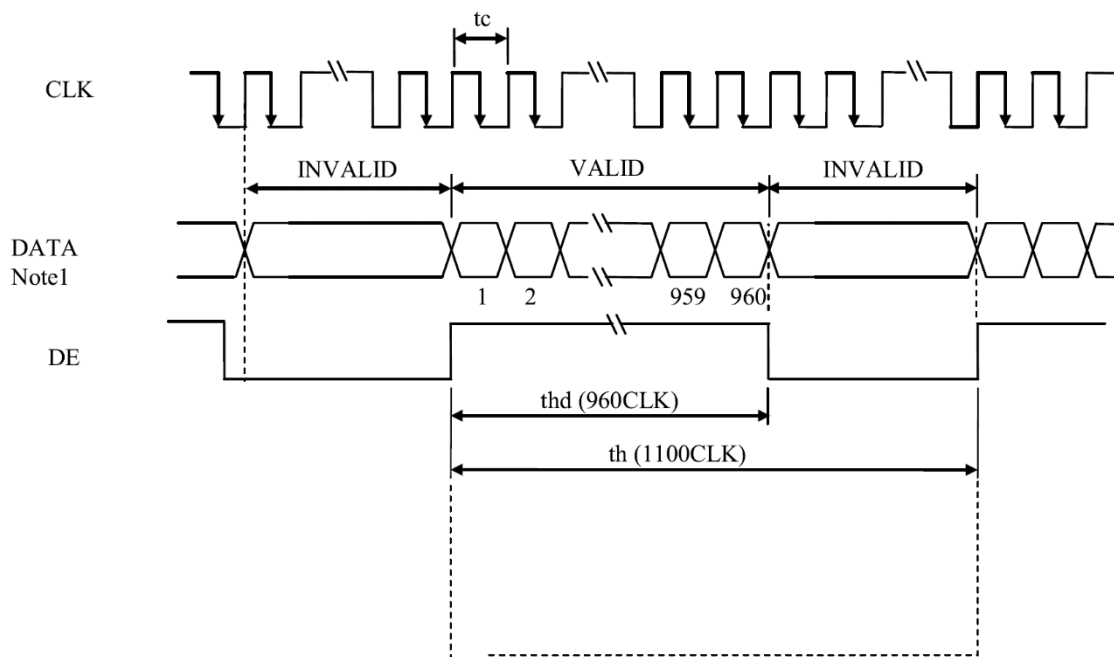
tc= 1CLK, th= 1H

Note2: See the data sheet of LVDS transmitter.

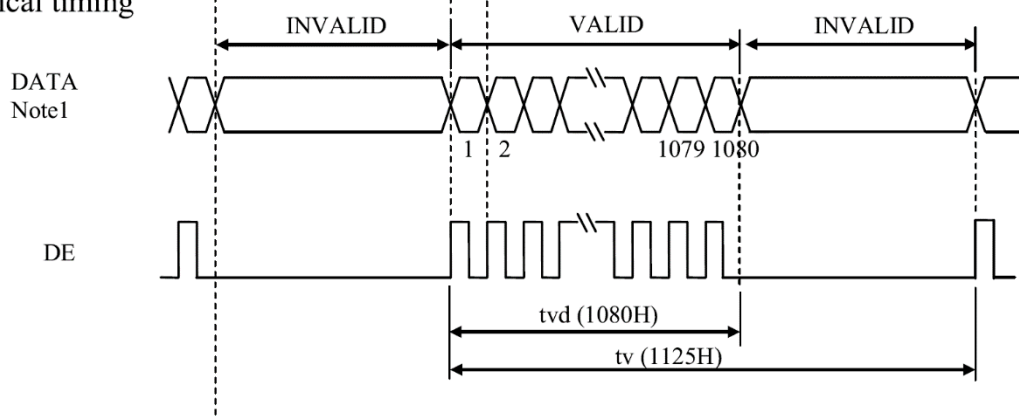
Note3: Vertical cycle (tv) should be specified in integral multiple of Horizontal cycle (th).

4.8.3 Input signal timing chart

Horizontal timing



Vertical timing

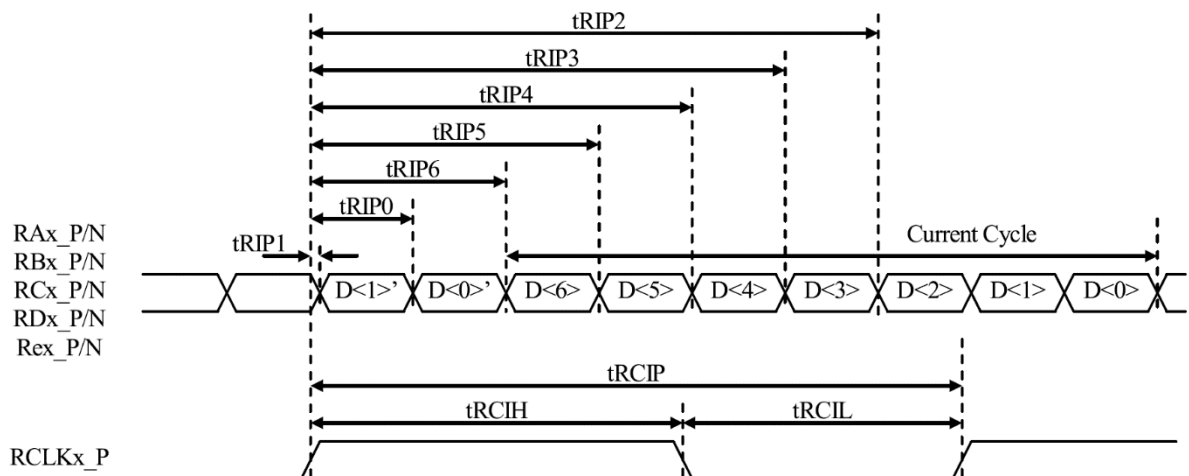


Note1: DATA (A) = RA0-RA7, GA0-GA7, BA0-BA7

DATA (B) = RB0-RB7, GB0-GB7, BB0-BB7

4.9 LVDS Rx AC SPEC

Symbol	Parameter	min.	typ.	max.	Units
t_{RCIP}	CKy_+ Period	12.27	-	15.38	ns
t_{RCIH}	CKy_+ High pulse width	-	$\frac{4}{7}t_{RCIP}$	-	ns
t_{RCIL}	CKy_+ Low pulse width	-	$\frac{3}{7}t_{RCIP}$	-	ns
t_{RMG}	Receiver Data Input Margin	-0.4	-	0.4	ns
t_{RIP1}	Input Data Position0	$- t_{RMG} $	0	$+ t_{RMG} $	ns
t_{RIP0}	Input Data Position1	$\frac{t_{RCIP}}{7} - t_{RMG} $	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7} + t_{RMG} $	ns
t_{RIP6}	Input Data Position2	$2\frac{t_{RCIP}}{7} - t_{RMG} $	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7} + t_{RMG} $	ns
t_{RIP5}	Input Data Position3	$3\frac{t_{RCIP}}{7} - t_{RMG} $	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7} + t_{RMG} $	ns
t_{RIP4}	Input Data Position4	$4\frac{t_{RCIP}}{7} - t_{RMG} $	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7} + t_{RMG} $	ns
t_{RIP3}	Input Data Position5	$5\frac{t_{RCIP}}{7} - t_{RMG} $	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7} + t_{RMG} $	ns
t_{RIP2}	Input Data Position6	$6\frac{t_{RCIP}}{7} - t_{RMG} $	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7} + t_{RMG} $	ns



4.10 OPTICS

4.10.1 Optical characteristics

Parameter		Condition	Symbol	Min.	Typ.	Max.	Unit	Remarks
Luminance		White at center θR= 0°,θL= 0°, θU= 0°,θD= 0°	L	280	400	-	cd/m²	
Contrast ratio		White/Black at center θR= 0°,θL= 0°, θU= 0°,θD= 0°	CR	600	1,000	-	-	Note3
Luminance uniformity		White θR= 0°,θL= 0°, θU= 0°,θD= 0°	LU	-	1.25	1.4	-	Note4
Chromaticity	White	x coordinate	Wx	-0.06	0.313	+0.06	-	Note5
		y coordinate	Wy		0.329		-	
	Red	x coordinate	Rx		0.63		-	
		y coordinate	Ry		0.335		-	
	Green	x coordinate	Gx		0.29		-	
		y coordinate	Gy		0.62		-	
	Blue	x coordinate	Bx		0.155		-	
		y coordinate	By		0.065		-	
Color gamut		θR= 0°,θL= 0°, θU= 0°,θD= 0° at center, against NTSC color space	C	65	72	-	%	
Response time		Black to White	Ton	-	12	20	ms	Note6
		White to Black	Toff	-	13	20	ms	Note7
Viewing angle	Right	θU= 0°, θD= 0°, CR≥10	θR	70	88	-	°	Note8
	Left	θU= 0°, θD= 0°, CR≥10	θL	70	88	-	°	
	Up	θR= 0°, θL= 0°, CR≥10	θU	70	88	-	°	
	Down	θR= 0°, θL= 0°, CR≥10	θD	70	88	-	°	

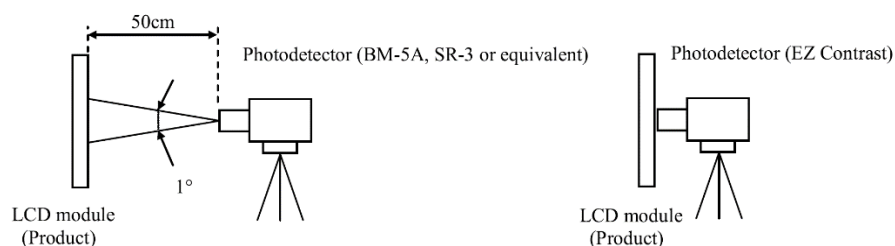
Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta= 25°C, VCC= 3.3V, VDD=12.0V, PWM duty ratio: 100%,

Display mode: FHD, Horizontal cycle= 1/67.43kHz, Vertical cycle= 1/59.94Hz,

Optical characteristics are measured at luminance saturation 20minutes after the product works in the dark room. Also measurement methods are as follows.



Note3: Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

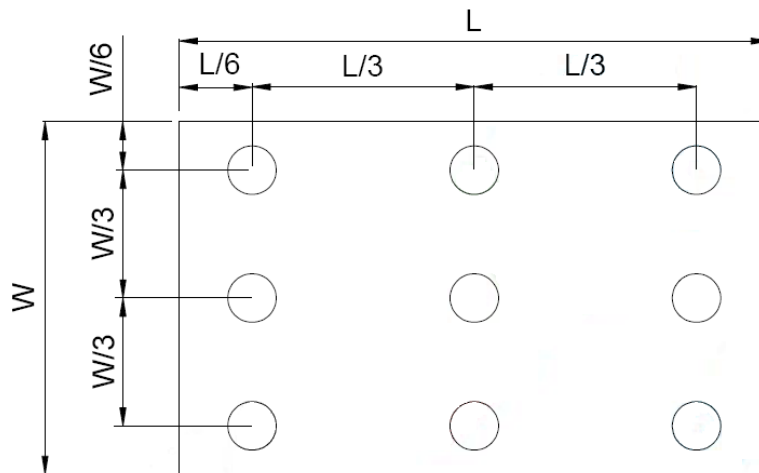
$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

Note4: Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

$$\text{Luminance Uniformity(LU)} = \frac{\text{Maximum Luminance from 9 points}}{\text{Minimum Luminance from 9 points}}$$

The luminance is measured at near the 9 points shown below.

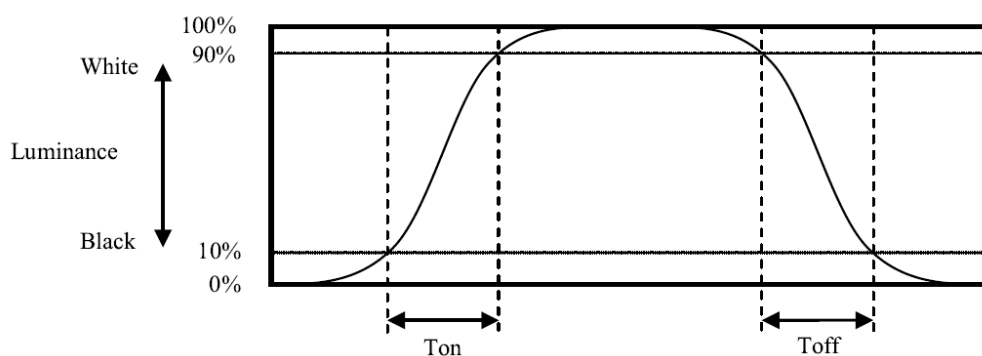


Note5: These coordinates are found on CIE 1931 chromaticity diagram.

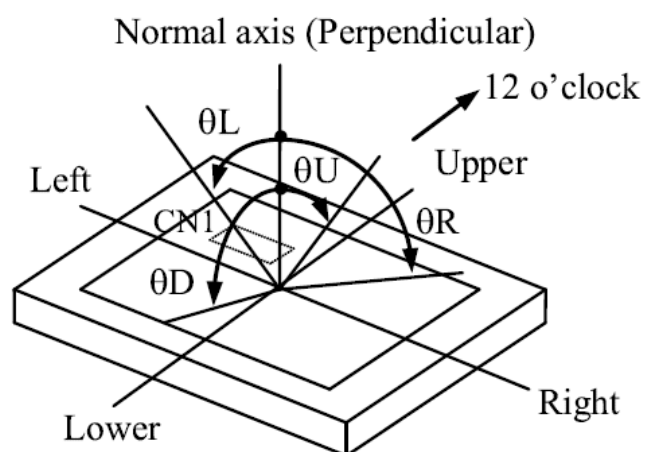
Note6: Product surface temperature: TopF= 29°C

Note7: Definition of response times

Response time is measured at the time when the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time when the luminance changes from 10% up to 90%. Also Toff is the time when the luminance changes from 90% down to 10% (See the following diagram.).



Note8: Definition of viewing angles



5. ESTIMATED LUMINANCE LIFETIME

The luminance lifetime is the time from initial luminance to half-luminance.

This lifetime is the estimated value, and is not guarantee value.

Condition		Estimated luminance lifetime (Life time expectancy) Note1, Note2, Note3	Unit
LED elementary substance	25°C (Ambient temperature of the product) Continuous operation, PWM duty ratio:100%	50,000	Hr
	70°C (Temperature of LCD panel surface and rear shield surface) Continuous operation, PWM duty ratio:100%	30,000	

Note1: Life time expectancy is mean time to half-luminance.

Note2: Estimated luminance lifetime is not the value for LCD module but the value for LED elementary substance.

Note3: By ambient temperature, the lifetime changes particularly. Especially, in case the product works under high temperature environment, the lifetime becomes short.

6. RELIABILITY TEST CONDITIONS

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=240 hrs	
Low Temperature Operation	-20±3°C , t=240 hrs	
High Temperature Storage	70±3°C , t=240 hrs	1,2
Low Temperature Storage	-20±3°C , t=240 hrs	1,2
Thermal Shock Test	-20°C ~ 60°C 30 min. ~ 30 min. (1 cycle) Total 100cycle	1,2
Storage Humidity Test	60 °C, Humidity 60%, 240 hrs	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 50 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1: Condensation of water is not permitted on the module.

Note 2: The module should be inspected after 1 hour storage in normal conditions (15-35°C, 45-65%RH).

Note 3 : The module shouldn't be tested more than one condition, and all the test conditions are independent.

Note 4 : All the reliability tests should be done without protective film on the module.

Definitions of life end point:

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

8. General Precautions

8.1 Handling Precautions

1. Display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:
 - Isopropyl alcohol
 - Ethyl alcoholSolvents other than those mentioned above may damage the polarizer. Especially, do not use the following:
 - Water
 - Ketone
 - Aromatic solvents
6. Do not attempt to disassemble the LCD Module.
7. If the logic circuit power is off, do not apply the input signals.
8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
 - a. Be sure to ground the body when handling the LCD Modules.
 - b. Tools required for assembly, such as soldering irons, must be properly ground.
 - c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
 - d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

8.2 Storage precautions

1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.
2. The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:
Temperature : 0℃ ~ 40℃
Relatively humidity: ≤80%
3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

8.3 General Precautions

1. Do not keep the LCD at the same display pattern continually. The residual image will happen and it will damage the LCD. Please use screen saver.
2. The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

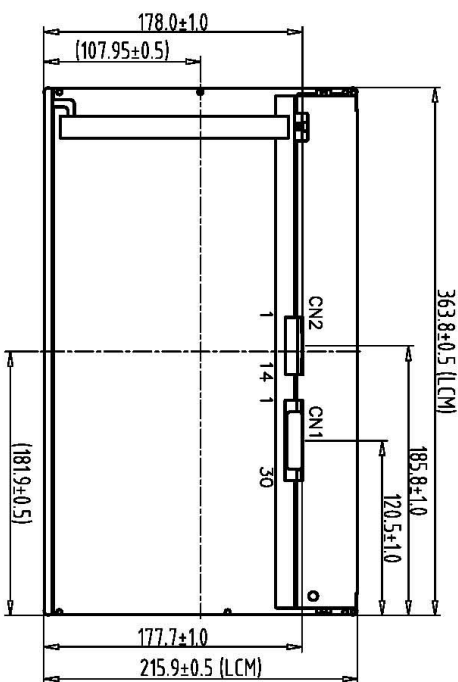
REV	REVISION RECORD	DATE	NAME
0	NEW RELEASE	09-07-18	UED



CN1		CN2	
1	DB1+	1	VDD
2	DA0+	2	VDD
3	DA1+	3	VDD
4	DA1-	4	VDD
5	DA2-	5	VDD
6	DA2+	6	GND
7	GND	7	GND
8	CLKA-	8	GND
9	CLKA+	9	GND
10	DA3-	10	GND
11	DA3+	11	RVSD
12	DB0-	12	BRC
13	DB0+	13	PMU
14	GND	14	GND
15	DB1-		

Back view

1. Unless indicated, Tolerance " $\pm 0.5^\circ$ "
2. UV Glue For OLB Protection.
3. LCD 1920x1080 (RGB) TFT LCD => 15.6" TFT LCD
4. CN1 Connector: Hirose MDF76KBW-30S-1H(S5) or Equivalent.
5. Matching Connector: Hirose MDF76-30P-1C or Equivalent.
6. CN2 Connector: Hirose DF19-14P-1H(S4) or Equivalent.
7. Matching Connector: Hirose DF19-14S-1C or Equivalent.



1							TITLE
2							19201080N (15.6") IPS
3							
4							
5							
6							
7			DIM.	DWN.	DATE		
8			NM	JED	09-07-18		
9			IE NO.	CER.	DATE		
10			PARTS NO. LCH-1	APPD.	DATE		
11			19201080N				
12							
						DWG. NO. *180938MA	SHEET 1 OF 1