



Product Specification

AU OPTRONICS CORPORATION

() Preliminary Specifications

(V) Final Specifications

Module	14.0"(13.97") HD 16:9 Color TFT-LCD
Model Name	G140XTN01.0

Customer	Date	Approved by	Date
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Checked & Approved by	Date	Prepared by	Date
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Note: This Specification is subject to change without notice.		General Display Business Division / AU Optronics corporation	



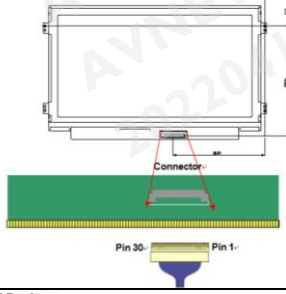
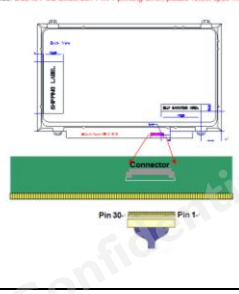
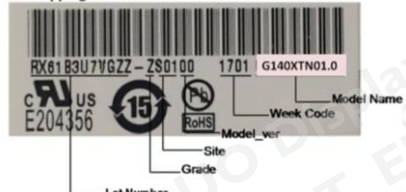
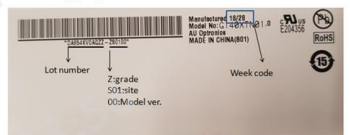
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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.0 2017/03/06	All	First Edition for Customer		
0.1 2017/3/29	1	1.only AUO module name 2.without packing dimension 3.without handle guide	1.add panasonic global parts number 2.add label & packing information 3.add handle guide	
0.2 2017/4/14	26	w/o BL label dimension	Add BL label dimension	
1.0 2017/4/17		Preliminary Specifications	Final Specifications	
1.1 2018/5/16	21		Update Timing Characteristics	
1.2 2018/10/23	20	<p>Note1: Start from right side. (Due to Pin 1 printing error, please follow spec mark.)</p> 	<p>Note1: Start from right side. Due to PCB silkscreen Pin 1 printing error, please follow spec mark.</p> 	
1.2 2018/10/23	27	<p>9. Shipping and Package.</p> <p>9.1 Shipping Label Format.</p> 	<p>9. Shipping and Package.</p> <p>9.1 Shipping Label Format.</p> 	

1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

G140XTN01.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x 768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

G140XTN01.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	354.95			
Active Area	[mm]	309.399 x 173.952			
Pixels H x V		1366 x 3(RGB) x 768			
Pixel Pitch	[mm]	0.2265 x 0.2265			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White(TN)			
White Luminance (I _{LED} =25mA) (Note: I _{LED} is LED current)	[cd/m ²]	220 typ. (5 points average) 187 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		400 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	2.9W max. (Include Logic and Blu power)			
Weight	[Grams]	270 max.			
Physical Size Include bracket	[mm]		Min.	Typ.	Max.
		Length	319.9	320.4	320.9
		Width	204.6	205.1	205.6
		Thickness	-	-	3.0
Electrical Interface		1 Lane eDP			
Glass Thickness	[mm]	0.4			
Surface Treatment		Anti-Glare, Hardness 3H			
Support Color		262K colors (RGB 6-bit)			

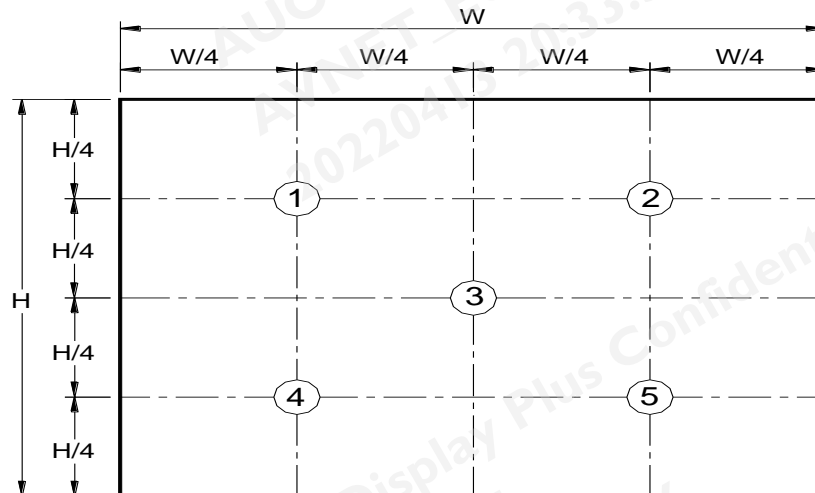
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

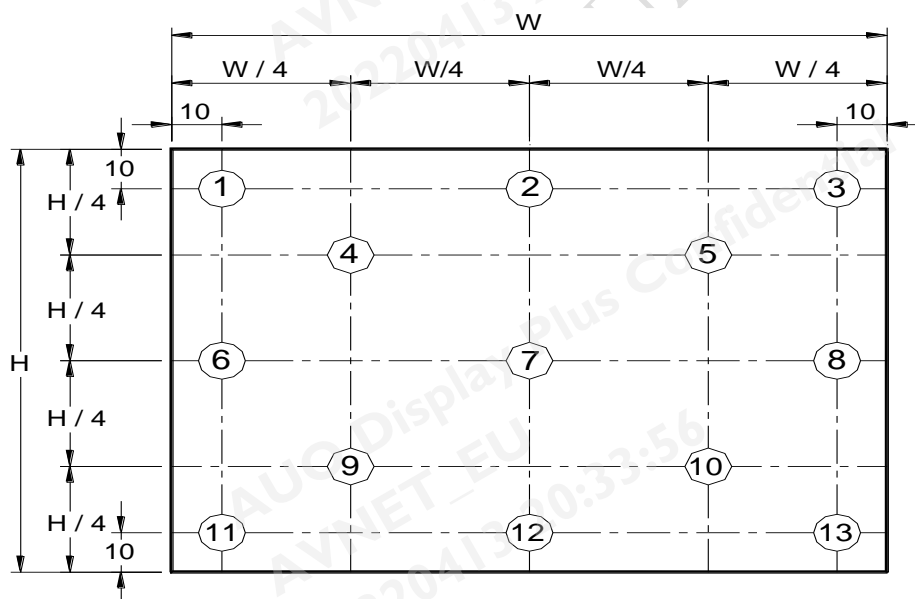
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I _{LED} =25mA		5 points average	187	220	-	cd/m ²	1, 4, 5.
Viewing Angle	θ_R	Horizontal (Right)	40	45	-	degree	4, 9
	θ_L	CR = 10 (Left)	40	45	-		
	ϕ_H	Vertical (Upper)	10	15	-		
	ϕ_L	CR = 10 (Lower)	30	35	-		
Luminance Uniformity	δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio	CR		300	400	-		4, 6
Cross talk	%		-	-	4		4, 7
Response Time	T _{RT}	Rising + Falling	-	8	16	msec	4, 8
Color / Chromaticity Coordinates	Red	Rx	0.537	0.567	0.597	-	4
		Ry	0.308	0.338	0.368		
	Green	Gx	0.311	0.341	0.371		
		Gy	0.531	0.561	0.591		
	Blue	Bx	0.131	0.161	0.191		
		By	0.102	0.132	0.162		
	White	Wx	0.283	0.313	0.343		
		Wy	0.299	0.329	0.359		
			-	45	-		
NTSC	%						

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

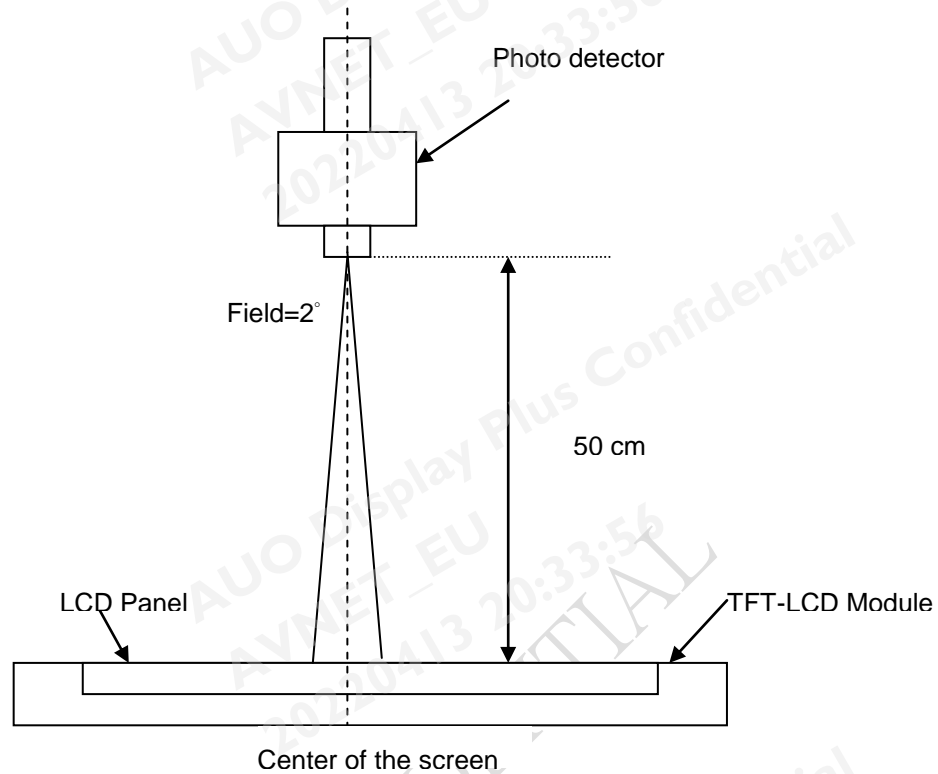
$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

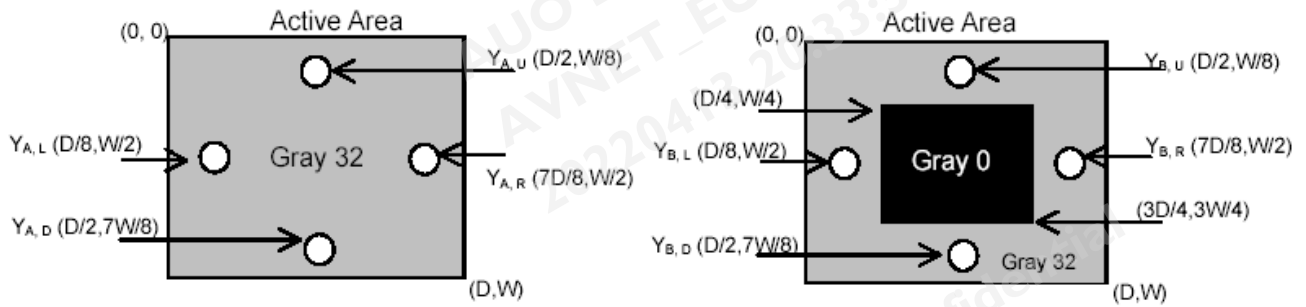
Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

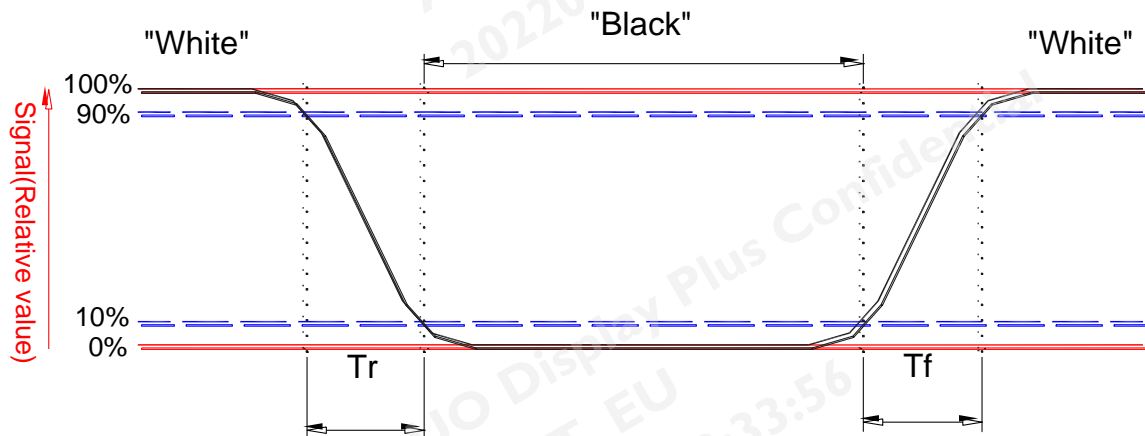
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



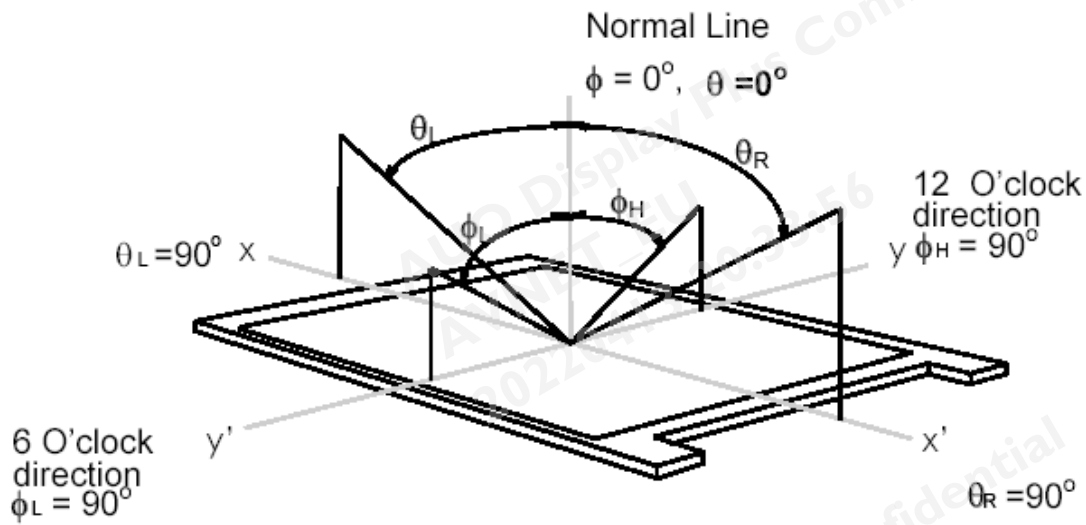
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



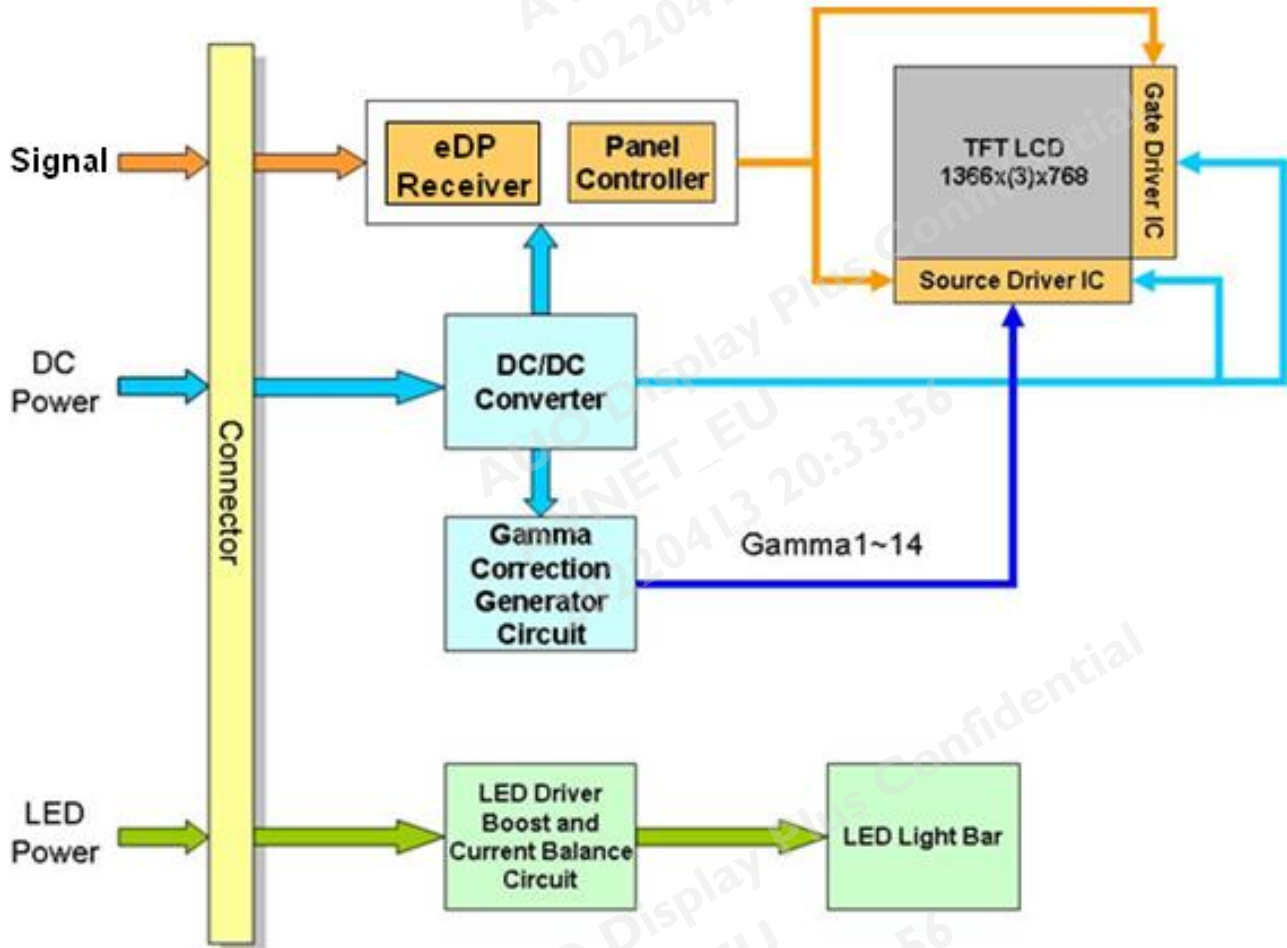
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (ϕ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 30 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

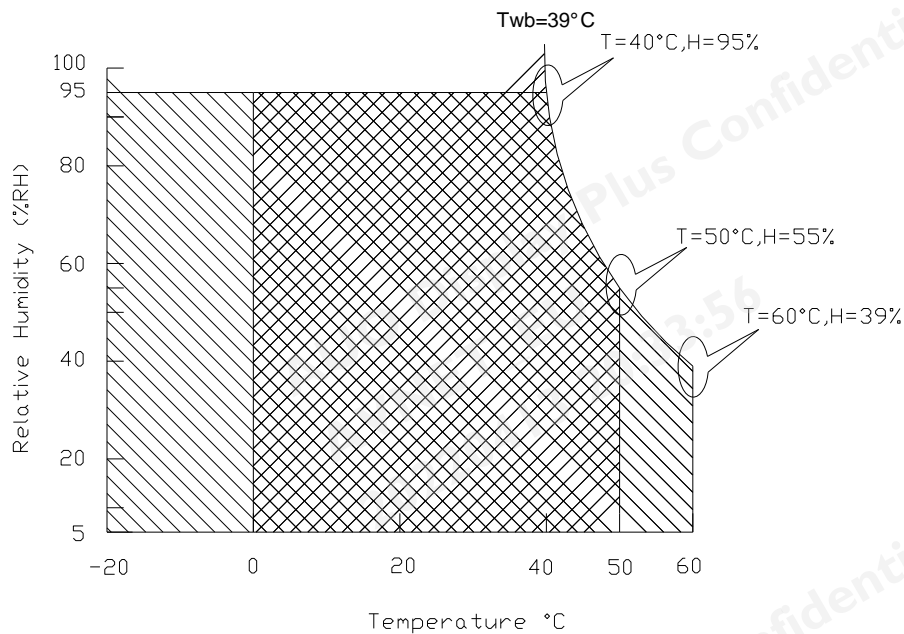
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

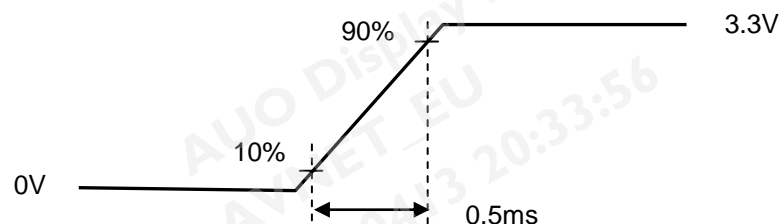
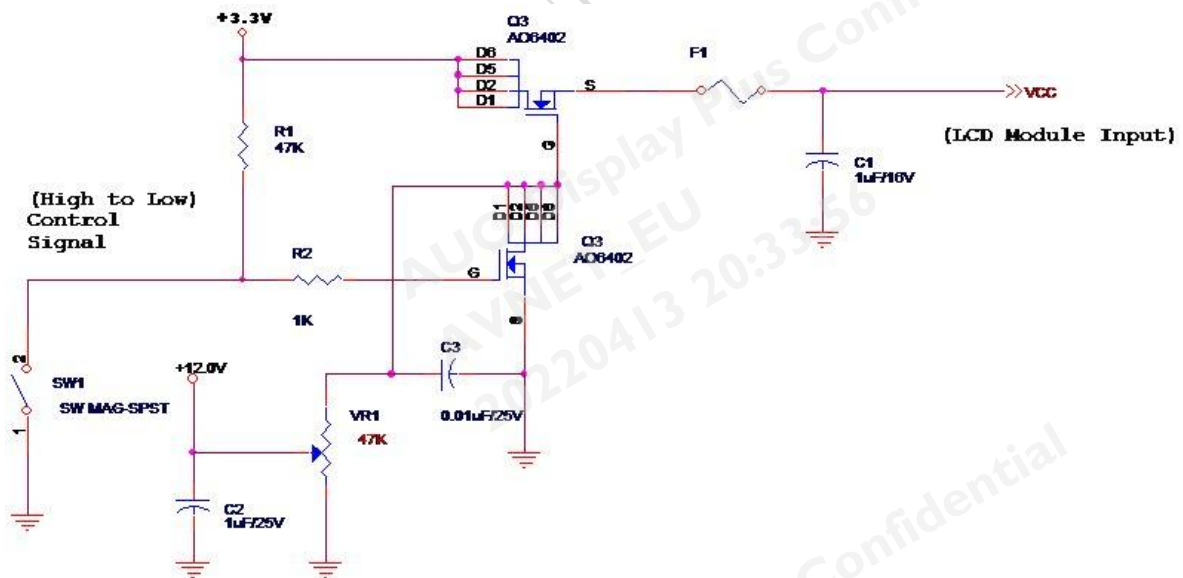
The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-		0.7	[Watt]	Note 1
IDD	IDD Current(RMS)	-		212	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Typical Measurement Condition : Mosaic Pattern

Note 2 : Measure Condition

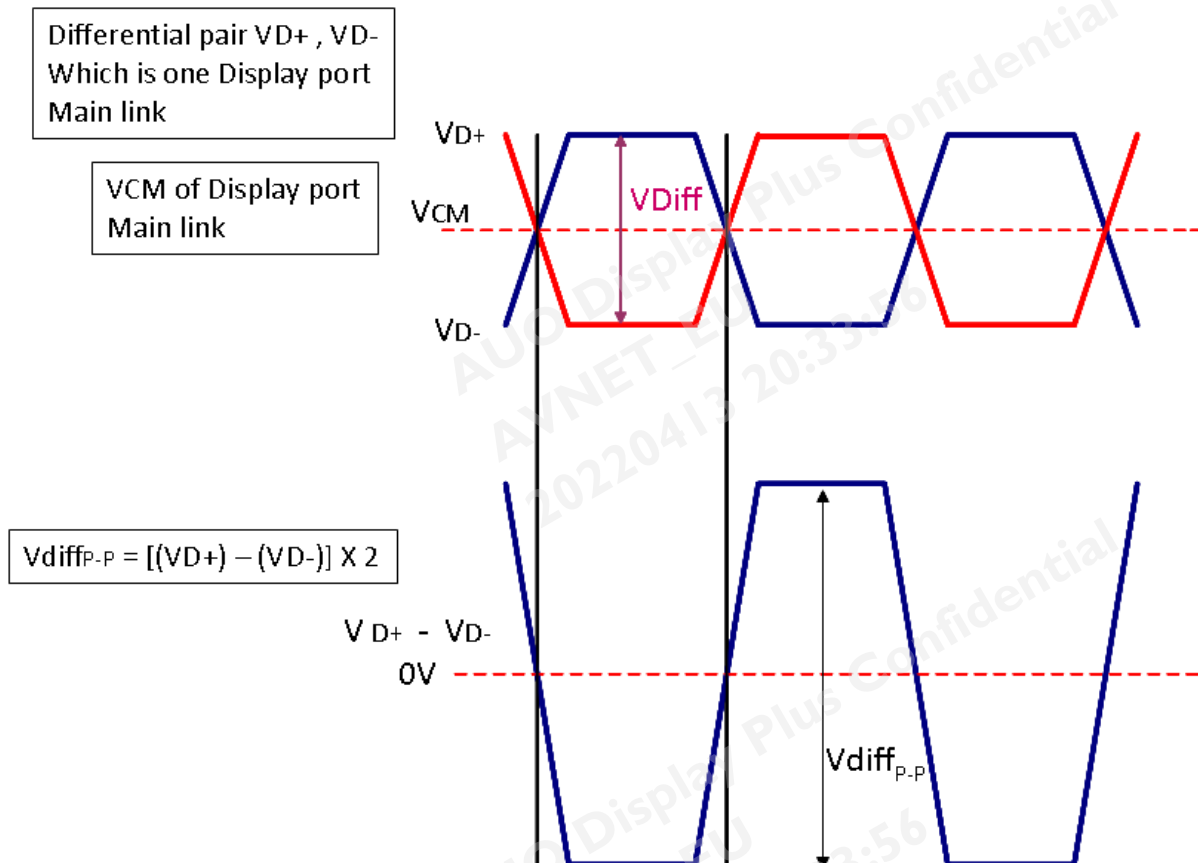


5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

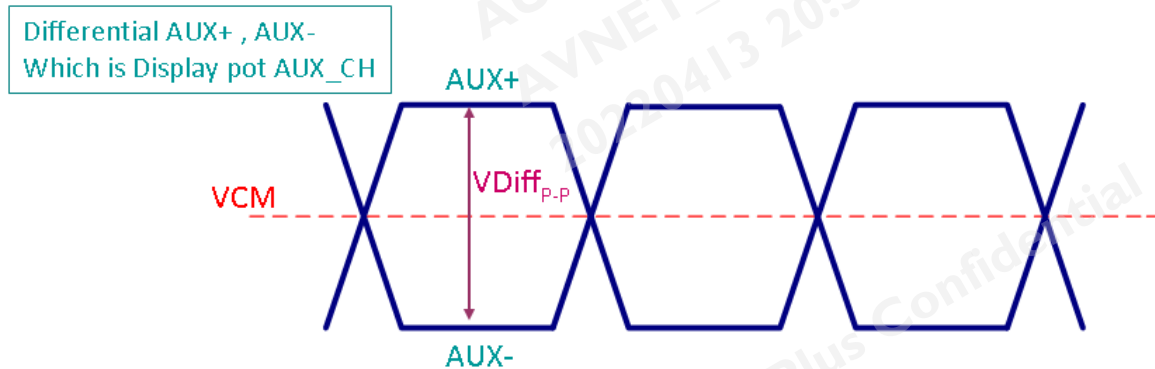
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff _{P-P}	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Fallow as VESA display port standard V1.1a

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff _{P-P}	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Fallow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

Fallow as VESA display port standard V1.1a.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.2	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 If=24 mA

Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.2	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.6	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.2	-	5.0	[Volt]	
PWM Logic Input Low Level		-	-	0.6	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	1	--	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

6.1 Pixel Format Image

	1															1366								
1st Line	R	G	B	R	G	B												R	G	B	R	G	B

68th Line	R	G	B	R	G	B												R	G	B	R	G	B



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

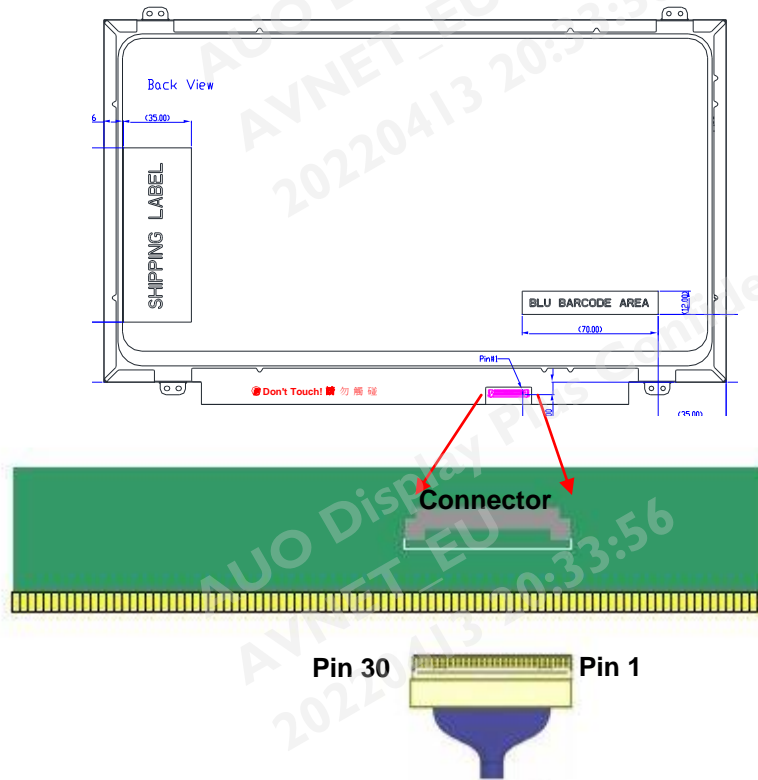
Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	JAE, HD2S030HA1
Mating Housing/Part Number	IPEX 20455-030E-12

6.2.2 Pin Assignment (1 Lane)

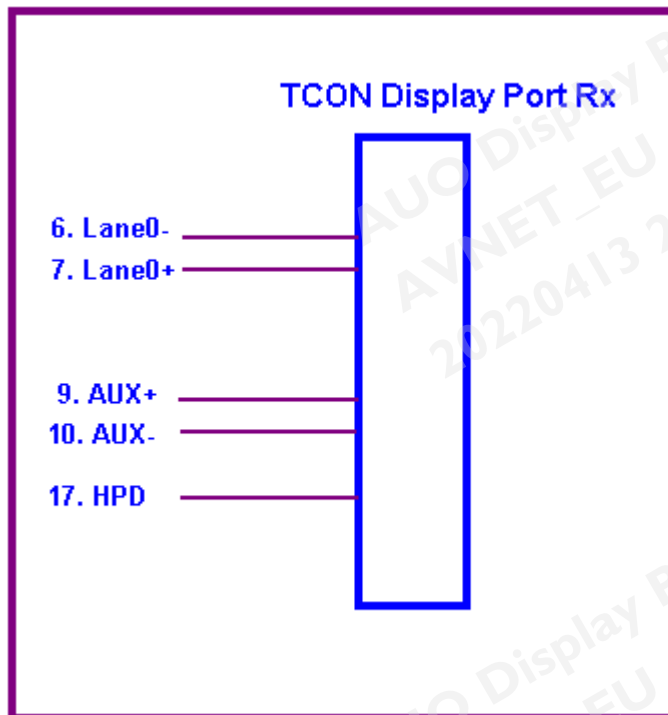
eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	No Connect
2	H_GND	High Speed Ground
3	NC	No Connect
4	NC	No Connect
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	NC	Reverse for AUO TEST only
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight ground
19	BL_GND	Backlight ground
20	BL_GND	Backlight ground
21	BL_GND	Backlight ground
22	BL_Enable	Backlight On / Off
23	BL_PWM_DIM	System PWM signal Input
24	NC	Reverse for AUO TEST only
25	NC	Reverse for AUO TEST only
26	BL_PWR	Backlight power (5V~21V)
27	BL_PWR	Backlight power (5V~21V)
28	BL_PWR	Backlight power (5V~21V)
29	BL_PWR	Backlight power (5V~21V)
30	NC	No connect

Note1: Start from right side. Due to PCB silkscreen PIN 1 printing error, please follow spec mark



Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



6.3 Interface Timing

6.3.1 Timing Characteristics

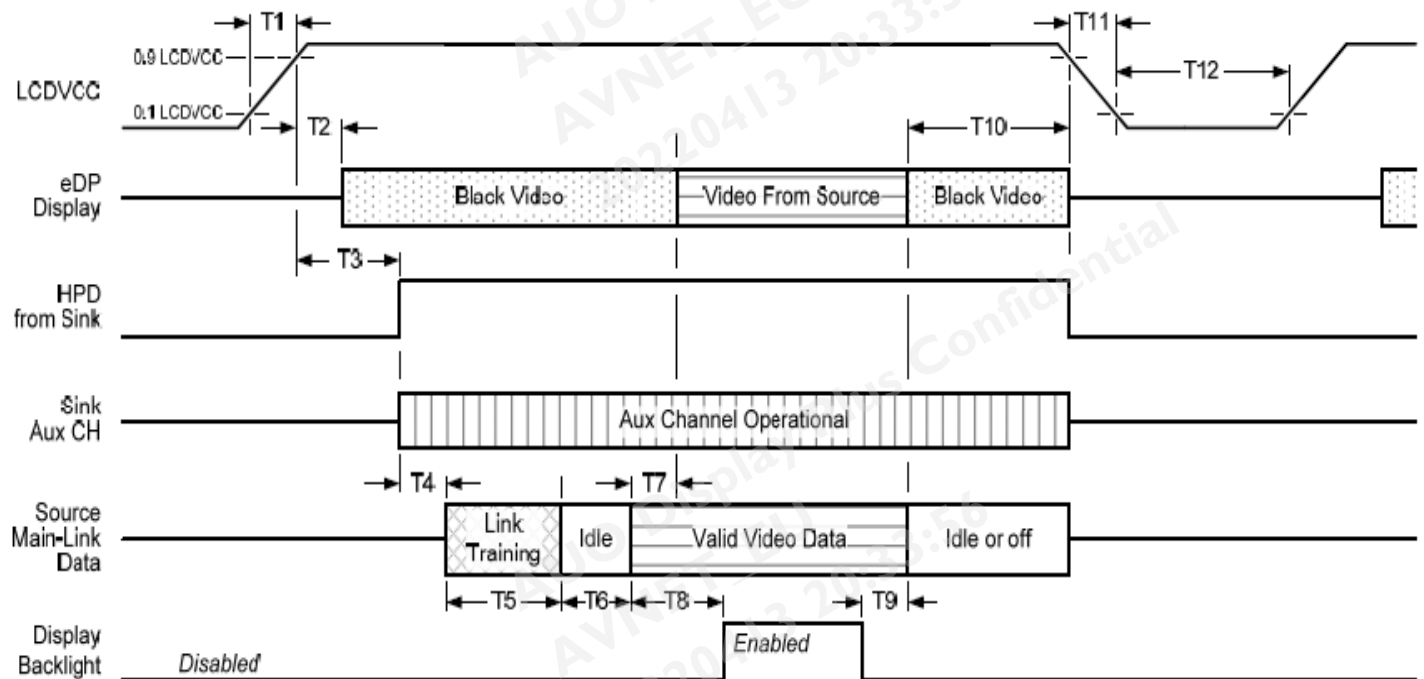
Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T _{Clock}	72.4	75	78.4	MHz
Vertical Section	Period	T _V	790	808	810	T _{Line}
	Active	T _{VD}	768			
	Blanking	T _{VB}	22	40	42	
Horizontal Section	Period	T _H	1526	1547	1614	T _{Clock}
	Active	T _{HD}	1366			
	Blanking	T _{HB}	160	181	248	

Note 1 : The above is as optimized setting

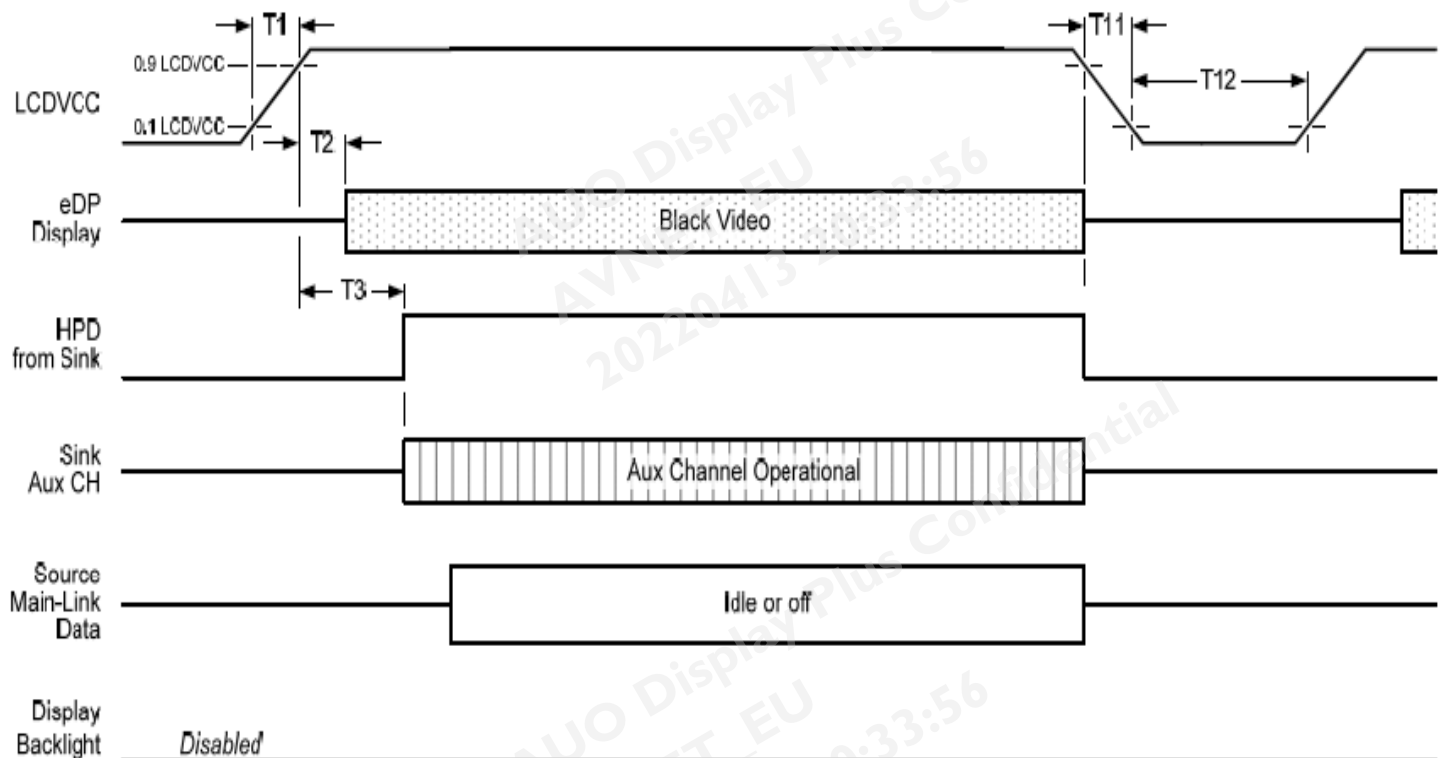
6.4 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

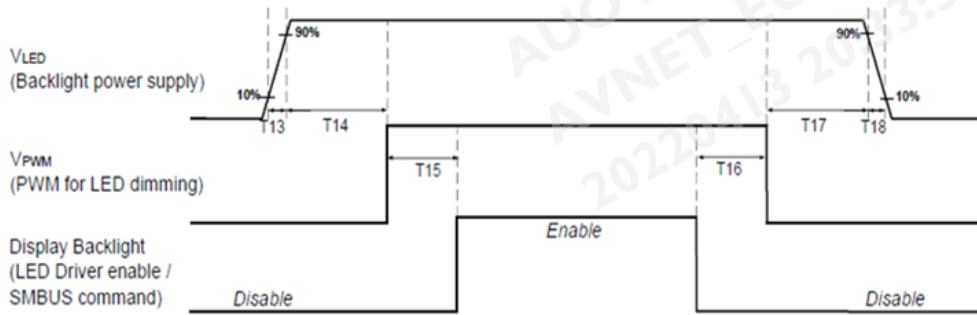
Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

- upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
- when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.2	10
T14	0	-
T15	0	-
T16	0	-
T17	0	-
T18	0.2	10
T19	1*	-
T20	1*	-

Seamless change: $T19/T20 = 5 \times T_{PWM}^*$

* $T_{PWM} = 1/PWM \text{ Frequency}$

Note 1 : If T14,T15,T16,T17<10ms , The display garbage may occur. We suggest T14,T15,T16,T17>10ms to avoid the display garbage.

Note 2 : If T13 or T18<0.5ms , the inrush current may cause the damage of fuse. If T13 or T18<0.5ms , the inrush current I^2t is under typical melt of fuse Spec. , there is no mentioned problem.

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

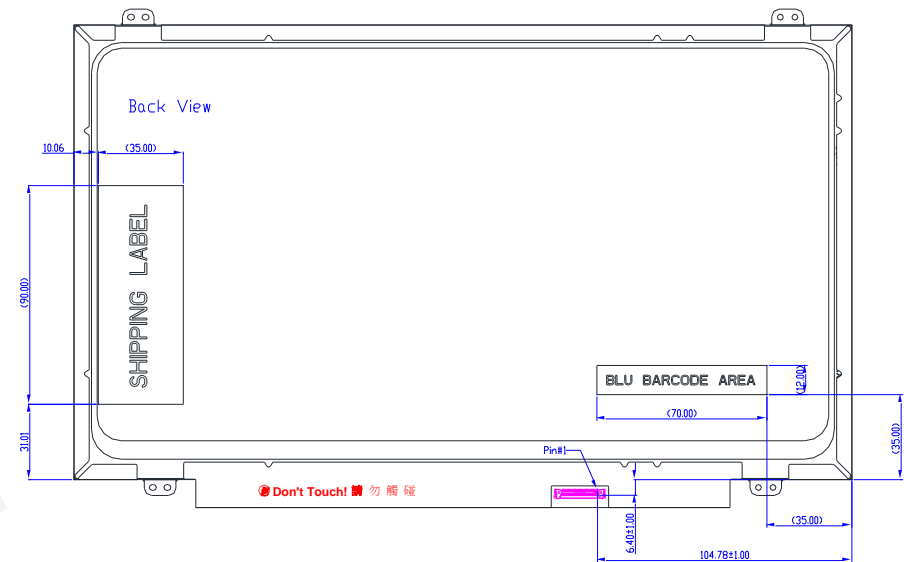
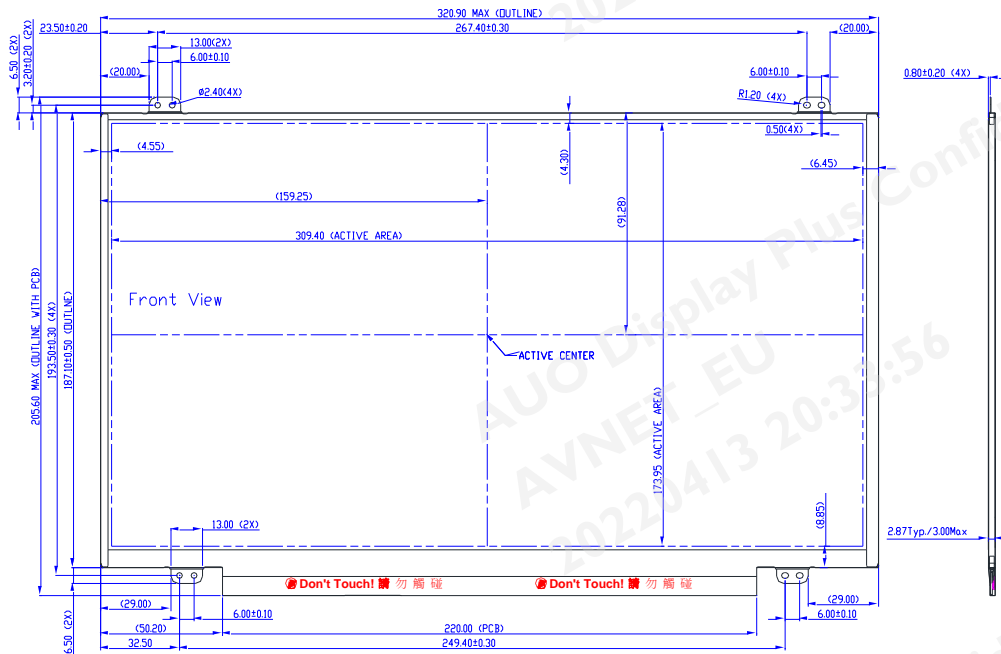
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃ to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable.
No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension

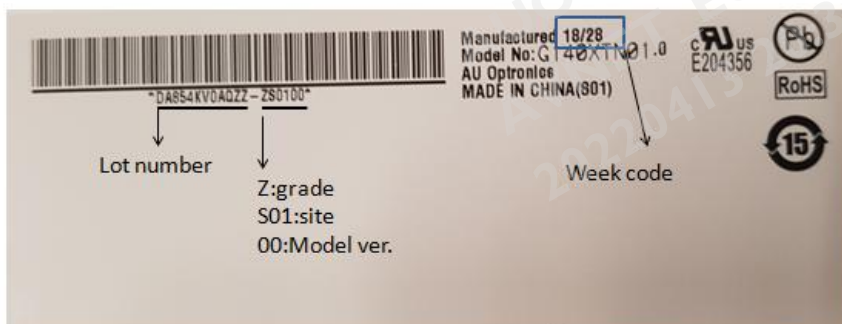


Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

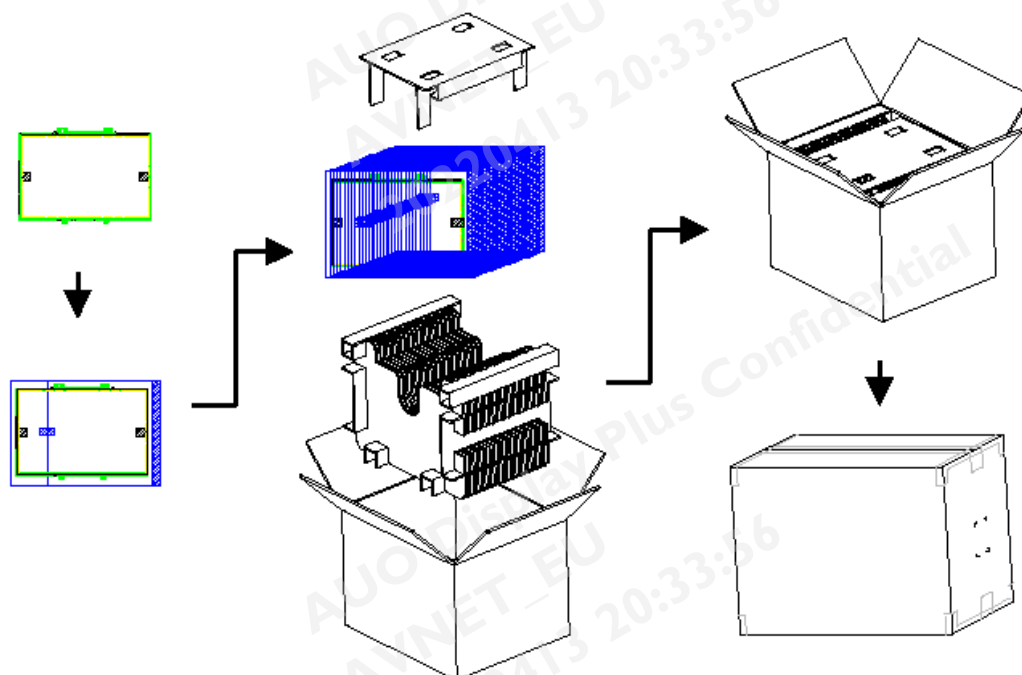
Due to PCB silkscreen PIN 1 printing error, please follow spec mark

9. Shipping and Package

9.1 Shipping Label Format



9.2 Carton Package



Max capacity: 40 pcs TFT-LCD module per carton

Max weight: 14Kg per carton

Outside dimension of carton: 407mm * 377mm * 309mm

Pallet size: 1150mm * 840mm * 132mm

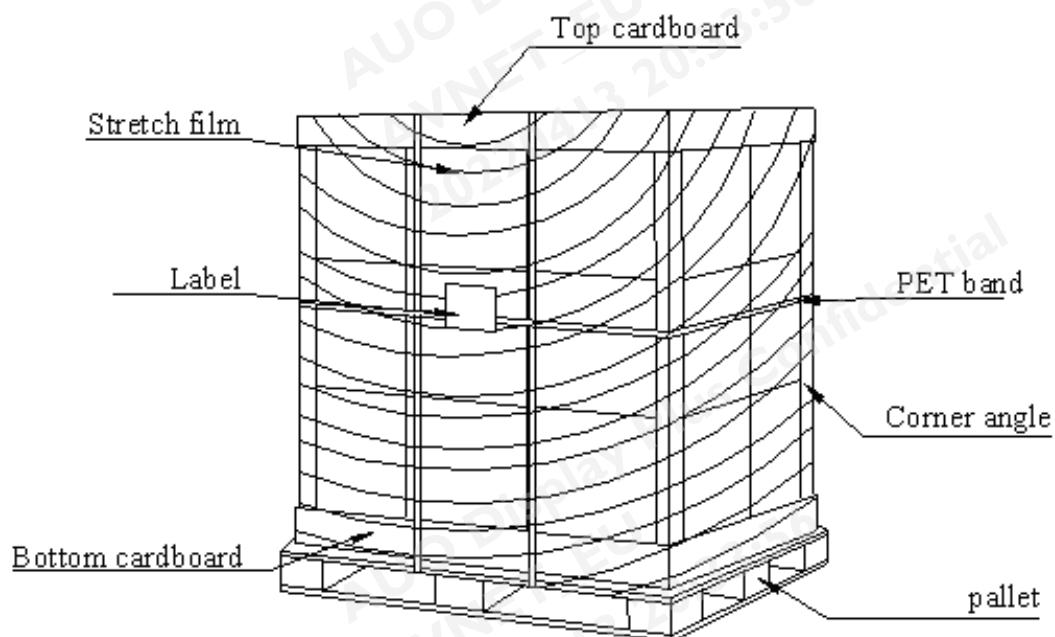
Box stacked

Module by air: (2*3)*4 layers, one pallet put 24 boxes, total 960 pcs module.

Module by sea: (2*3)*4 layers + (2*3)*1 layers, two pallet put 30 boxes, total 1200 pcs module.

Module by sea (HQ): (2*3)*4 layers + (2*3)*2 layers, two pallet put 42 boxes, total 1680 pcs module.

9.3 Shipping Package of Palletizing Sequence



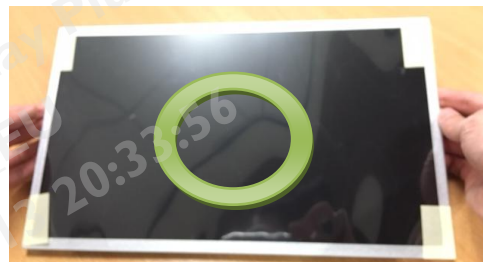
10. Handling guide

This is a LCD model, and please be cautious when pulling it out of package or assembling it onto platform. Careless handlings, e.g. twist, bending, pressing, or collision, will result malfunction of LCD models.

(1) Handling method notice



Do not lift and hold the panel with single hand at right or left side from tray.



Lift and hold the panel up with both hands from tray.

(2) On the table notice



Do not press edge of panel to avoid glass broken.



Do not press the surface of the panel to avoid the glass broken or polarizer scratch.

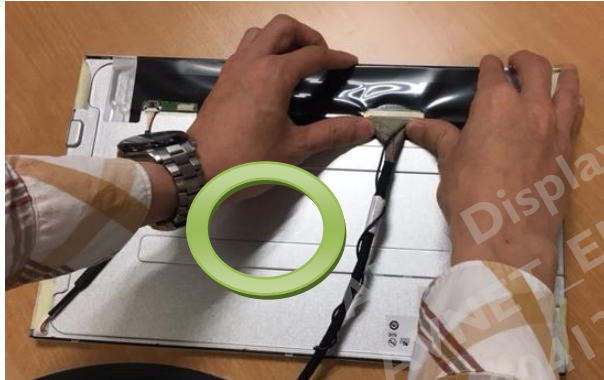


Do not put anything or tool on the panel to avoid the glass broken or polarizer scratch.

(3) Cable assembly notice



Do not insert the connector with single hand and touching the PCBA.



Insert the connector by pushing right and left edge.

11. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	0000000 0	0	
01		FF	1111111 1	255	
02		FF	1111111 1	255	
03		FF	1111111 1	255	
04		FF	1111111 1	255	
05		FF	1111111 1	255	
06		FF	1111111 1	255	
07		00	0000000 0	0	
08	EISA Manuf. Code LSB	06	0000011 0	6	
09	Compressed ASCII	AF	1010111 1	175	
0A	Product Code	3C	0011110 0	60	
0B	hex, LSB first	2E	0010111 0	46	
0C	32-bit ser #	00	0000000 0	0	

0D		00	0000000 0	0	
0E		00	0000000 0	0	
0F		00	0000000 0	0	
10	Week of manufacture	00	0000000 0	0	
11	Year of manufacture	19	0001100 1	25	
12	EDID Structure Ver.	01	0000000 1	1	
13	EDID revision #	04	0000010 0	4	
14	Video input def. (digital I/P, non-TMDS, CRGB)	95	1001010 1	149	
15	Max H image size (rounded to cm)	1F	0001111 1	31	
16	Max V image size (rounded to cm)	11	0001000 1	17	
17	Display Gamma $(=\text{gamma} \times 100) - 100$	78	0111100 0	120	
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	02	0000001 0	2	
19	Red/green low bits (Lower 2:2:2:2 bits)	BB	1011101 1	187	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	F5	1111010 1	245	
1B	Red x (Upper 8 bits)	94	1001010 0	148	
1C	Red y/ highER 8 bits	55	0101010 1	85	
1D	Green x	54	0101010 0	84	
1E	Green y	90	1001000 0	144	
1F	Blue x	27	0010011 1	39	
20	Blue y	23	0010001 1	35	
21	White x	50	0101000 0	80	
22	White y	54	0101010 0	84	
23	Established timing 1	00	0000000 0	0	
24	Established timing 2	00	0000000 0	0	
25	Established timing 3	00	0000000 0	0	
26	Standard timing #1	01	0000000 1	1	
27		01	0000000 1	1	
28	Standard timing #2	01	0000000 1	1	
29		01	0000000 1	1	
2A	Standard timing #3	01	0000000 1	1	
2B		01	0000000 1	1	
2C	Standard timing #4	01	0000000 1	1	
2D		01	0000000 1	1	

2E	Standard timing #5	01	0000000 1	1	
2F		01	0000000 1	1	
30	Standard timing #6	01	0000000 1	1	
31		01	0000000 1	1	
32	Standard timing #7	01	0000000 1	1	
33		01	0000000 1	1	
34	Standard timing #8	01	0000000 1	1	
35		01	0000000 1	1	
36	Pixel Clock/10000 LSB	CE	1100111 0	206	
37	Pixel Clock/10000 USB	1D	0001110 1	29	
38	Horz active Lower 8bits	56	0101011 0	86	
39	Horz blanking Lower 8bits	E2	1110001 0	226	
3A	HorzAct:HorzBlnk Upper 4:4 bits	50	0101000 0	80	
3B	Vertical Active Lower 8bits	00	0000000 0	0	
3C	Vertical Blanking Lower 8bits	1E	0001111 0	30	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	0011000 0	48	
3E	HorzSync. Offset	26	0010011 0	38	
3F	HorzSync.Width	16	0001011 0	22	
40	VertSync.Offset : VertSync.Width	36	0011011 0	54	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	0000000 0	0	
42	Horizontal Image Size Lower 8bits	35	0011010 1	53	
43	Vertical Image Size Lower 8bits	AD	1010110 1	173	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	0001000 0	16	
45	Horizontal Border (zero for internal LCD)	00	0000000 0	0	
46	Vertical Border (zero for internal LCD)	00	0000000 0	0	
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	0001100 0	24	
48	Detailed timing/monitor	00	0000000 0	0	
49	descriptor #2	00	0000000 0	0	
4A		00	0000000 0	0	
4B		0F	0000111 1	15	
4C		00	0000000 0	0	
4D		00	0000000 0	0	
4E		00	0000000 0	0	

4F		00	0000000 0	0	
50		00	0000000 0	0	
51		00	0000000 0	0	
52		00	0000000 0	0	
53		00	0000000 0	0	
54		00	0000000 0	0	
55		00	0000000 0	0	
56		00	0000000 0	0	
57		00	0000000 0	0	
58		00	0000000 0	0	
59		20	0010000 0	32	
5A	Detailed timing/monitor	00	0000000 0	0	
5B	descriptor #3	00	0000000 0	0	
5C		00	0000000 0	0	
5D		FE	1111111 0	254	
5E		00	0000000 0	0	
5F	Manufacture	41	0100000 1	65	A
60	Manufacture	55	0101010 1	85	U
61	Manufacture	4F	0100111 1	79	O
62		0A	0000101 0	10	
63		20	0010000 0	32	
64		20	0010000 0	32	
65		20	0010000 0	32	
66		20	0010000 0	32	
67		20	0010000 0	32	
68		20	0010000 0	32	
69		20	0010000 0	32	
6A		20	0010000 0	32	
6B		20	0010000 0	32	
6C	Detailed timing/monitor	00	0000000 0	0	
6D	descriptor #4	00	0000000 0	0	
6E		00	0000000 0	0	
6F		FE	1111111 0	254	

70		00	0000000 0	0	
71	Manufacture P/N	42	0100001 0	66	B
72	Manufacture P/N	31	0011000 1	49	1
73	Manufacture P/N	34	0011010 0	52	4
74	Manufacture P/N	30	0011000 0	48	0
75	Manufacture P/N	58	0101100 0	88	X
76	Manufacture P/N	54	0101010 0	84	T
77	Manufacture P/N	4E	0100111 0	78	N
78	Manufacture P/N	30	0011000 0	48	0
79	Manufacture P/N	32	0011001 0	50	2
7A	Manufacture P/N	2E	0010111 0	46	.
7B	Manufacture P/N	45	0100010 1	69	E
7C		20	0010000 0	32	
7D		0A	0000101 0	10	
7E	Extension Flag	00	0000000 0	0	
7F	Checksum	C8	1100100 0	200	
				640	
SUM				0	

11.2 Notes

- 1) The height of cell tape no higher than top polarizer 3.0mm
- 2) Marking DPCD version, including PSR, PSR2, MBO, VESA DSC,

DPCD Ver.	PSR	MBO	VESA DSC
1.2	Off	Off	Off

- 3) LED Driving Solution: Minimum change scale duty of the PWM is 0.1% @PWM frequency 200Hz.
- 4) When twisting or pressing LCD module, it may cause unexpected acoustic noises or sounds.
- 5) Maximum value of "Peak current" is as same as "Inrush current" in Electrical Characteristics (Power Specification)
- 6) VDiffP-P (Peak-to-peak Voltage at a receiving Device) follow as VESA display port standard (test point, TP3, is on panel's PCBa)

