

QSeven 2.0 Reference Board

Contents


Page 1	MAIN
Page 2	Block Diagram
Page 3	Qseven Connector
Page 4	PCI-e Clock Buffer
Page 5	MUX PCI-e, SATA, USB 2.0
Page 6	SATA, Feature, LPC, I2C, SPI
Page 7	Audio
Page 8	PCI-e (Slot x16)
Page 9	PCI-e (3 x PCI-e x1 slots)
Page 10	miniPCI-e + SIM Slots
Page 11	HDMI/DP Slot
Page 12	LVDS/eDP Slot
Page 13	CAN interface, POST Codes display
Page 14	Super I/O #1 (W83627DHG)
Page 15	Super I/O #2 (XR28V384)
Page 16	USB 3.0 ports, USB 2.0 ports #6 #7
Page 17	USB 2.0 ports #2 ÷ #5
Page 18	SDIO, Battery, Speaker, LEDs
Page 19	FANs, ETHERNET
Page 20	Power #1
Page 21	Power #2
Page 22	MFG, Debug Uart, Qseven UART
Page 23	Holes, GND Probes

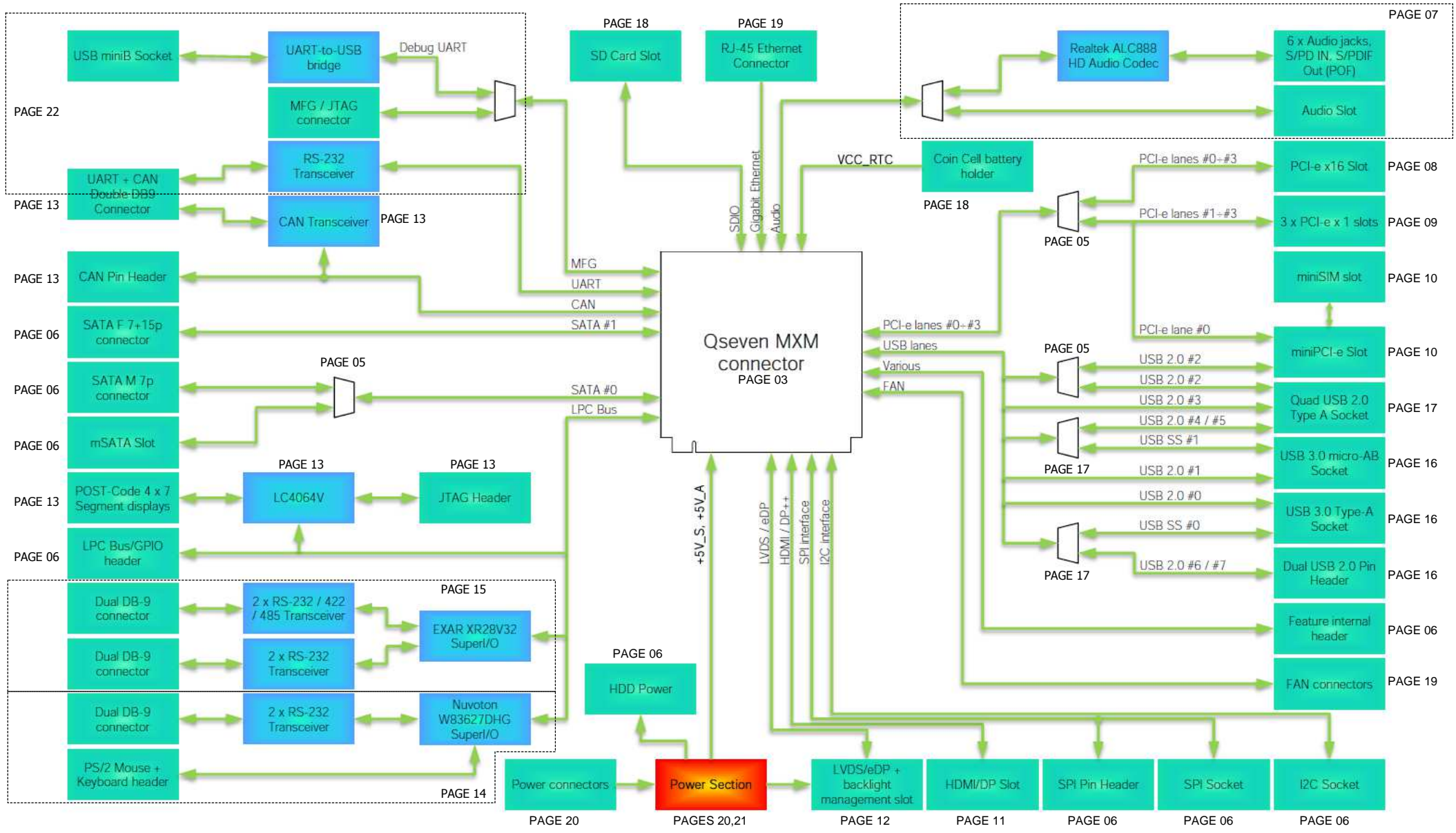
Reference Table

Capacitors CC (Ceramic), CE (Electrolytic):
After the value, it is shown the Minimum Rated Voltage (MRV).
If this it is not shown, then it is implicit that MRV is 6.3V.
Components with /X indications are foreseen in the PCB but must not be mounted

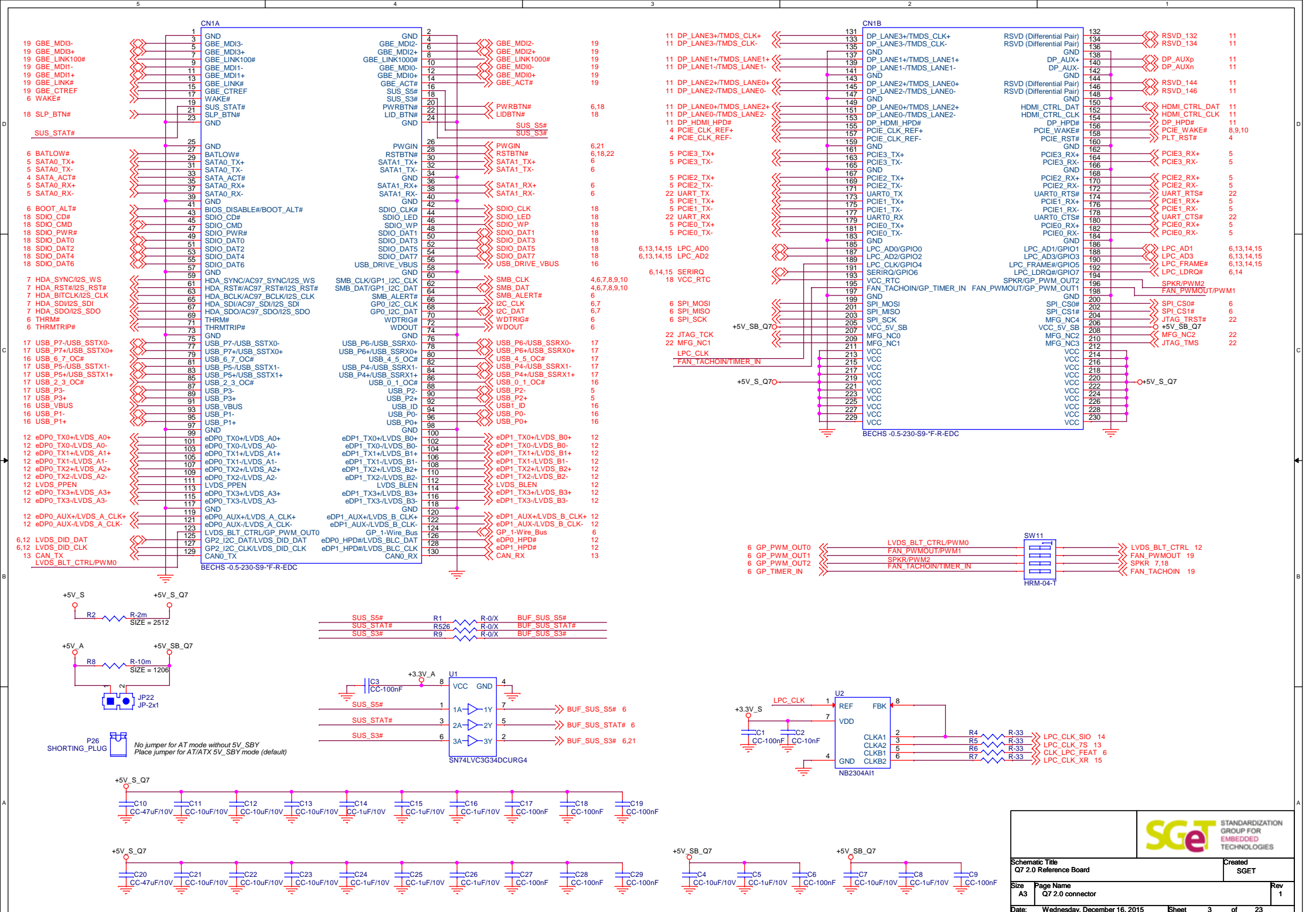
RECOMMENDED OPERATING CONDITIONS

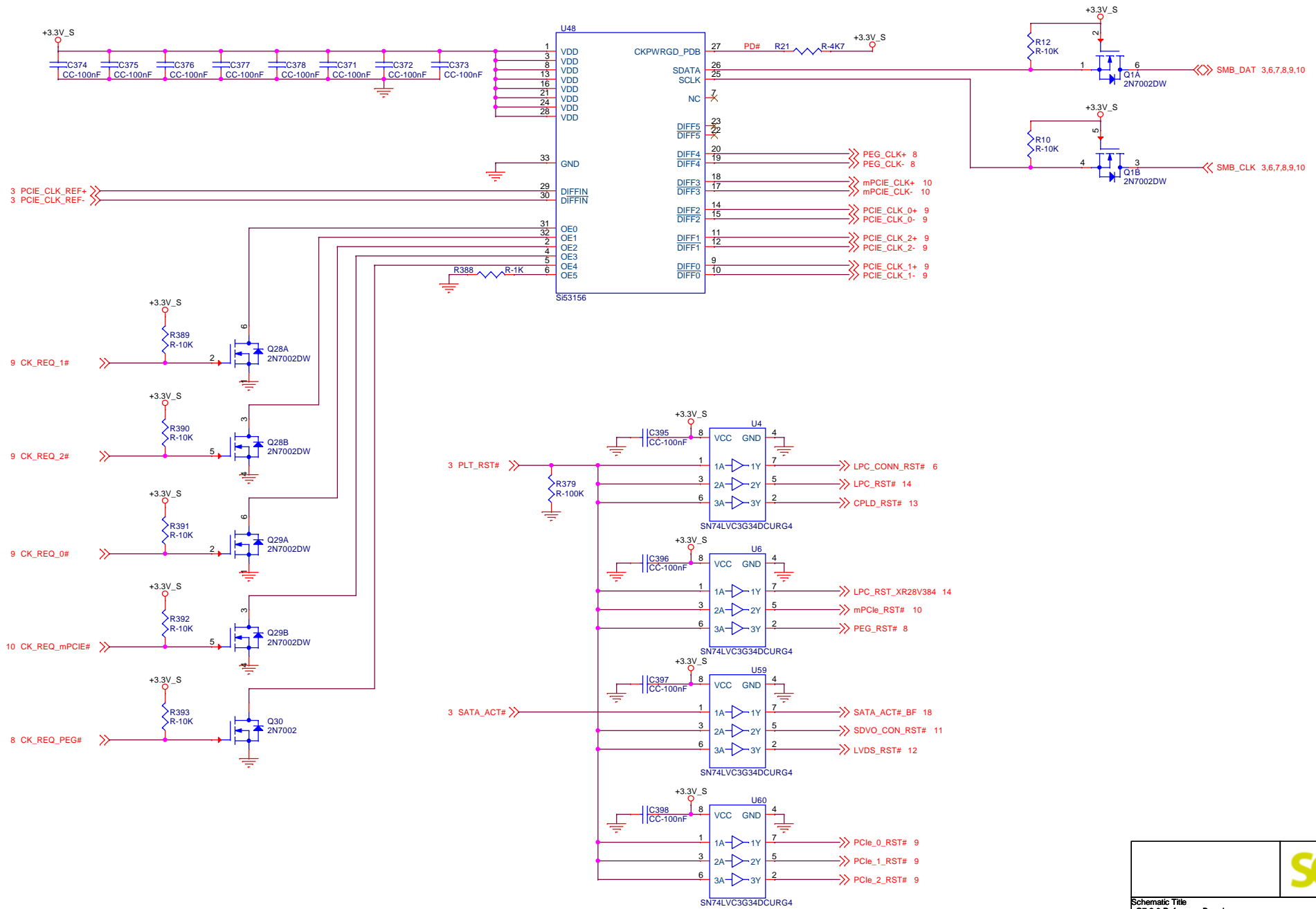
Supply voltage.....12V ± 5%

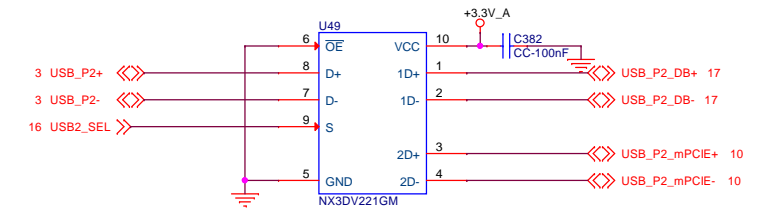
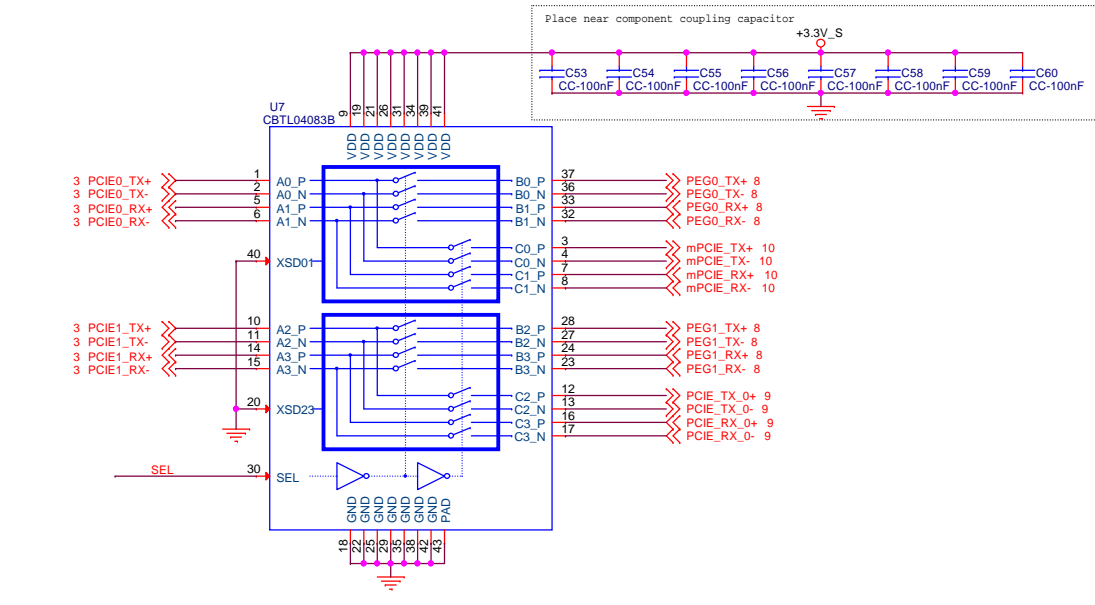
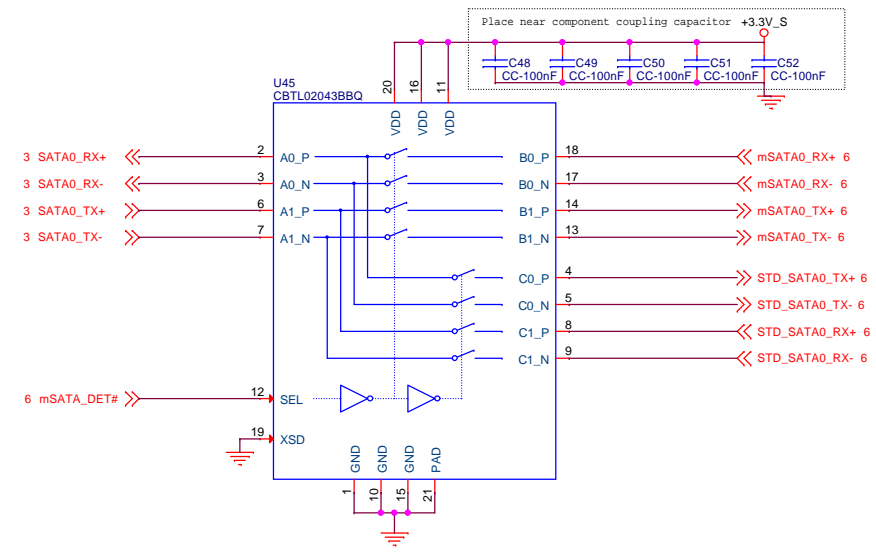
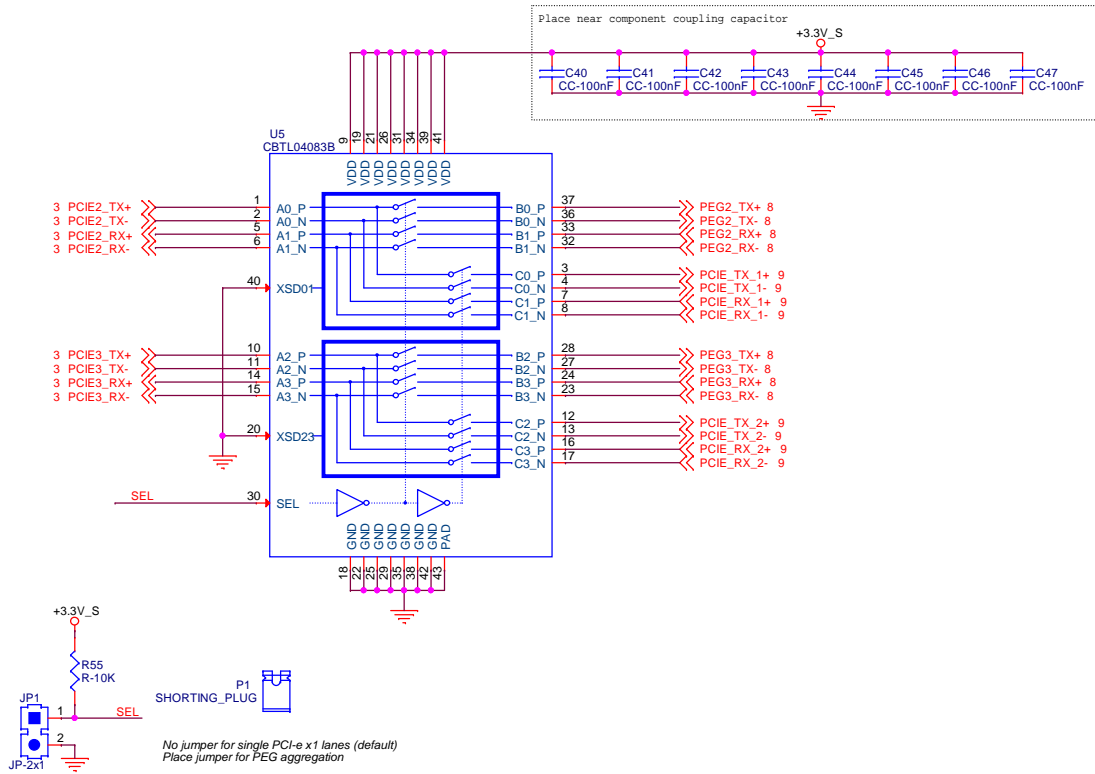
		 STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES	
Schematic Title Q7 2.0 Reference Board		Created SGET	
Size A3	Page Name Main page	Rev 1	
Date: Wednesday, December 16, 2015		Sheet	1 of 23



		SGET STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES	
Schematic Title Q7 2.0 Reference Board			Created SGET
Size A3	Page Name USB and PCIe distribution	Rev 1	
Date: Wednesday, December 16, 2015	Sheet 2	of 23	

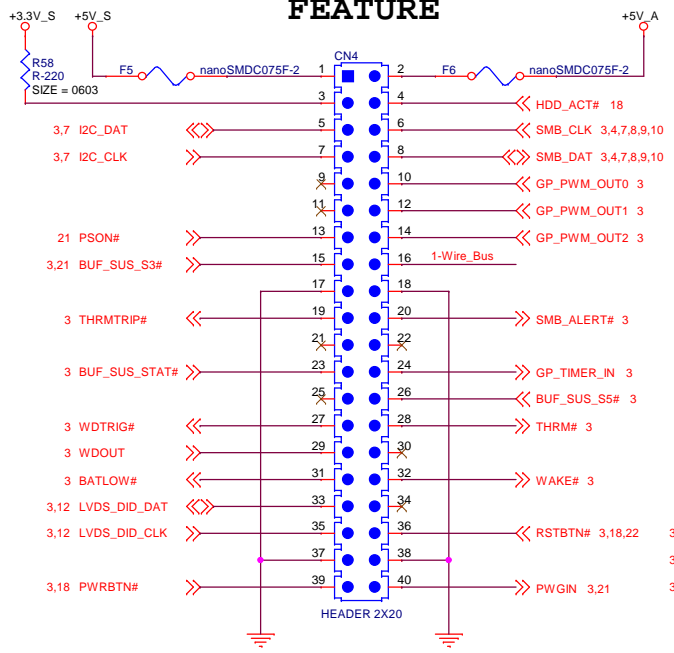




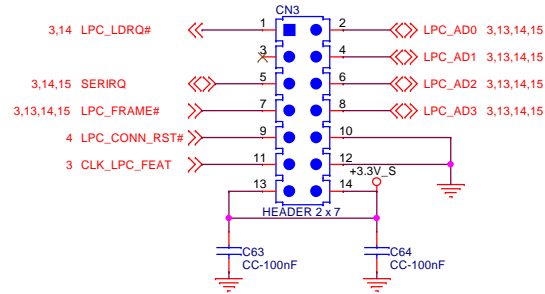


		 STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES	
Schematic Title			Created
Q7 2.0 Reference Board			SGET
Size	Page Name		
A3	Mux		
Date:	Wednesday, December 16, 2015	Sheet	5 of 23
			Rev 1

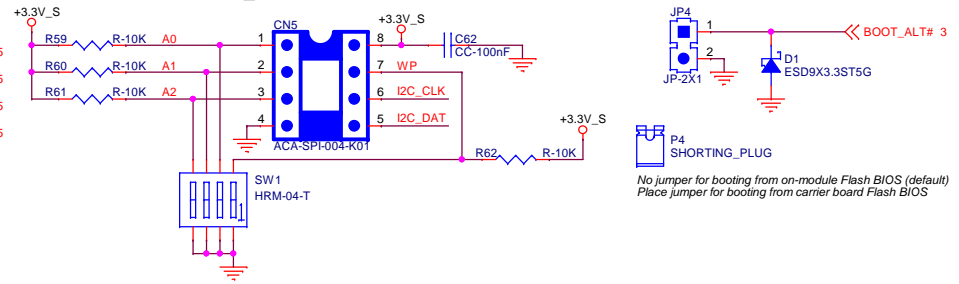
FEATURE



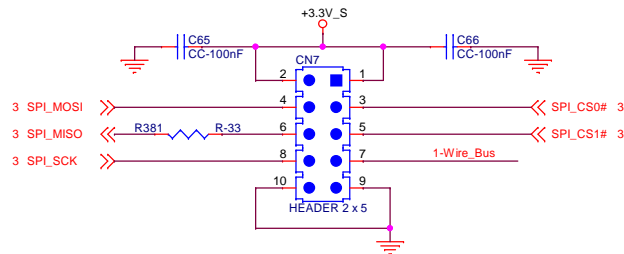
LPC Test connector



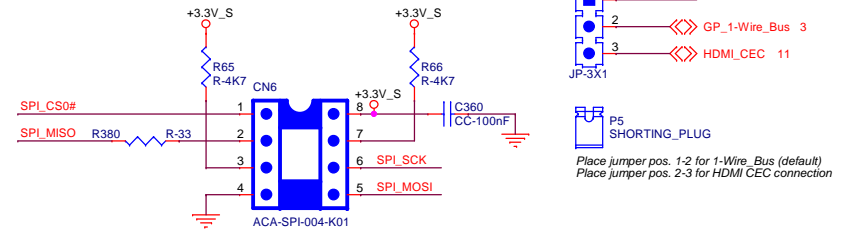
I2C Eeprom SOCKET



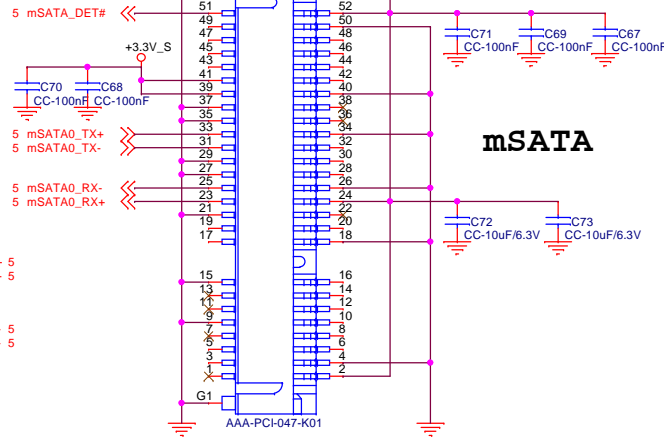
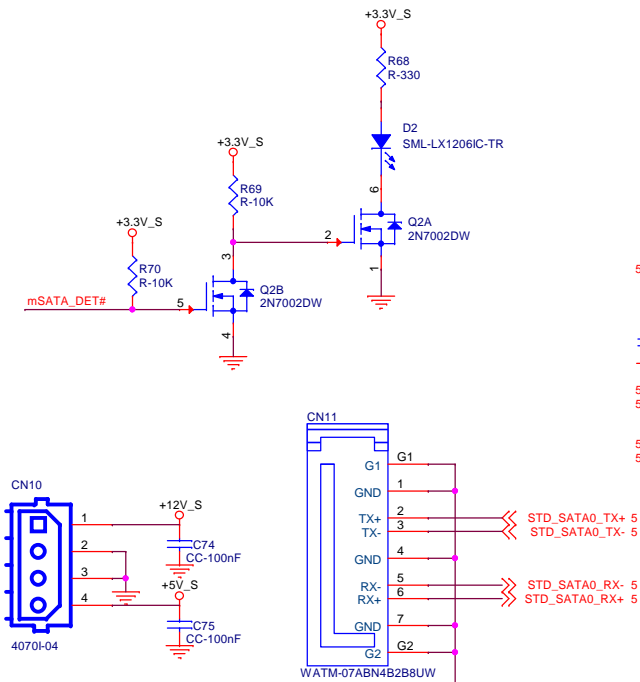
SPI connector



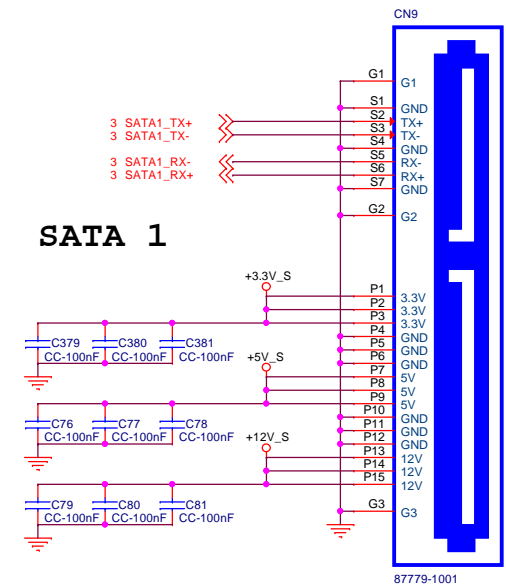
SPI FLASH SOCKET



SATA 0



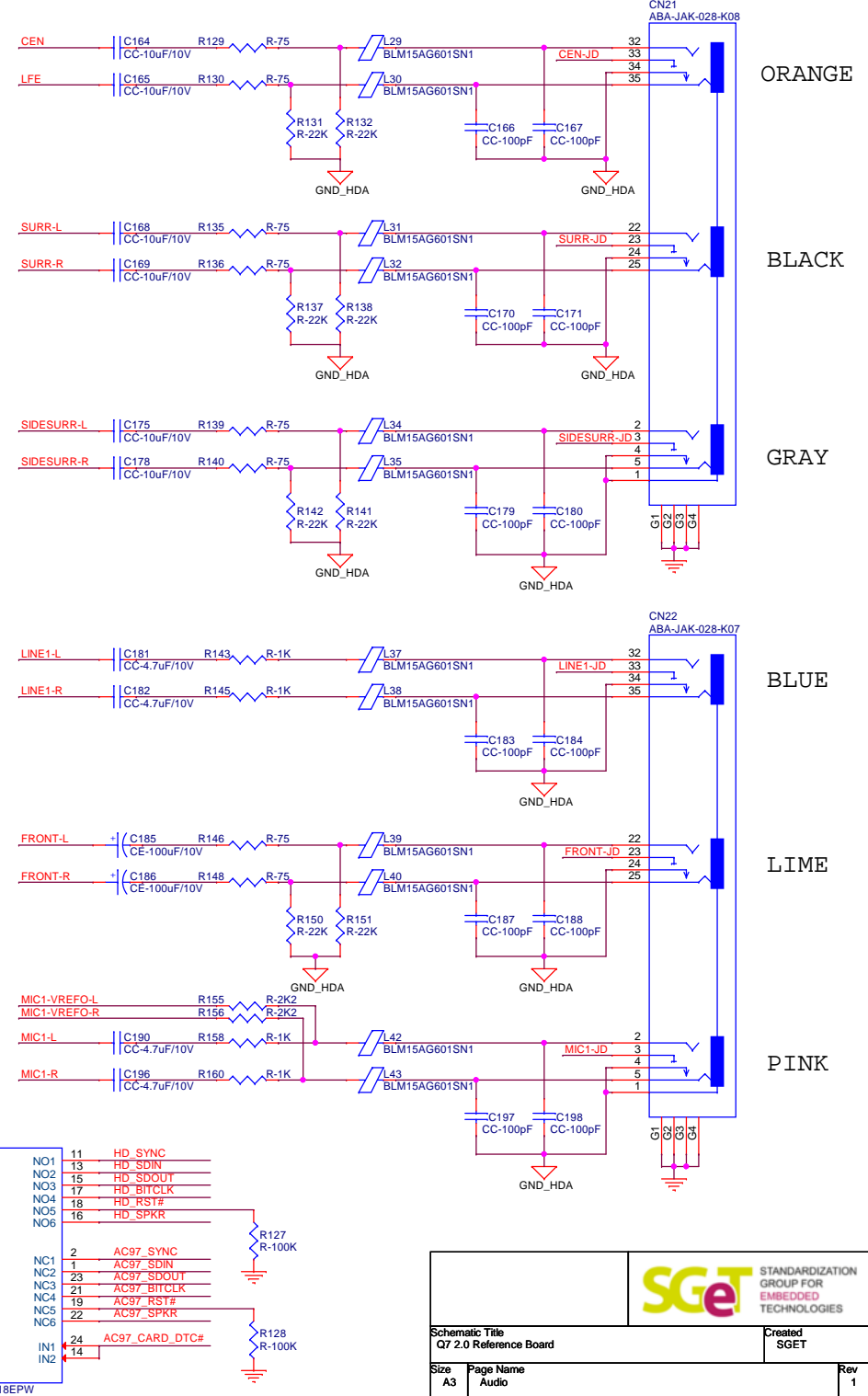
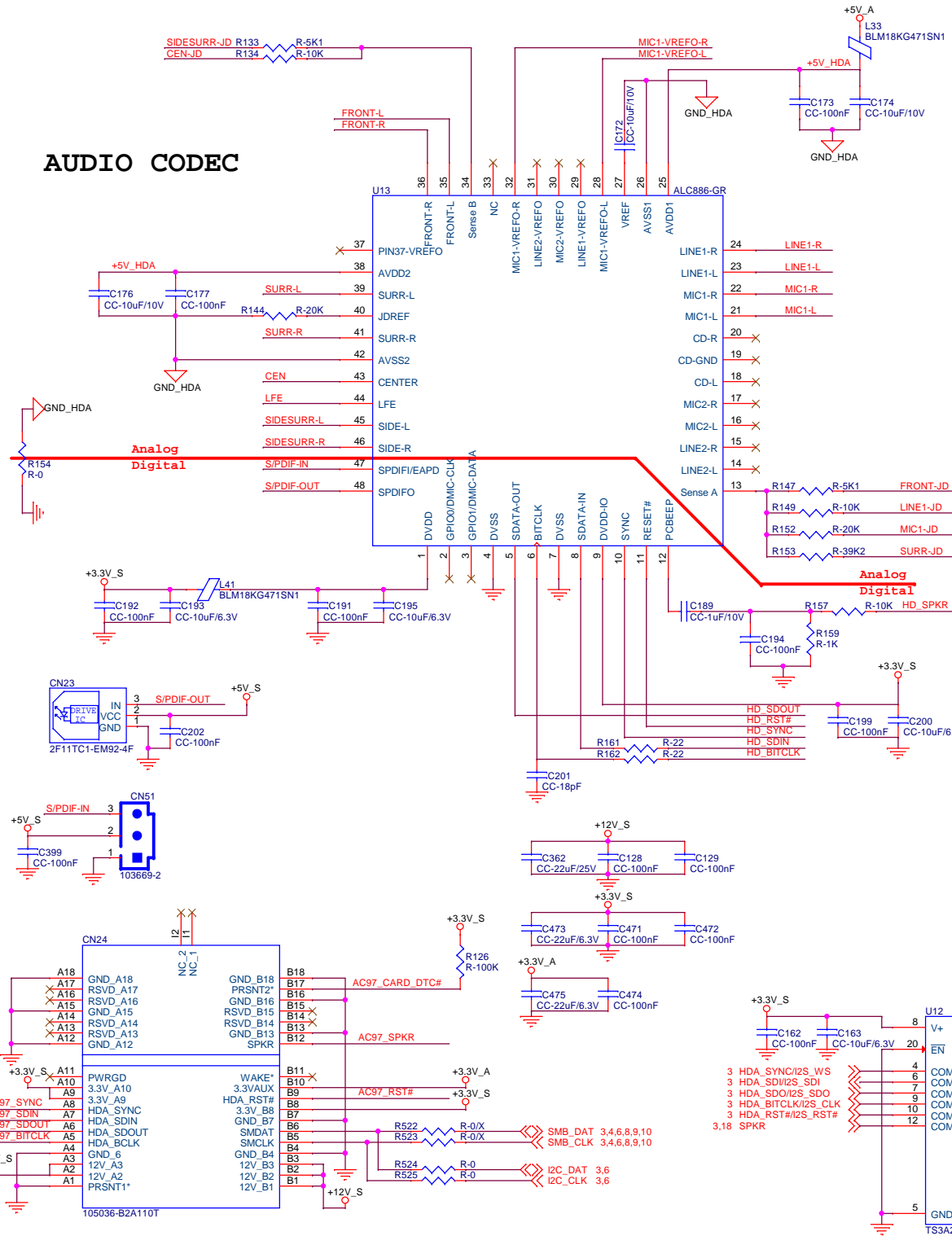
SATA 1



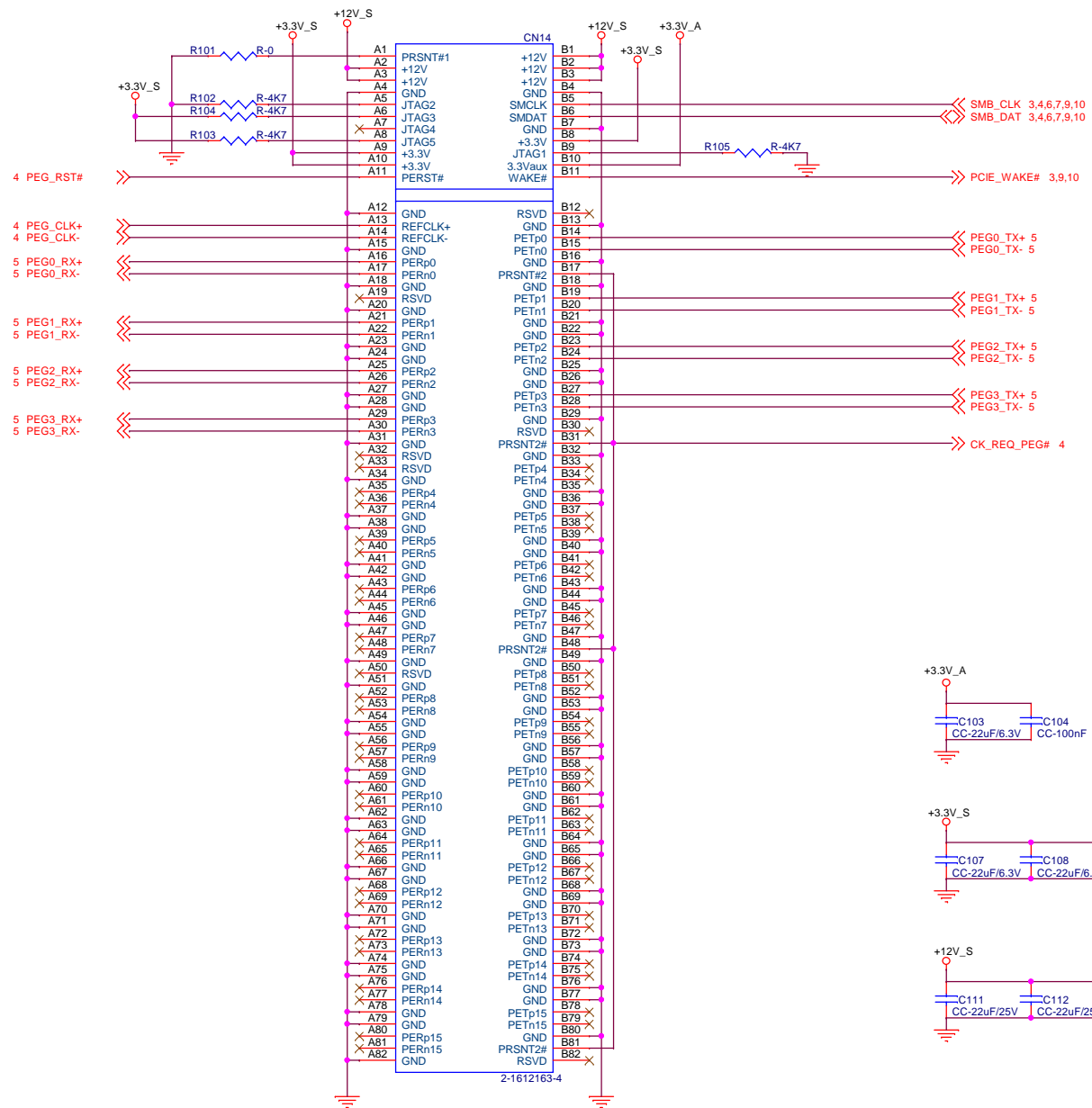
Schematic Title Q7 2.0 Reference Board		Created SGET
Size A3	Page Name Sata, Feature connector,LPC	Rev 1
Date: Wednesday, December 16, 2015	Sheet 6	of 23



AUDIO CODEC



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Schematic Title Q7 2.0 Reference Board		Created SGE
Size A3	Page Name Audio	Rev 1
Date: Wednesday, December 16, 2015		Sheet 7 of 23

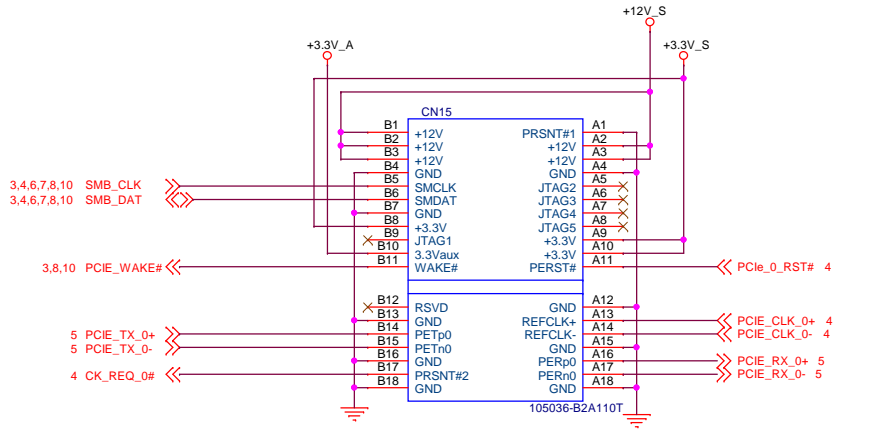


PCIeX x16

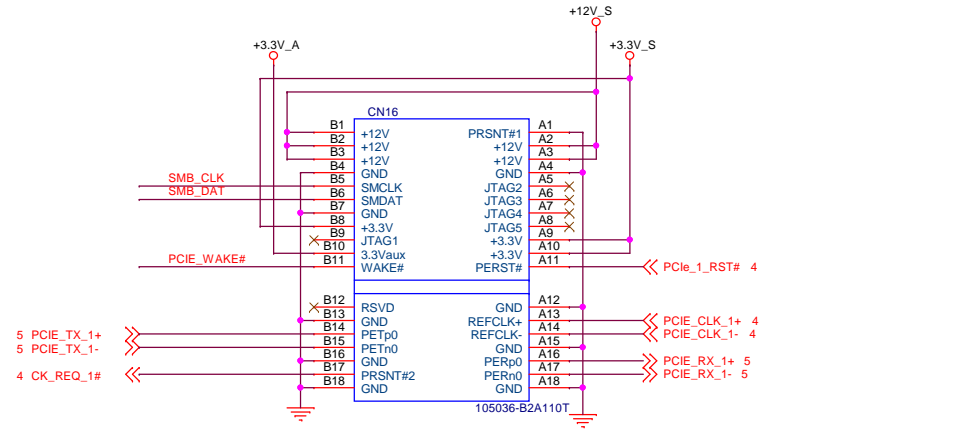


Schematic Title Q7 2.0 Reference Board		Created SGET
Size A3	Page Name PCIeX16	Rev 1
Date: Wednesday, December 16, 2015	Sheet 8	of 23

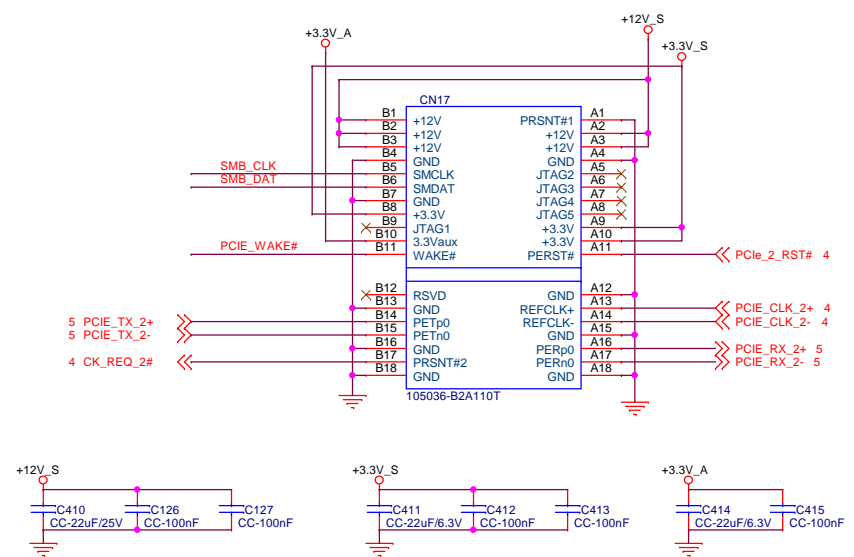
PCI Express X1 SLOT 1



PCI Express X1 SLOT 2

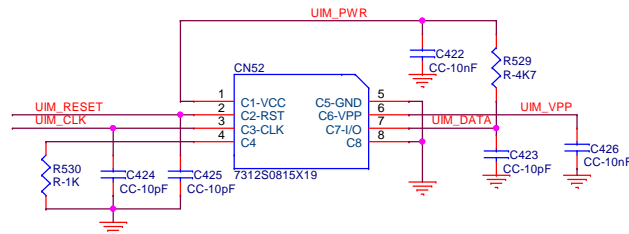
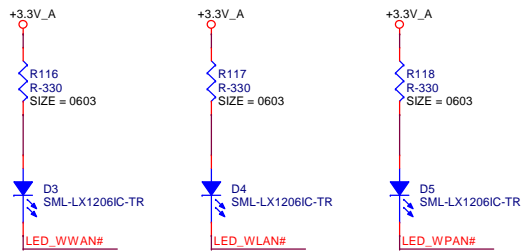
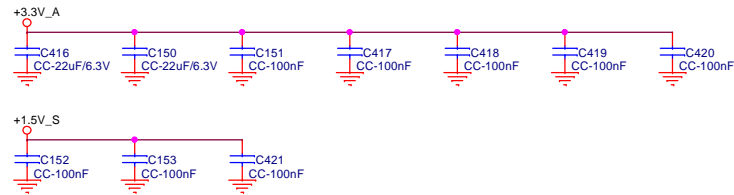
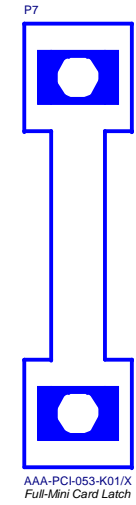
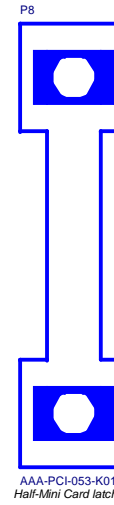
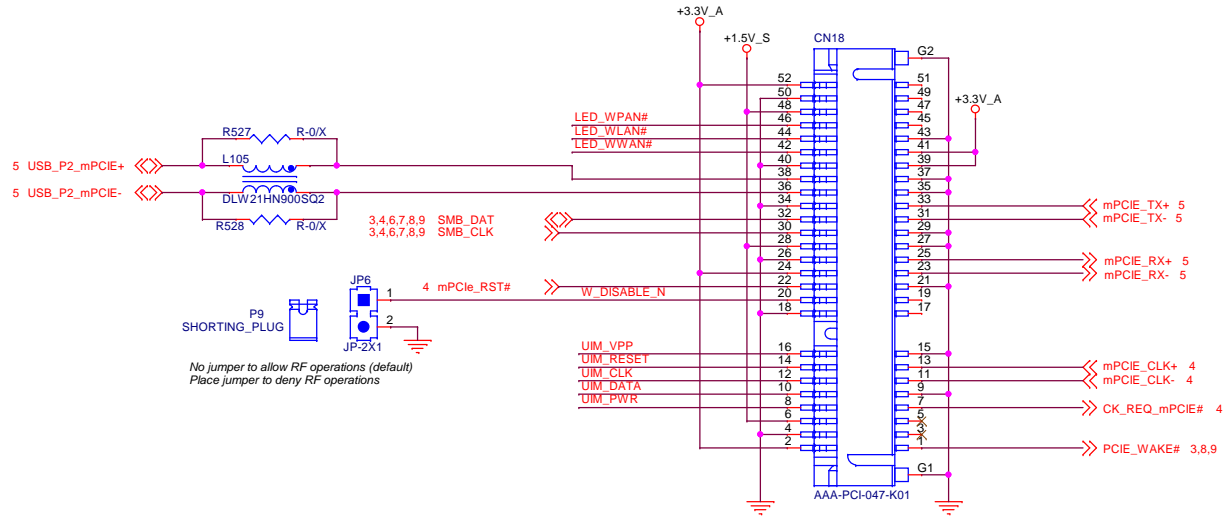


PCI Express X1 SLOT 3



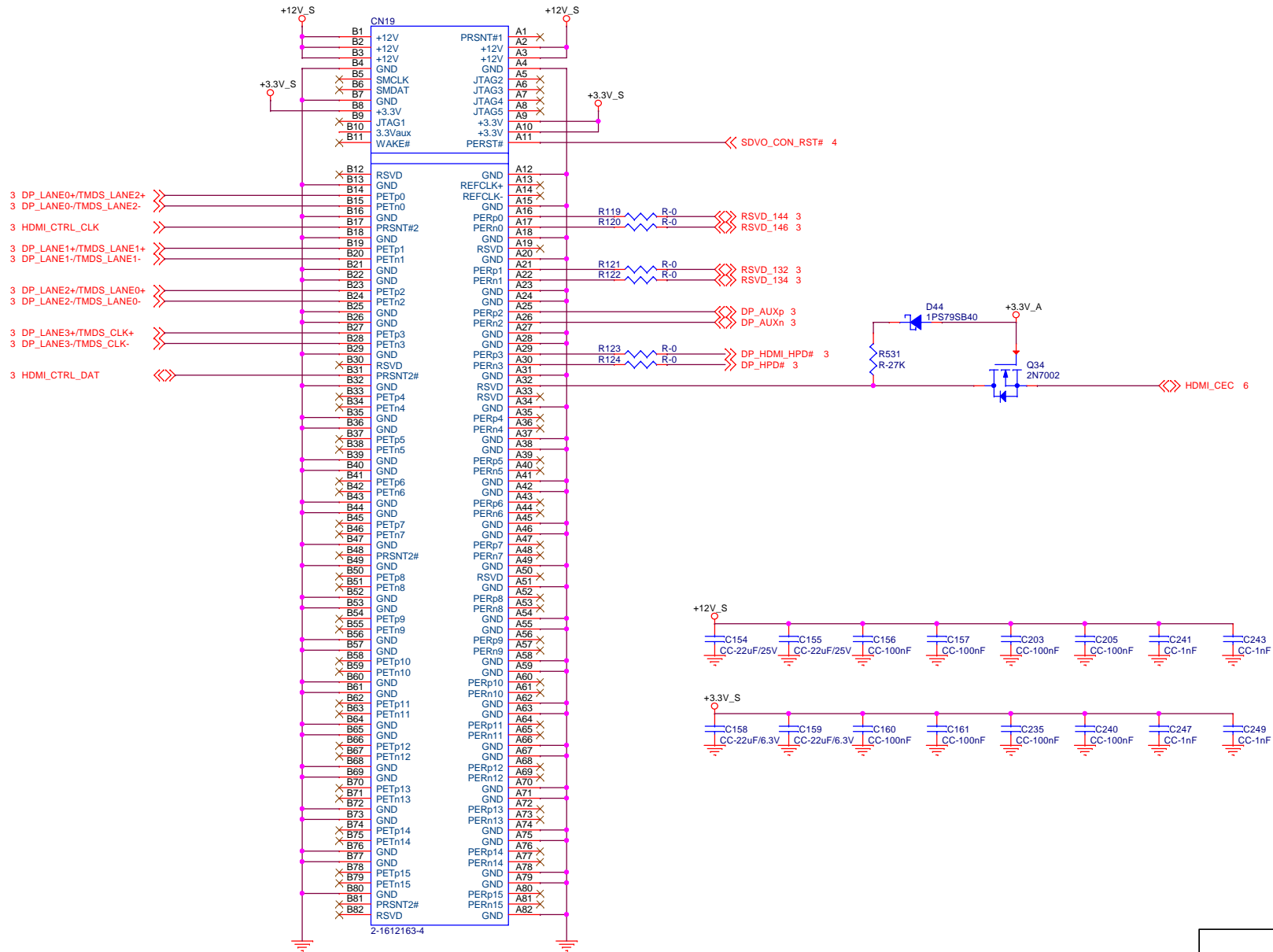
		STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES	
		Schematic Title Q7 2.0 Reference Board	
Size A3		Page Name PCIeX1	
Date Wednesday, December 16, 2015		Created SGET	
Sheet 9		of 23	
Rev 1			

PCI Express Mini Card



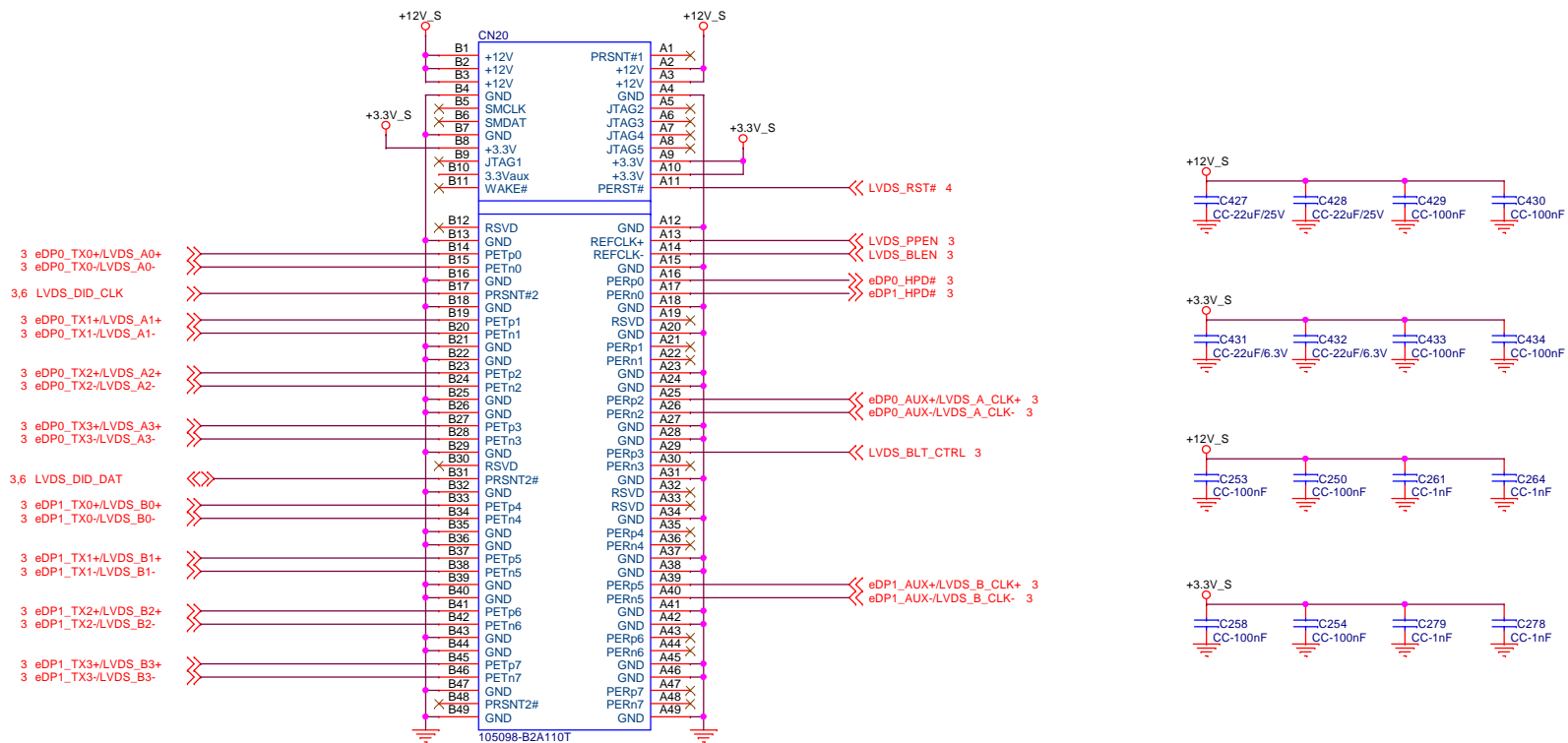
		SGE STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES	
Schematic Title Q7 2.0 Reference Board			Created SGET
Size A3	Page Name mPCIe	Rev 1	
Date: Wednesday, December 16, 2015	Sheet 10	of 23	

HDMI / DISPLAYPORT



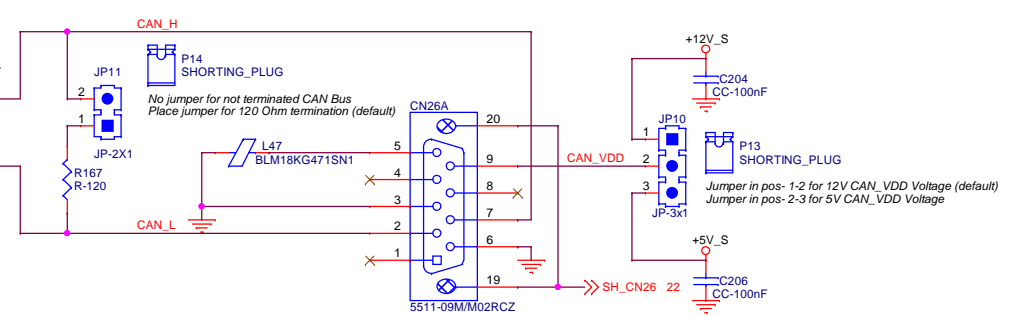
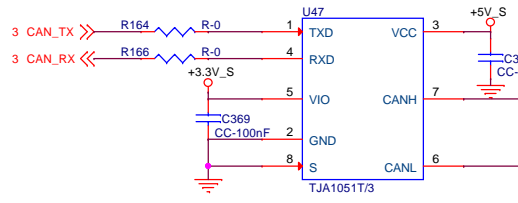
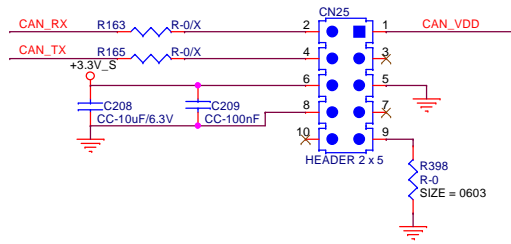
Schematic Title Q7 2.0 Reference Board		Created SGET
Size A3	Page Name HDMI,DP	Rev 1
Date: Wednesday, December 16, 2015	Sheet 11	of 23

LVDS/eDP

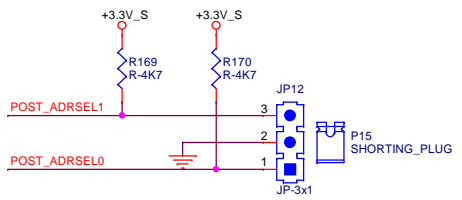


Schematic Title Q7 2.0 Reference Board		Created SGET
Size A3	Page Name LVDS	Rev 1
Date: Wednesday, December 16, 2015	Sheet 12	of 23

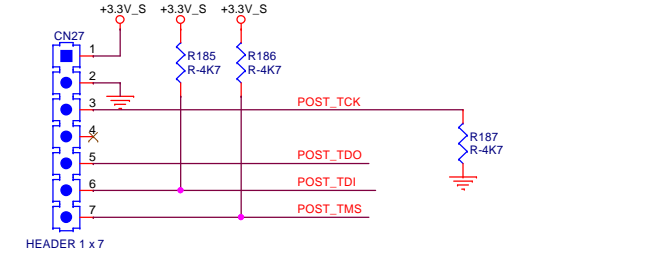
CAN-BUS



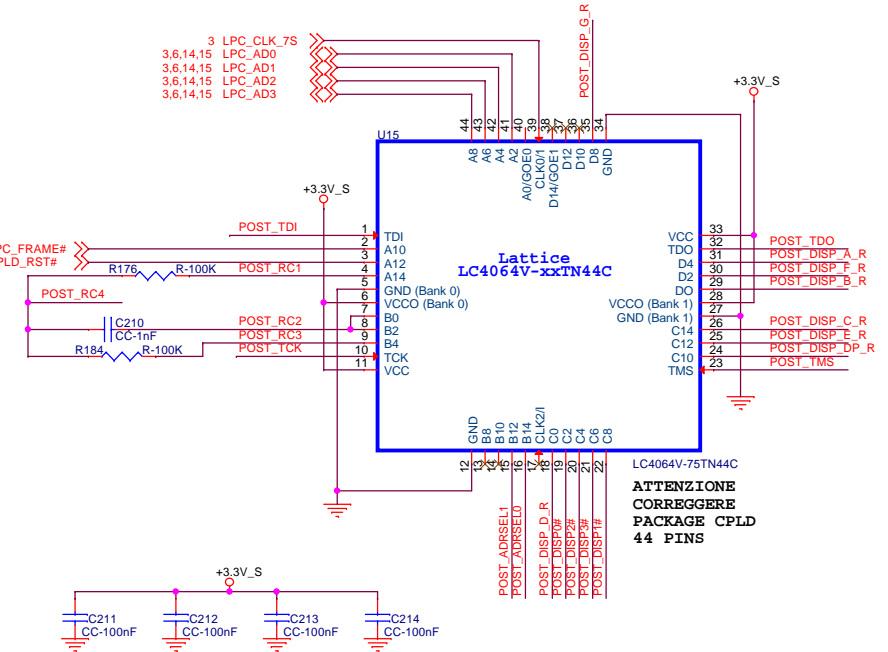
LPC POSTcode



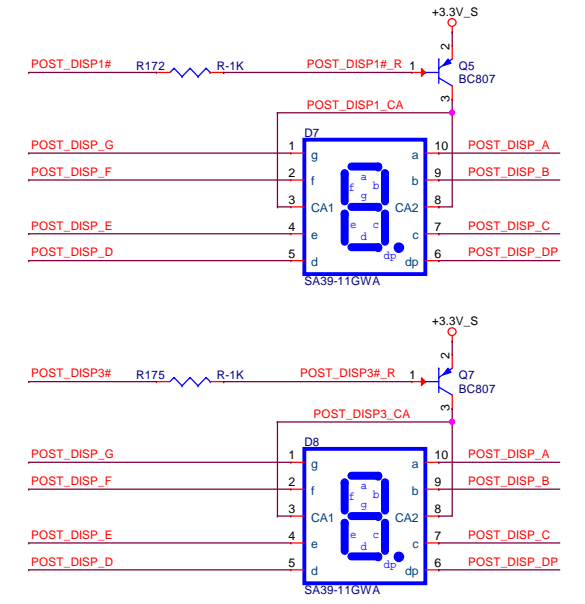
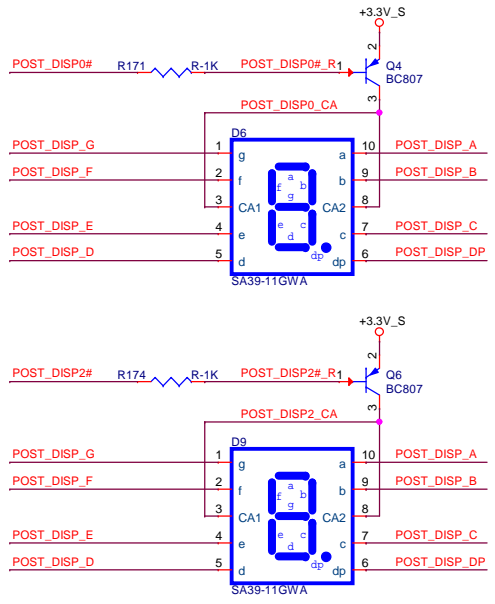
POST_DISP A R	R173	R-100	SIZE = 0603	POST_DISP A
POST_DISP B R	R177	R-100	SIZE = 0603	POST_DISP B
POST_DISP C R	R178	R-100	SIZE = 0603	POST_DISP C
POST_DISP DP R	R179	R-100	SIZE = 0603	POST_DISP DP
POST_DISP D R	R180	R-100	SIZE = 0603	POST_DISP D
POST_DISP E R	R181	R-100	SIZE = 0603	POST_DISP E
POST_DISP F R	R182	R-100	SIZE = 0603	POST_DISP F
POST_DISP G R	R183	R-100	SIZE = 0603	POST_DISP G

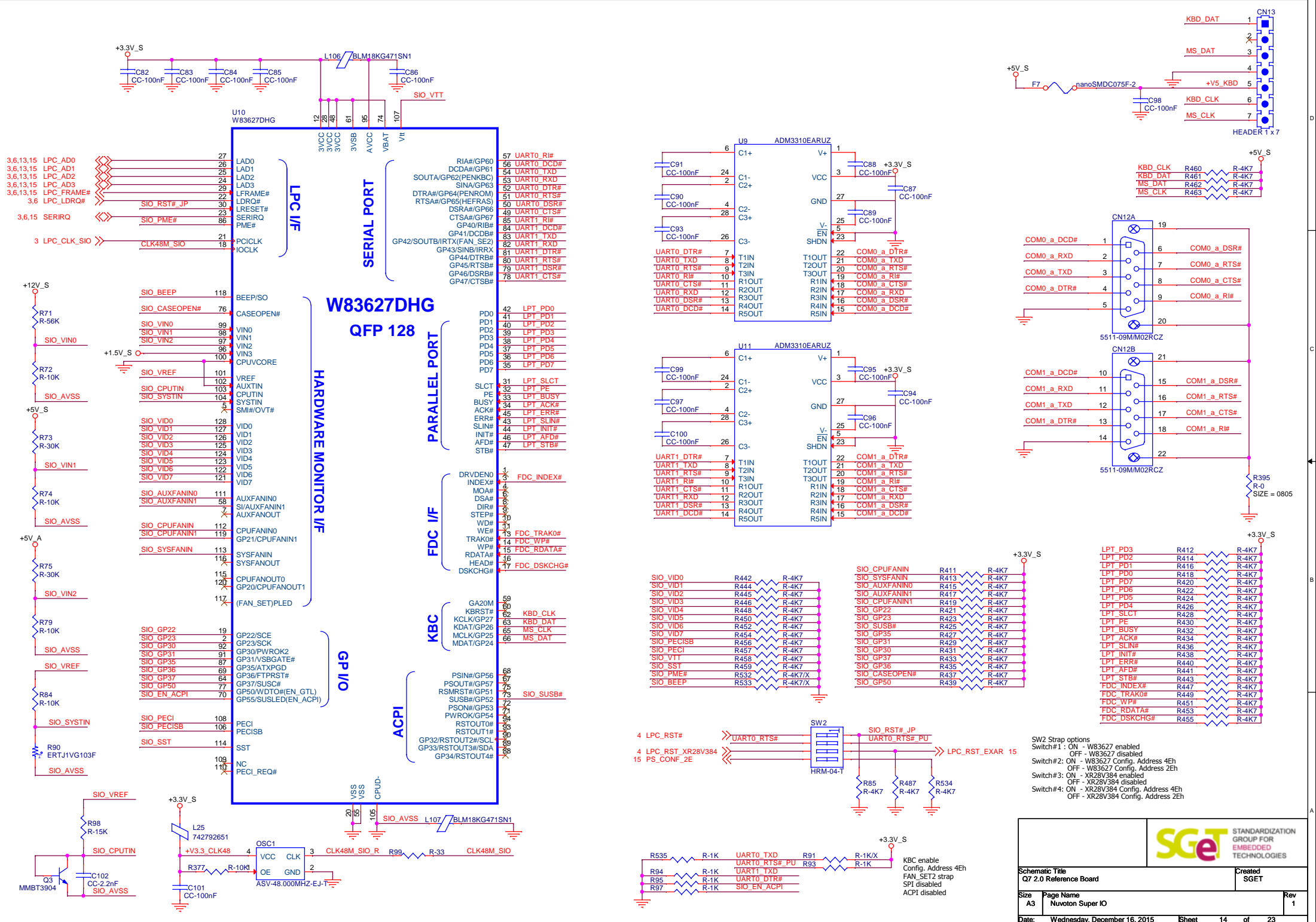


Jumper in pos- 1-2 for address 90 / 94H
Jumper in pos- 2-3 for address 80 / 84H (default)



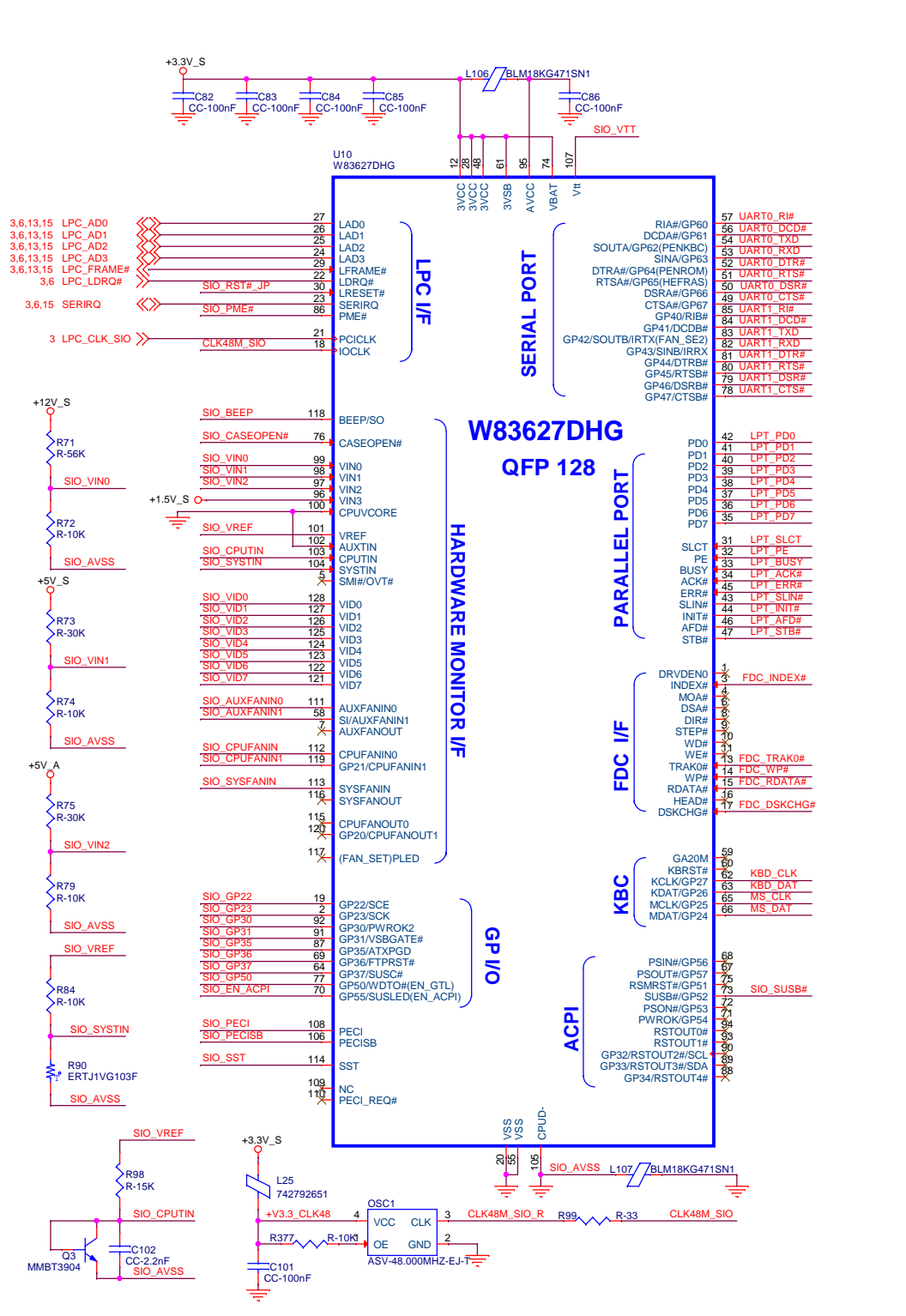
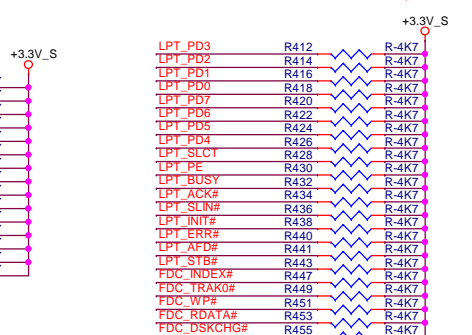
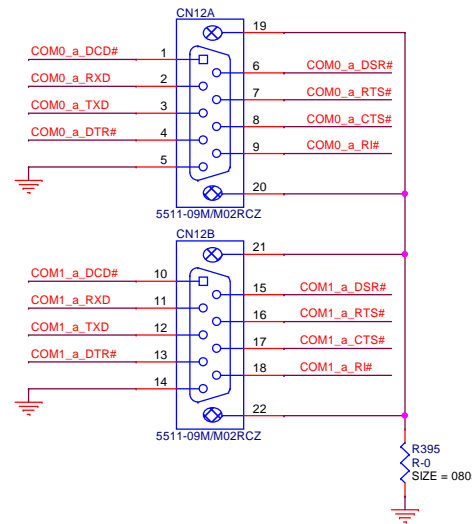
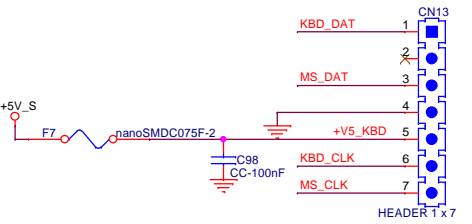
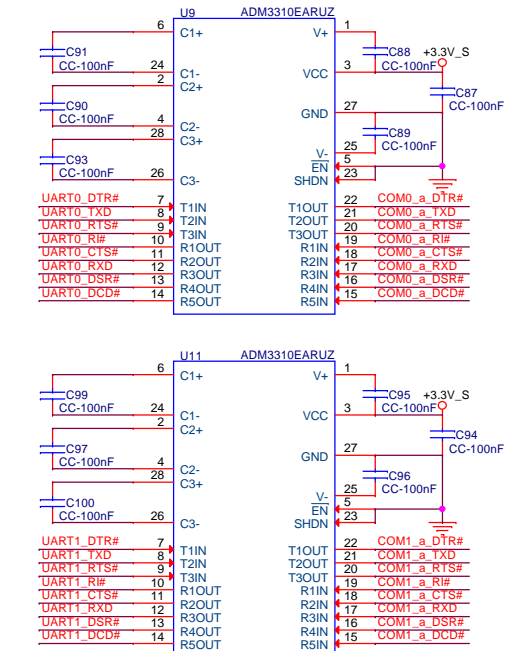
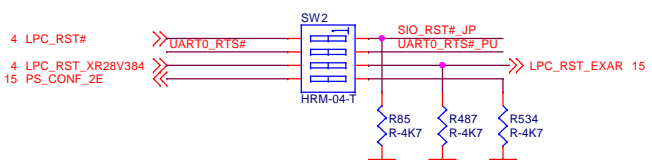
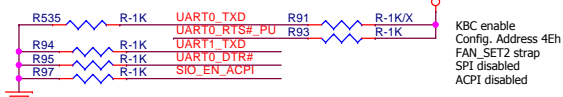
ATTENZIONE
CORREGGERE
PACKAGE CPLD
44 PINS

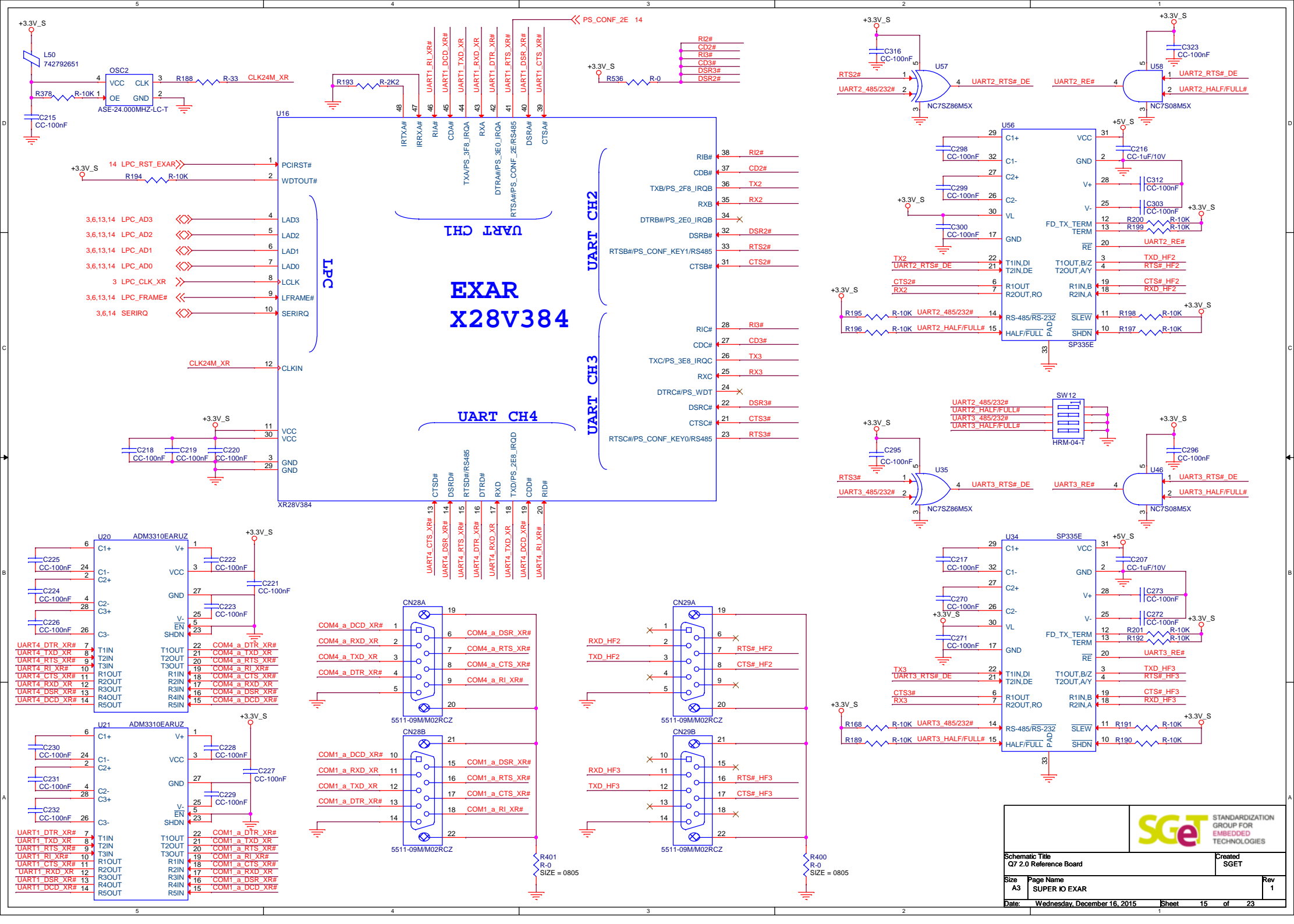




SW2 Strap options
 Switch#1: ON - W83627 enabled
 OFF - W83627 disabled
 Switch#2: ON - W83627 Config, Address 4Eh
 OFF - W83627 Config, Address 2Eh
 Switch#3: ON - XR28V384 enabled
 OFF - XR28V384 disabled
 Switch#4: ON - XR28V384 Config, Address 4Eh
 OFF - XR28V384 Config, Address 2Eh

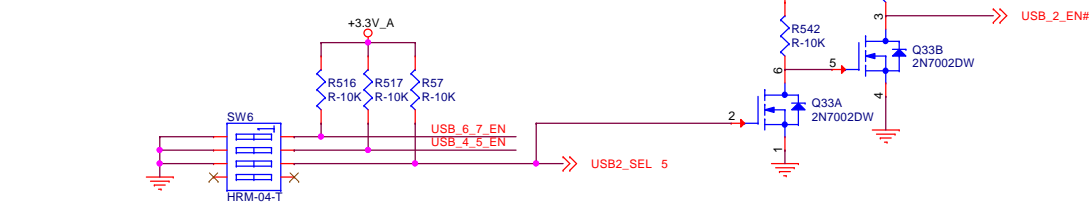
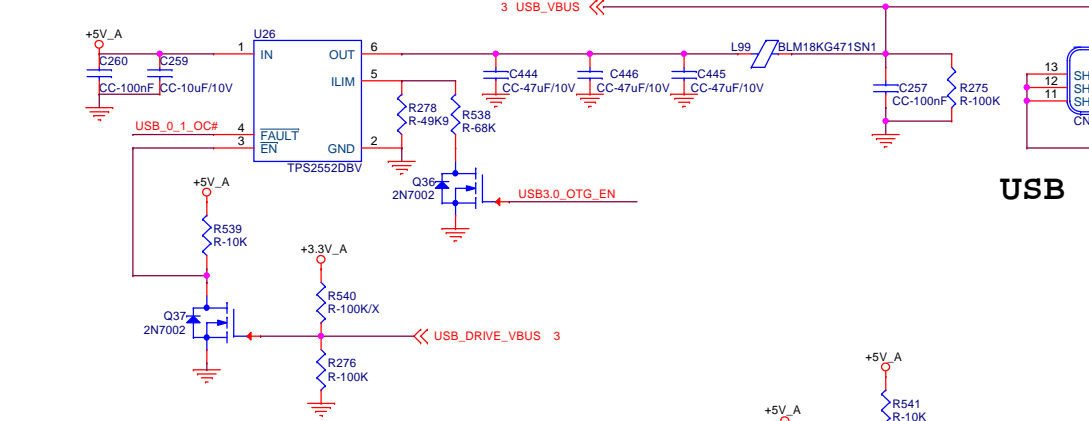
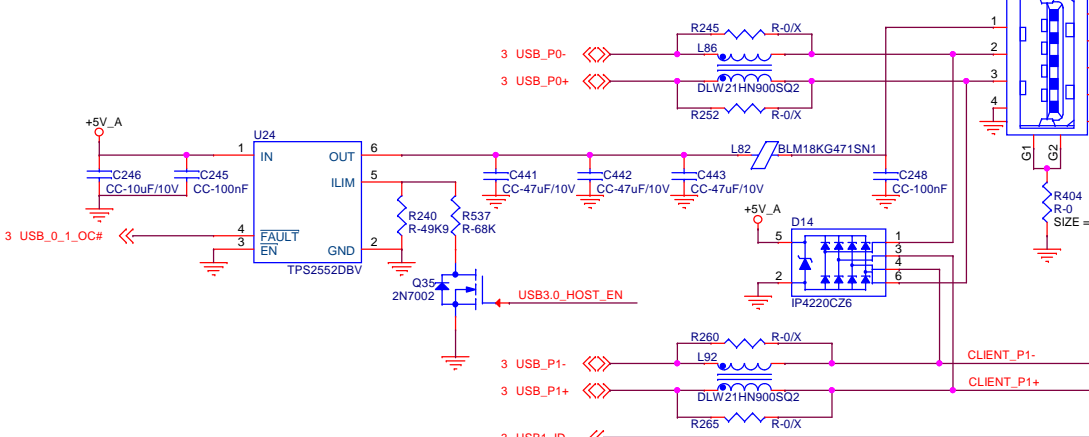
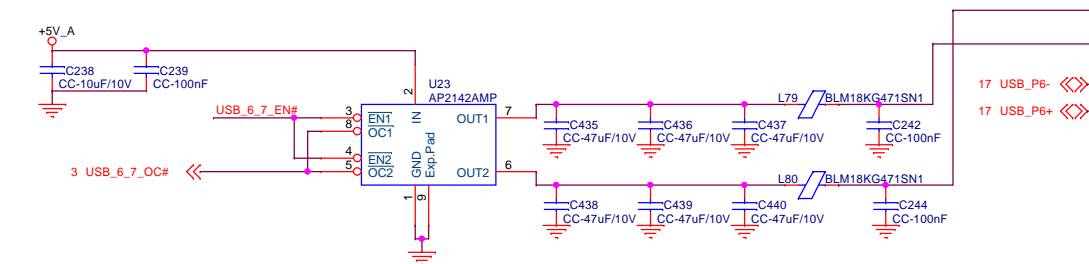
Schematic Title Q7 2.0 Reference Board		Created SGET
Size A3	Page Name Nuoton Super IO	Rev 1
Date: Wednesday, December 16, 2015		Sheet 14 of 23





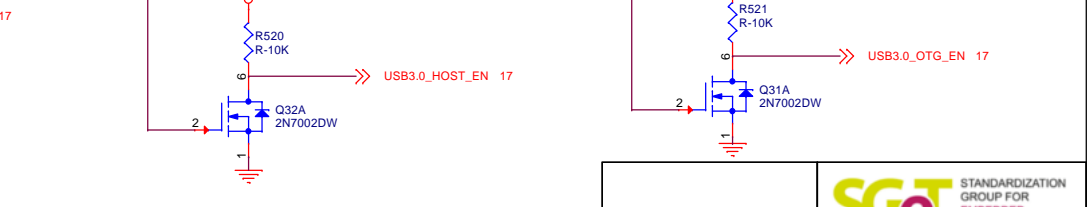
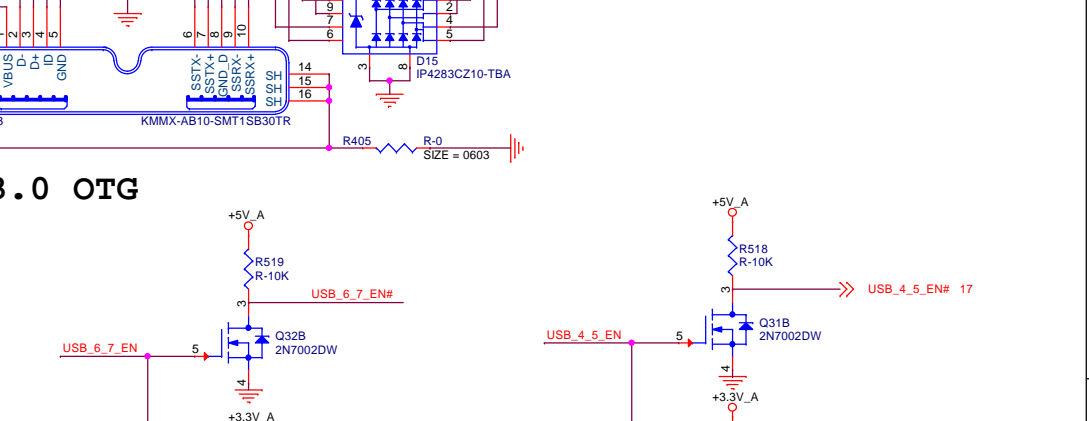
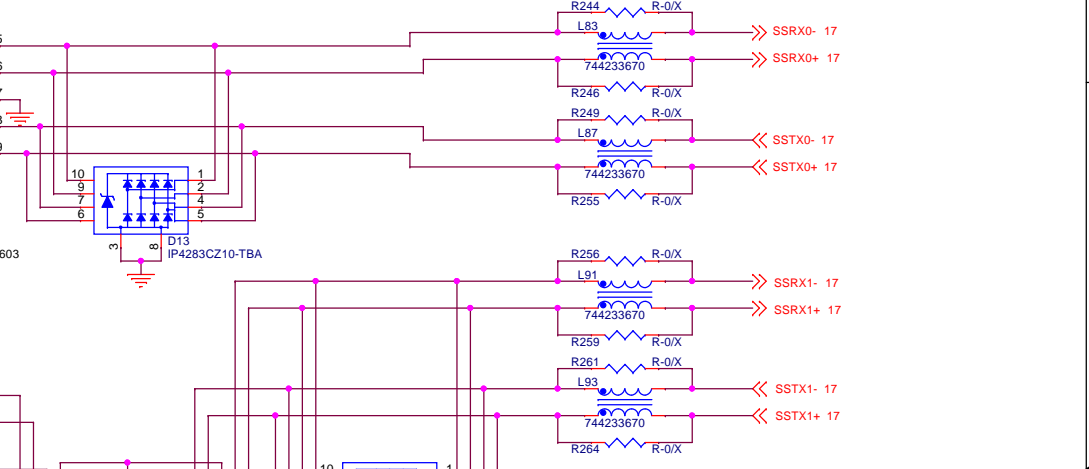
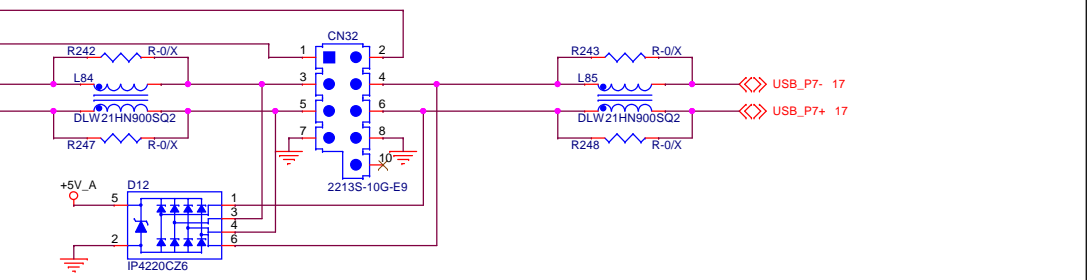
		STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES
Schematic Title Q7 2.0 Reference Board		Created SGET
Size A3	Page Name SUPER IO EXAR	Rev 1
Date : Wednesday, December 16, 2015		Sheet : 15 of 23

USB 3.0 HOST

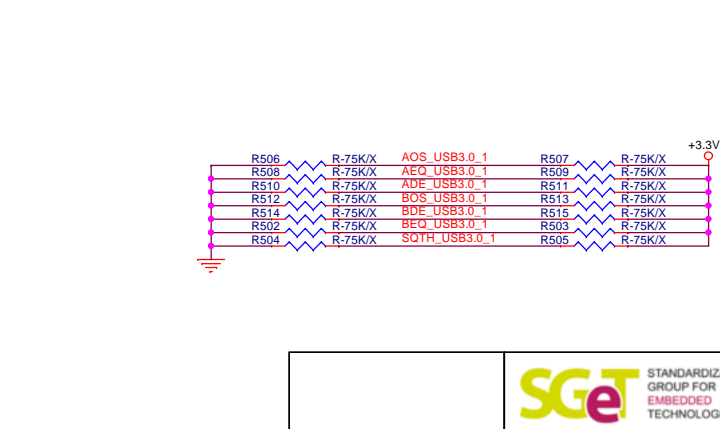
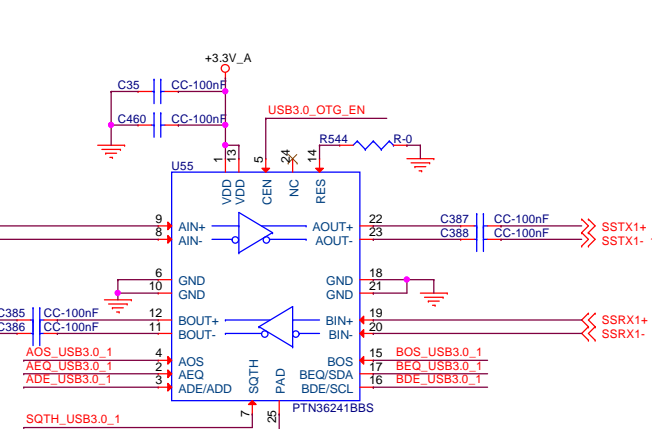
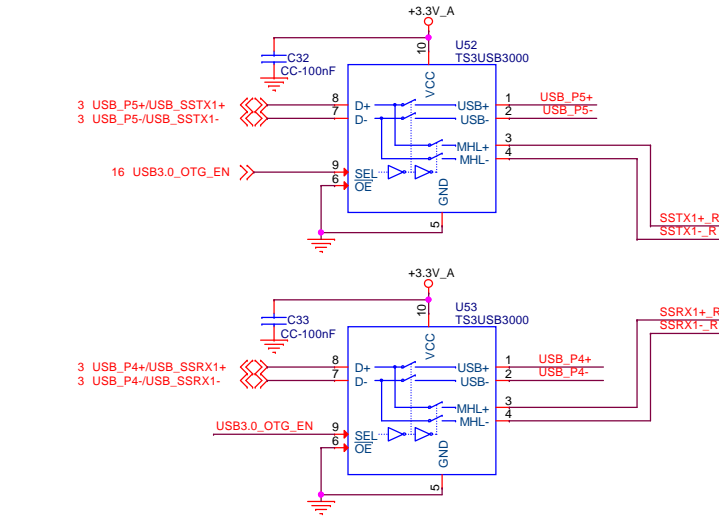
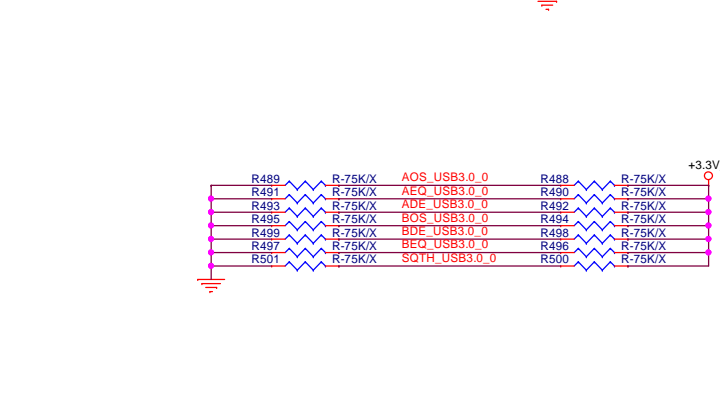
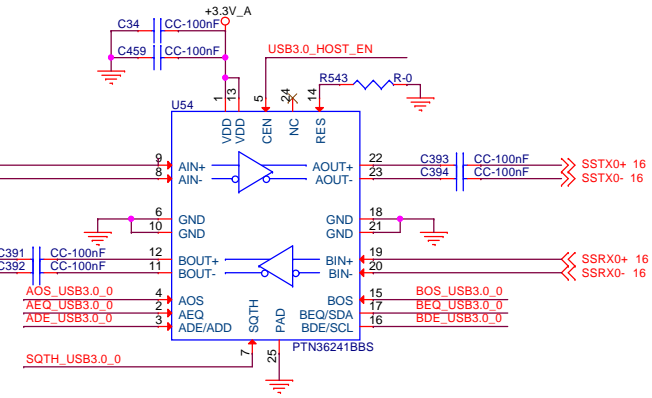
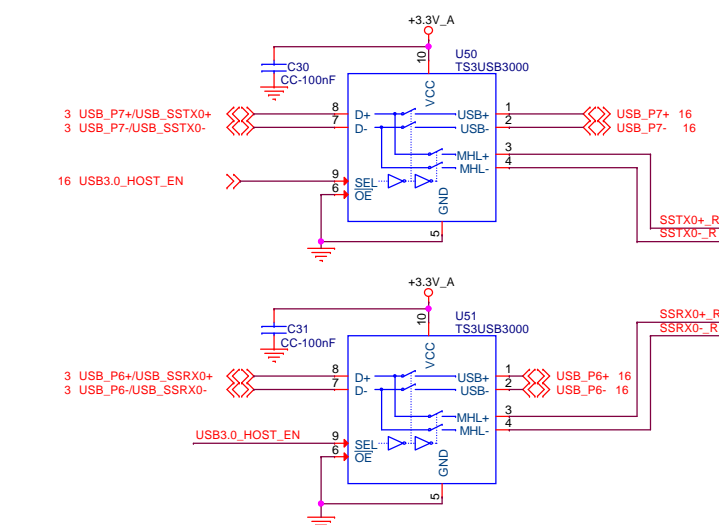
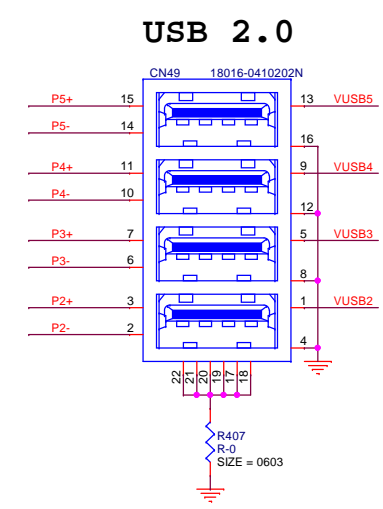
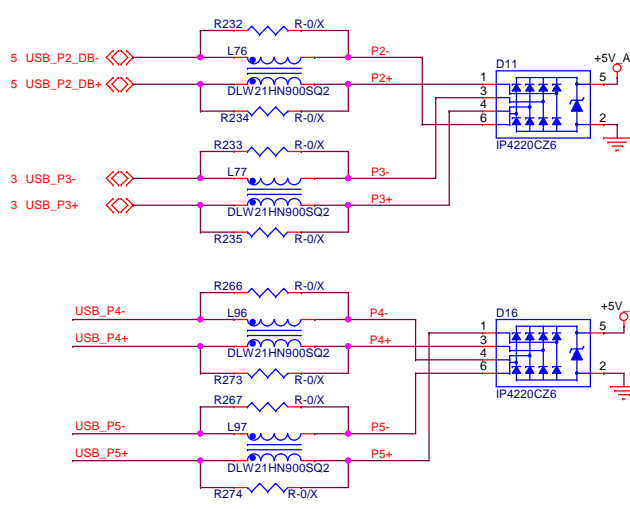
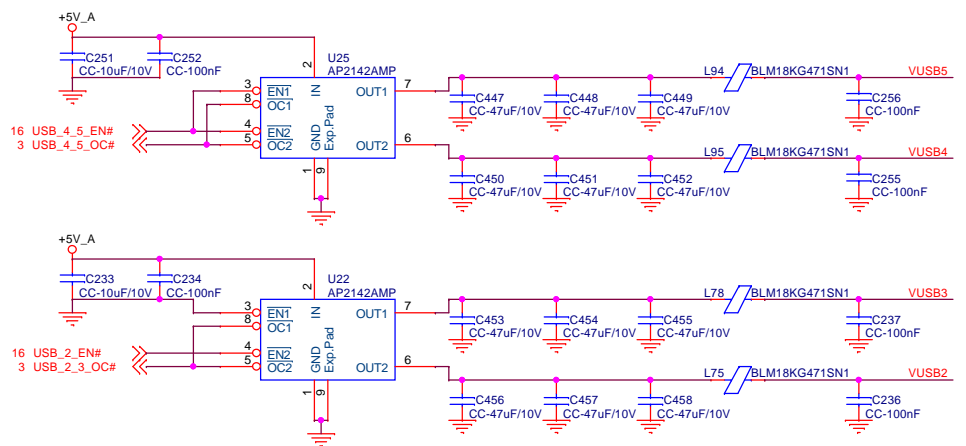


SW6 options
 Switch #1: ON - USB 3.0 port #0 enabled
 OFF - USB 2.0 ports #6 and #7 enabled
 Switch #2: ON - USB 3.0 port #1 enabled
 OFF - USB 2.0 ports #4 and #5 enabled
 Switch #3: ON - USB port #2 on type A Slot CN49
 OFF - USB port #2 on miniPCI-e Slot CN18

USB 3.0 OTG



Schematic Title Q7 2.0 Reference Board		Created SGET
Size A3	Page Name USB 3.0 / USB 2.0 INTERNAL	Rev 1
Date: Wednesday, December 16, 2015	Sheet 16	of 23

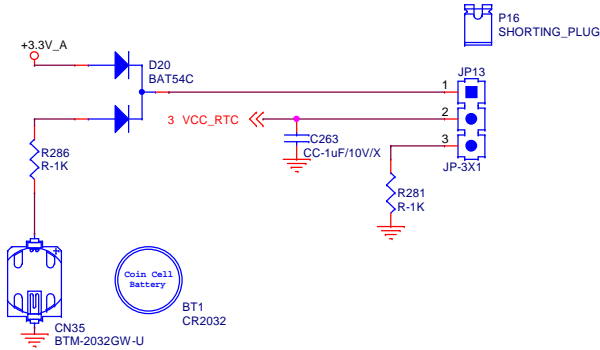


Schematic Title Q7 2.0 Reference Board		Created SGET
Size A3	Page Name USB 2.0 / USB SETUP	Rev 1
Date Wednesday, December 16, 2015	Sheet 17	of 23

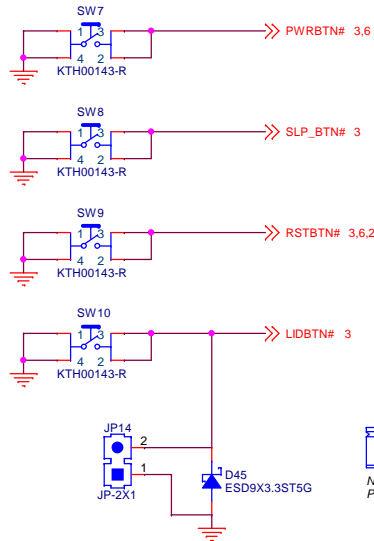


RTC/CMOS BATTERY

Place jumper pos. 1-2 for normal operations (default)
Place jumper pos. 2-3 for battery disconnection

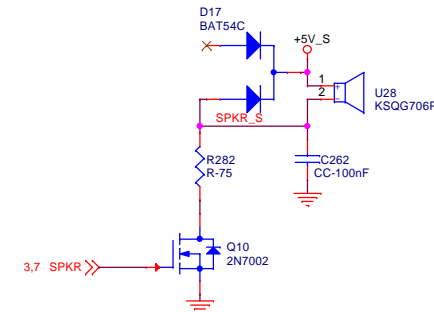


BUTTONS

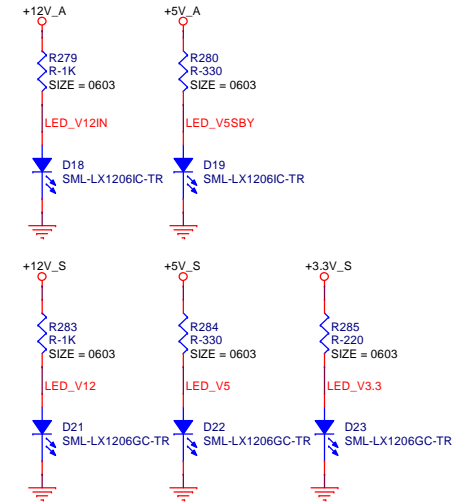


No jumper for normal working (default)
Place jumper to simulate activation of LIBBTN

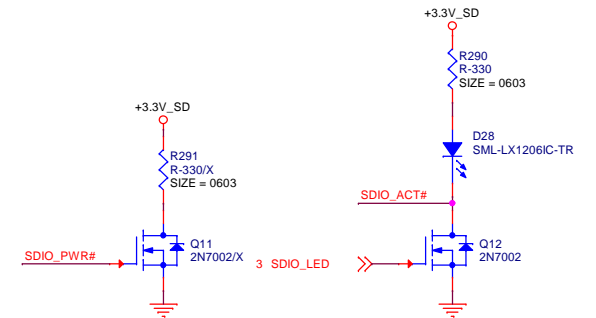
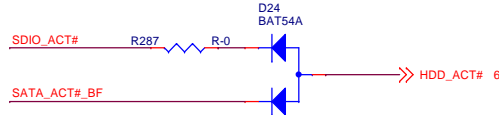
SPEAKER



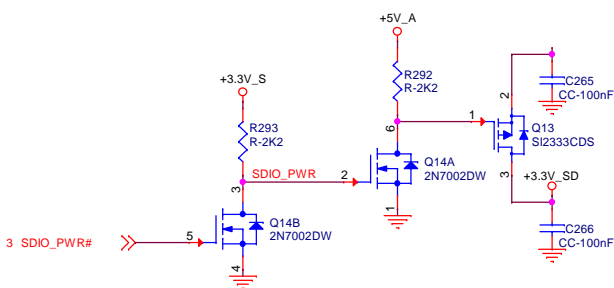
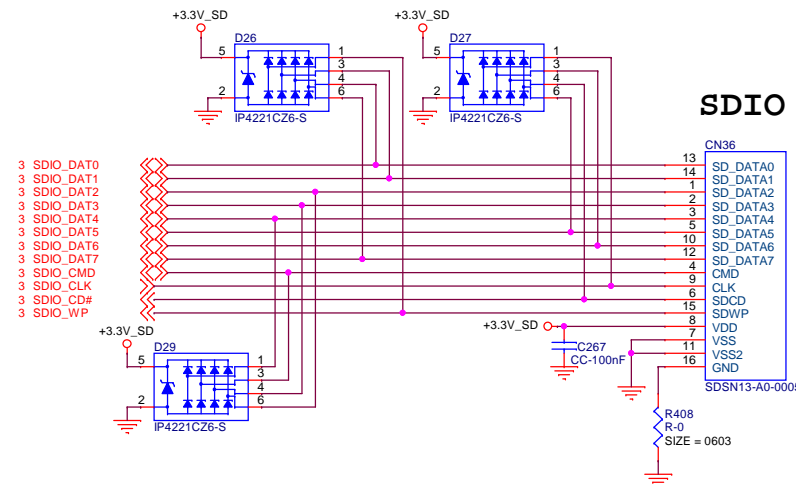
POWER LEDs



4 SATA_ACT#_BF

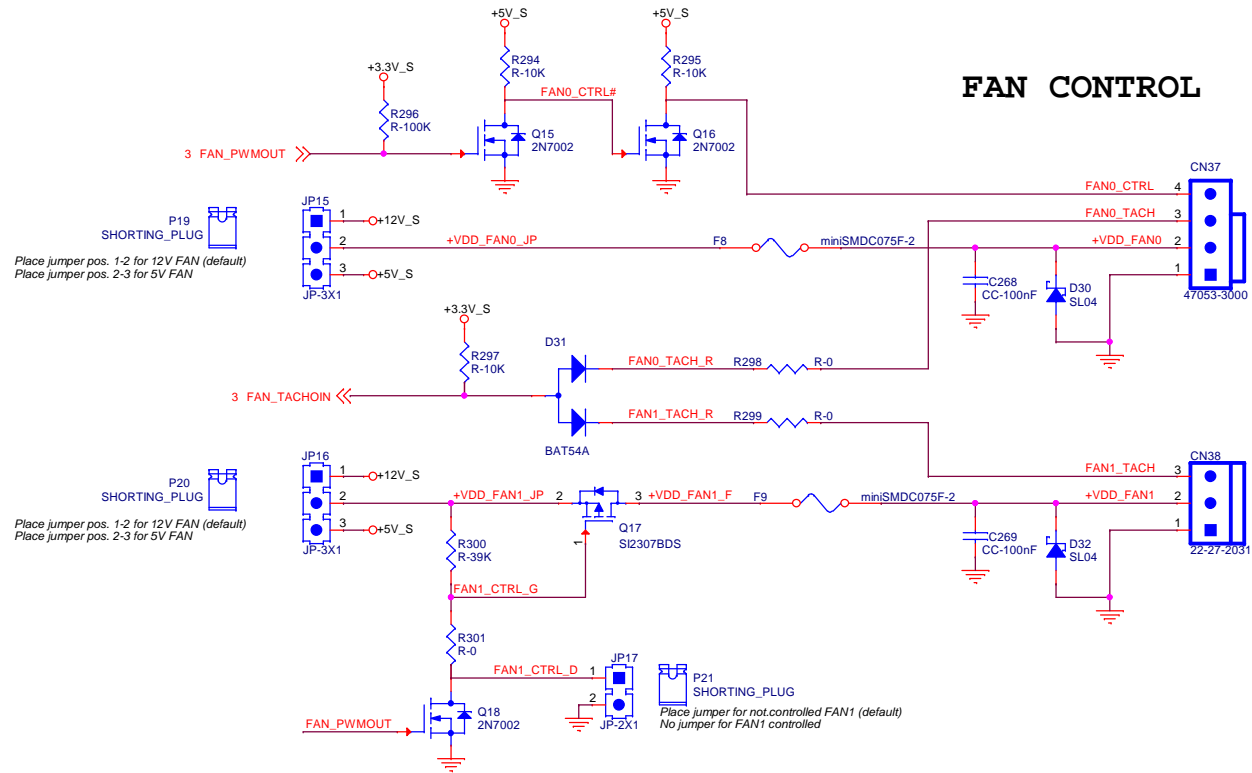


SDIO

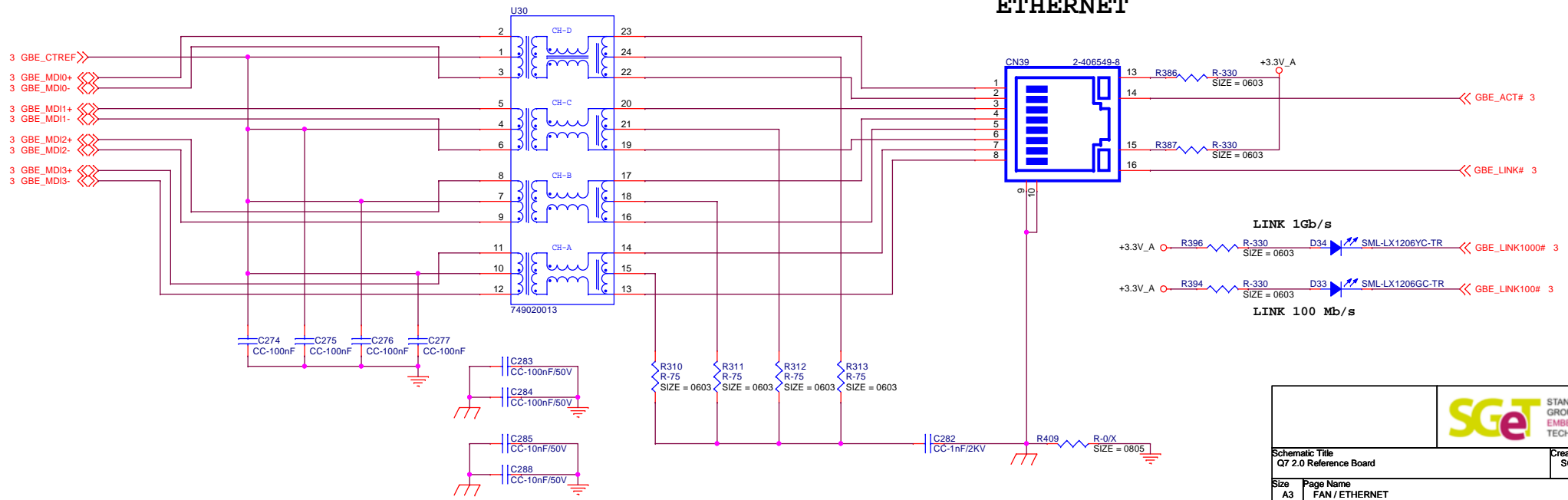


		STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES	
		Schematic Title Q7 2.0 Reference Board	
Size A3	Page Name SDIO/BATT/SPEAKER/BUTTONS/LEDS	Created SGET	Rev 1
Date: Wednesday, December 16, 2015		Sheet 18 of 23	

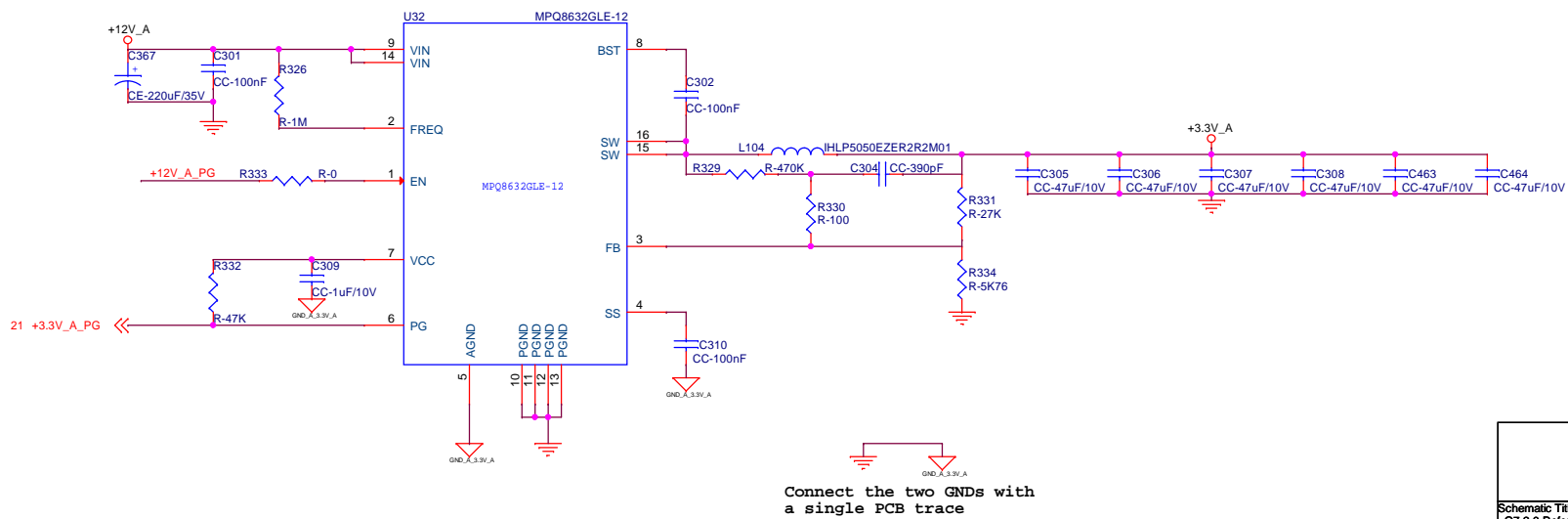
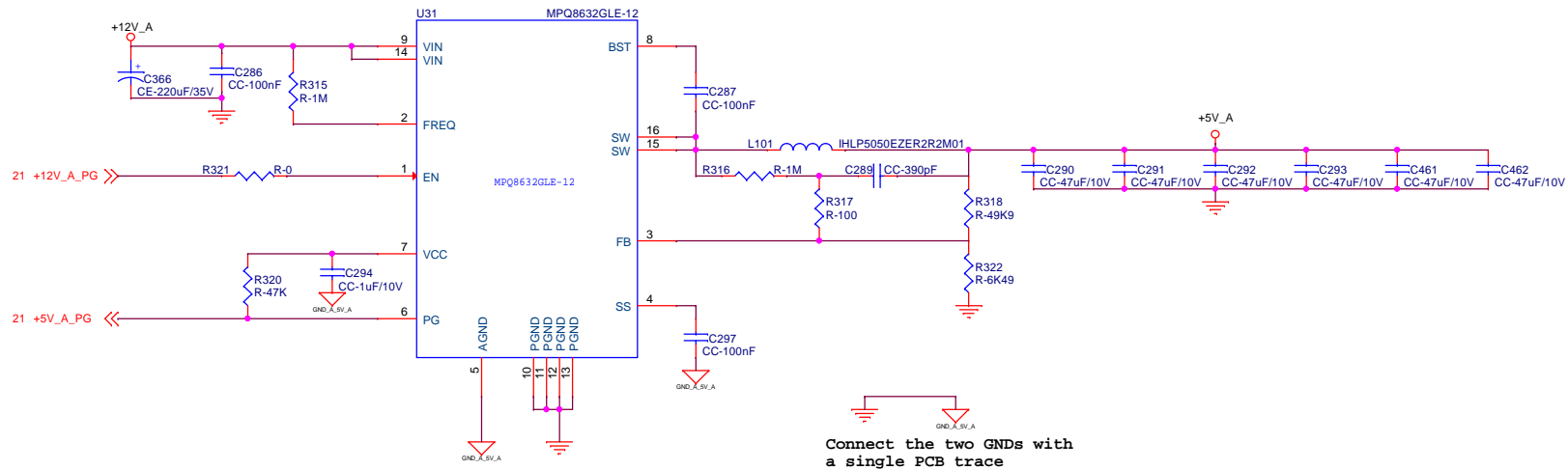
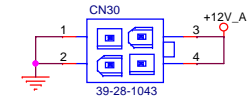
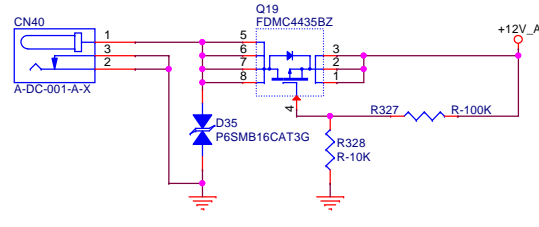
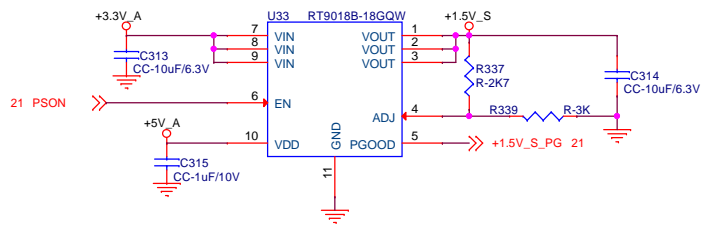
FAN CONTROL



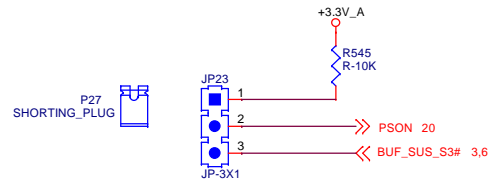
ETHERNET



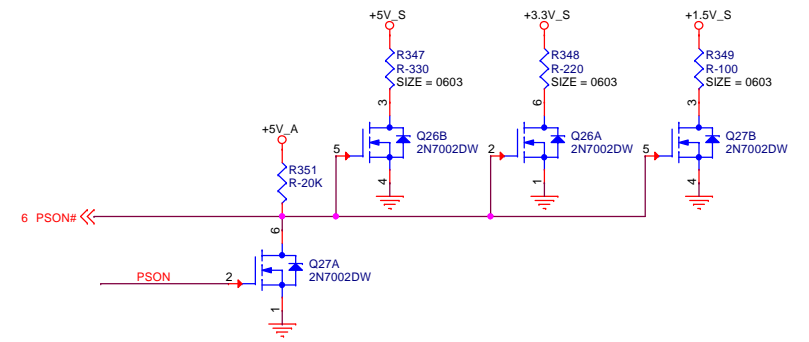
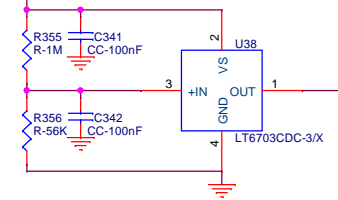
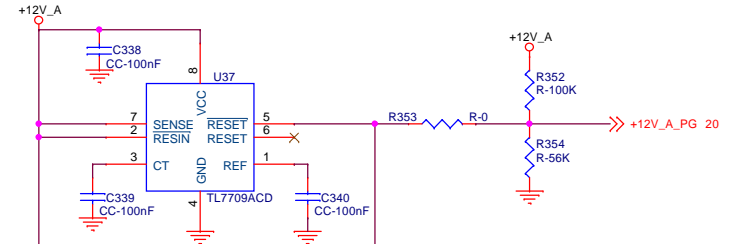
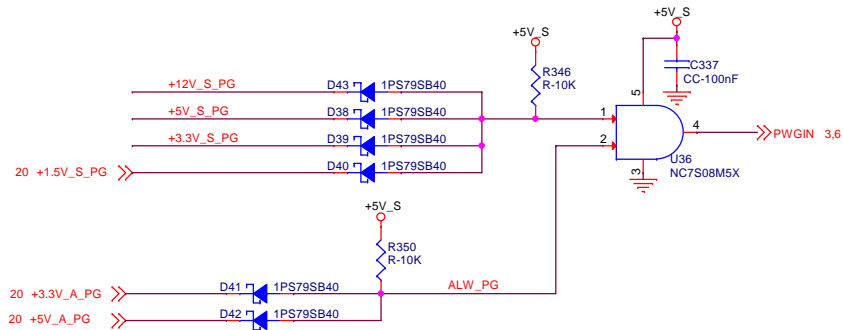
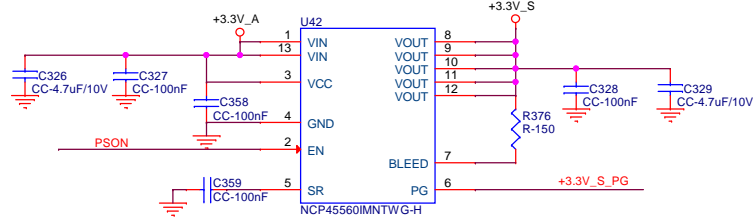
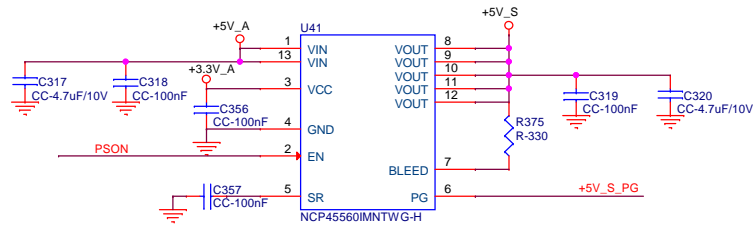
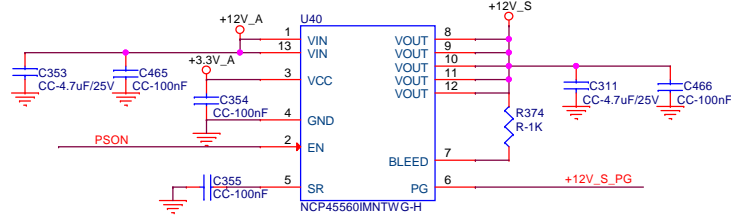
		STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES
Schematic Title Q7 2.0 Reference Board		Created SGET
Size A3	Page Name FAN / ETHERNET	Rev 1
Date: Wednesday, December 16, 2015		Sheet 19 of 23



		STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES	
		Schematic Title Q7 2.0 Reference Board	
Size A3		Page Name POWER 1	
Date: Wednesday, December 16, 2015		Sheet 20 of 23	
		Created SGET	
		Rev 1	



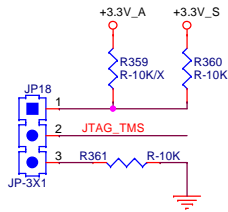
Place jumper pos. 1-2 for ATX PSU controlled mode(default)
Place jumper pos. 2-3 for ATX PSU in AT mode



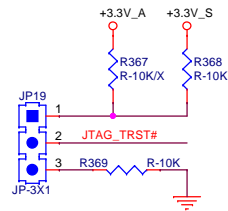
		STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES	
		Schematic Title Q7 2.0 Reference Board	
Size A3		Page Name POWER 2	
Date: Wednesday, December 16, 2015		Sheet 21 of 23	
Created SGET		Rev 1	



Place jumper pos. 1-2 to connect RSTBTN# to SRST# (default)
Place jumper pos. 2-3 to connect JTAG_TRST# to SRST#



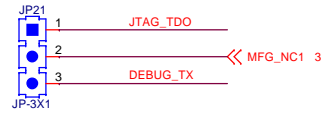
Place jumper pos. 1-2 to place pull-up on JTAG_TMS (default)
Place jumper pos. 2-3 to place pull-down on JTAG_TMS



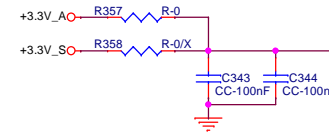
Place jumper pos. 1-2 to place pull-up on JTAG_TRST# (default)
Place jumper pos. 2-3 to place pull-down on JTAG_TRST#



Place jumper pos. 1-2 to connect JTAG (default)
Place jumper pos. 2-3 to connect Debug UART

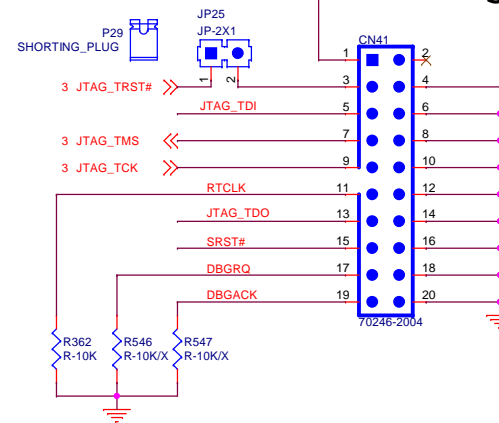


Place jumper pos. 1-2 to connect JTAG (default)
Place jumper pos. 2-3 to connect Debug UART

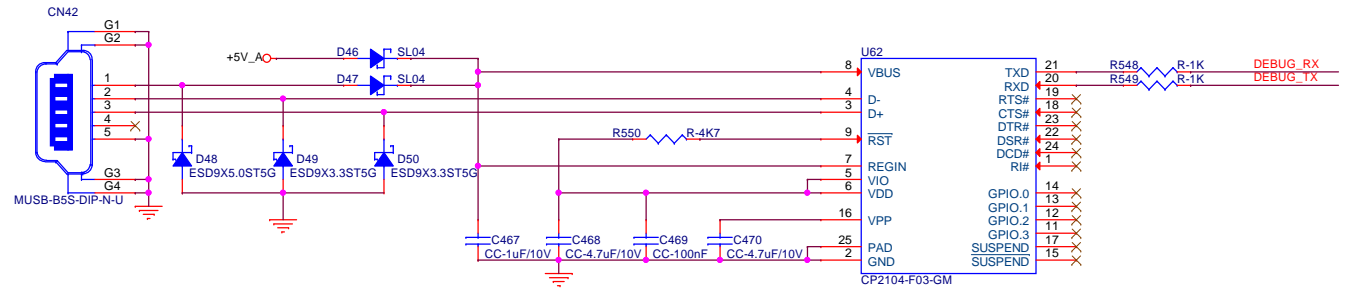


JTAG connector

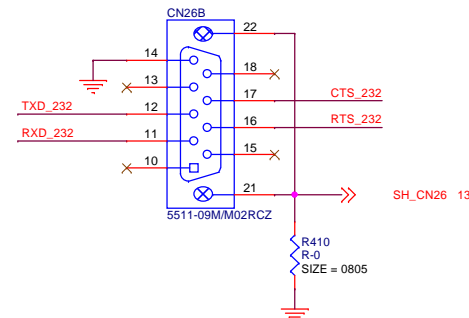
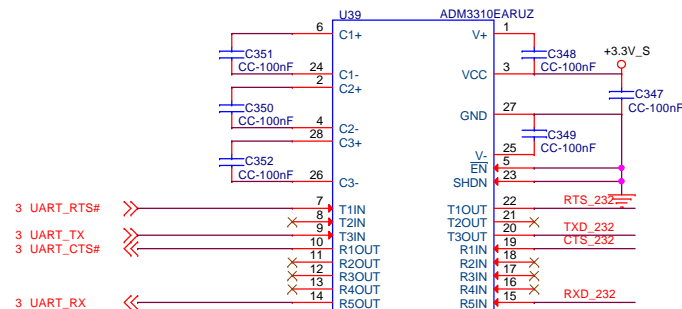
No jumper for JTAG_TRST# signal externally not available
Place jumper for JTAG_TRST# signal externally available (default)



Debug UART

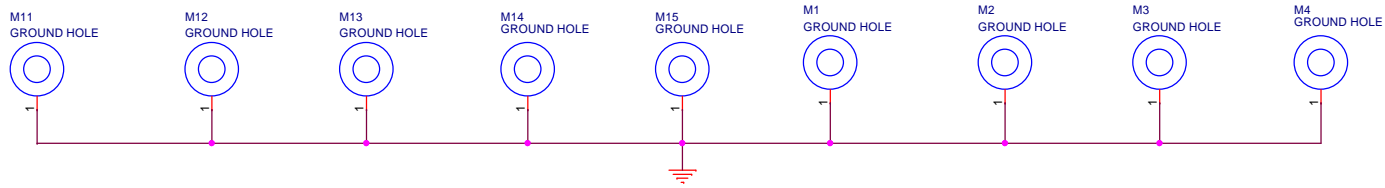


Qseven UART

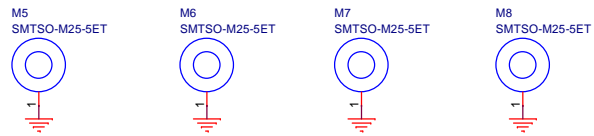


Schematic Title Q7 2.0 Reference Board		Created SGET
Size A3	Page Name DEBUG UART	Rev 1
Date: Wednesday, December 16, 2015	Sheet 22	of 23

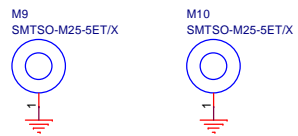
Carrier HOLES



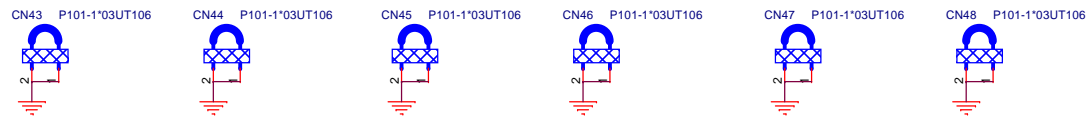
Qseven STANDARD HOLES



uQseven STANDARD HOLES



GROUND PROBES



Schematic Title Q7 2.0 Reference Board		Created SGET
Size A3	Page Name CONFIGURATION	Rev 1
Date: Wednesday, December 16, 2015	Sheet 23	of 23